

Virtex UltraScale FPGA



Programmable System Integration

- Up to 5.5M system logic cells
- Integrated 100G Ethernet MAC and 150G Interlaken cores
- Integrated blocks for PCI Express®

Increased System Performance

- 30G transceivers for chip-to-chip, chip-to-optics, 28G backplanes
- 2,400Mb/s DDR4 for robust operation over varying PVT

Total Power Reduction

- Up to 40% lower power vs. Virtex-7 FPGAs
- 16G backplane capable transceivers at half the power
- Key process and architectural innovations such as ASIC-like clocking and block RAM cascading
- Range of device power options and design tool optimization methods including optimal logic packing and power optimization

Break-Out Performance and Capacity

Virtex® UltraScale™ devices provide the greatest performance and integration at 20nm, including serial I/O bandwidth and logic capacity. As the industry's only high-end FPGA at the 20nm process node, this family is ideal for applications ranging from 400G networking to large scale ASIC prototyping and emulation. These devices deliver a step-function in increased bandwidth and reduced latency for systems demanding massive data flow and packet processing. Based on the ASIC-class advantage of the Xilinx UltraScale architecture, Virtex UltraScale devices are co-optimized with the Vivado® Design Suite and leverage the UltraFAST™ design methodology to accelerate time to market.

Re-architecting the core for massive bandwidth with the UltraScale architecture

The UltraScale families are based on the first All Programmable architecture to span multiple nodes from planar through FinFET technologies and beyond, while also scaling from monolithic through 3D ICs. The UltraScale architecture provides diverse benefits and advantages to an array of markets and applications. The architecture combines enhancements in the configurable logic block (CLB), a dramatic increase in device routing, and a revolutionary ASIC-like clocking architecture with high-performance DSP, memory interface PHYs, and serial transceivers. All UltraScale architecture-based FPGAs are capable of pushing the system performance-per-watt envelope, enabling breakthrough speeds at high utilization. High system performance and multiple power reduction innovations make the UltraScale architecture the logical choice for many next-generation applications.

Building on the success of Xilinx's innovations, while looking ahead to tomorrow

Built with TSMC's 20nm SoC technology, the Virtex UltraScale family of FPGAs and 3D ICs combine the industry's best transceivers, integrated PCI Express, 100G Ethernet MAC/PCS, Interlaken blocks, 2nd generation silicon-stacked interconnect (SSI) technology, analytical placement, and co-optimization, with careful process optimization to achieve the highest performance-per-watt attainable at the process node. In addition, the Virtex UltraScale family leverages new IP Integrator technology, which allows designers to quickly stitch IP together by designing at the interface level. The IP Integrator provides correct-by-construction signal-level connectivity to enable an even higher level of productivity and integration. Each Virtex UltraScale device also has migration options to the Virtex UltraScale+™ family of FPGAs so that engineers can confidently design for today, keeping tomorrow's requirements in mind.

FEATURES OVERVIEW
20nm SoC process technology from TSMC

Industry-leading process from the #1 service foundry delivers a step function increase in performance-per-watt

- >40% greater performance-per-watt over Virtex-7 FPGAs

Next-generation routing, ASIC-like clocking & enhanced fabric

Enabling breakthrough speeds at high utilization

- Smaller area and greater power consistency
- Efficient CLB use and placement for reduced interconnect delay

Integrated 100G Ethernet MAC and 150G Interlaken cores

ASIC-class cores for breakthrough performance in packet processing

- 60K-100K system logic cell savings per port
- Up to 80% dynamic power savings vs. soft implementation

Enhanced DSP slices for diverse applications

Enabling a massive increase in fixed- and floating-point performance

- Up to 4.3TeraMACs of bandwidth at 741MHz operation
- Double-precision floating point in 30% fewer resources
- Complex fixed-point arithmetic in half the resources

High-speed memory cascading

Removes key bottlenecks in DSP and packet processing

- Eliminates fabric usage when building deep memories
- Reduces routing congestion
- Reduces dynamic power consumption

Step-function increase in 3D IC inter-die bandwidth

Virtual monolithic design

- Registered inter-die routing lines enable >600MHz
- Abundant and flexible clocking

Massive memory interface bandwidth

Next-generation DDR and serial memory support

- DDR4 support of up to 2,400Mb/s
- Support for server-class DIMMs – 8X capacity vs. Virtex-7 FPGAs
- Hybrid Memory Cube serial memory support of up to 30G

Massive I/O bandwidth and dramatic latency reduction

2X greater serial bandwidth than Virtex-7 FPGAs

- 30.5G chip-to-chip and chip-to-optics support
- 16.3G and 28G backplane support
- Smart blend of high-range and high-performance I/O for greater system efficiency

Integrated blocks for PCI Express

Complete end-to-end solution for multi-50G ports

- Gen3 x8 for 50G bandwidth per block
- Single-root I/O virtualization for data center applications
- Tandem field update for maximum system flexibility

Up to 40% power savings over Virtex-7 FPGAs

Total power reduction at every level: static, dynamic, I/O, and transceiver

- FPGA-optimized process and operating point
- Power-optimized transceivers and block RAM
- Fine-grained clock gating and superior logic utilization

Next-generation security

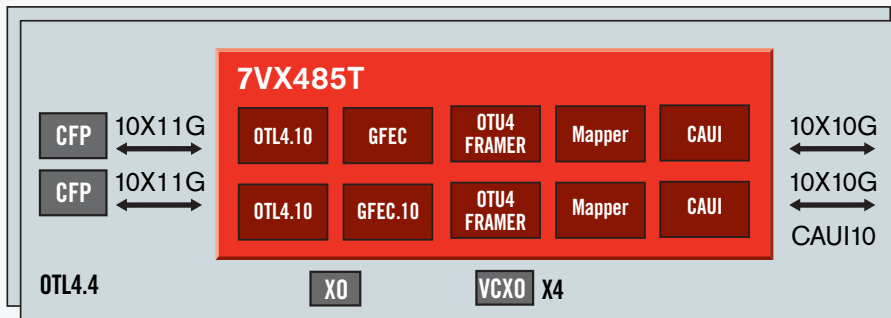
Enhanced features to protect IP and prevent tampering

- AES-GCM decryption, RSA-2048 authentication
- DPA countermeasures and permanent tamper penalty

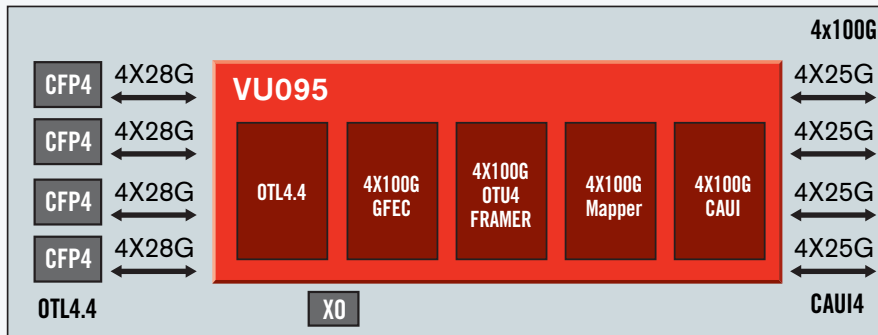
4x100G Transponder

Key UltraScale Portfolio Benefits:

Existing Infrastructure



Virtex UltraScale Solution



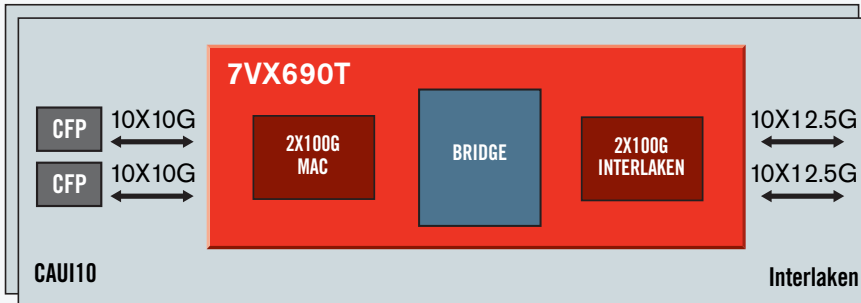
Solution Benefits
System Integration 2 Devices ⇒ 1 Device 2 line cards ⇒ 1 line card
System Performance 1X
BOM Cost 1X
Total Power -50%
Accerated Productivity Internal Frequency Synthesis

- High number of 28G transceivers for CFP4 modules, enabling integration with next-generation optics and higher port density
- Extensive number of VCXO oscillators integrates over nine clocking devices
- Enhanced clocking and routing and removal of processing bottlenecks enable 400G throughput on a single device
- SmartCORE™ IP including ITU G.709 GFEC, OTU4 Framer, and 100GbE to ODU4 Mapper for rapid implementation

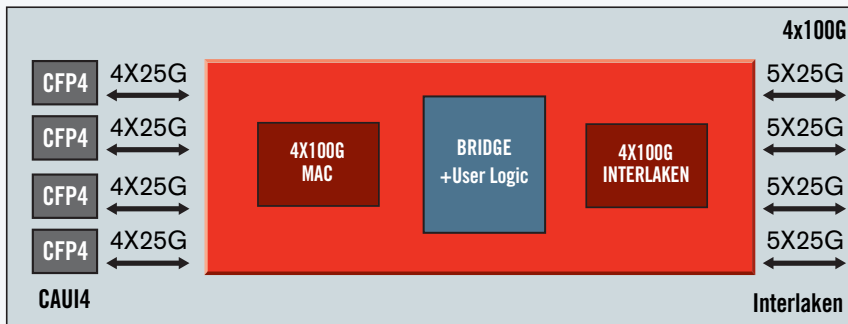
400G MAC to Interlaken Bridge

Key UltraScale+ Portfolio Benefits:

Existing Infrastructure



Virtex UltraScale Solution



Solution Benefits
Programmable System Integration 2 Devices ⇌ 1 Device 2 line cards ⇌ 1 line card
System Performance 1X
FPGA BOM Cost -30%
FPGA Total Power -60%
Accelerated Productivity Integrated 4X100G MAC Integrated 4X100G Interlaken

- Four 100G hard Ethernet MACs and four 100G Interlaken cores speed time to implementation, reduce latency, reduce power, and free up resources for additional functionality, e.g., packet processing
- High number of 28G transceivers for CFP4 module integration, enabling higher port density
- Enhanced clocking and routing to achieve 400G throughput on a single device
- 20nm process and a multitude of architectural enhancements to reduce power by 25%

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