Virtex-6 FPGA GTH Transceivers Characterization Report

CEI-11G-SR, CEI-11G-MR (Low Swing) and CAUI Electrical Interface

RPT135 (v1.0) June 10, 2011

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/10/11	1.0	Initial Xilinx release.

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Virtex-6 FPGA GTH Transceivers Characterization Report

Introduction

This characterization report compares the electrical performance of the Virtex®-6 FPGA GTH transceivers against OIF-CEI-02.0, *Common Electrical I/O (CEI)—Electrical and Jitter Interoperability agreements for 6G+ bps and 11G+ bps I/O and IEEE Std 802.3ba-2010 Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer specifications*. The characterization is performed as per OIF-CEI-02.0 for short reach (SR) and medium reach (MR) (low swing) interfaces and as per IEEE 802.3ba-2010 for a single 100-Gigabit attachment unit interface (CAUI) lane at a line rate of 11.18 Gb/s across voltage, temperature, and transceiver process corners.

This report is geared towards interfaces that are predominantly used as electrical interfaces for OTU-4 applications. SFI-S and OTL4.10, which are the most commonly used electrical interfaces in OTU-4 applications, are based on CEI-11G-SR and MR (low swing) respectively with respect to the electrical specifications. CAUI-like interfaces are also widely used in OTU-4 applications. Therefore, OTU-4 line rate of 11.18 Gb/s per lane is used for the characterization, even though the CAUI specification warrants 10.3125 Gb/s per lane.

The following tests are included in this report:

- Transmitter Near-End Output Eye, page 10
- Transmitter Output Jitter, page 12
- Transmitter Output Differential Amplitudes, page 15
- Transmitter Output Rise and Fall Times, page 16
- Transmitter Differential and Common Mode Output Return Loss, page 17
- Receiver Input Jitter Tolerance, page 20
- Receiver Differential and Common Mode Input Return Loss, page 29

Acronyms used in this guide include:

- BUJ Bounded uncorrelated jitter
- DCD Duty cycle distortion
- DJ Deterministic jitter
- ISI Inter symbol interference
- RJ Random jitter
- TJ Total jitter

Test Conditions

Table 1 and Table 2 show the supply voltage and temperature conditions, respectively.

Table 1: **Supply Voltage Test Conditions**

Condition	MGTHAVCC (V)	MGTHAVCCRX (V)	MGTHAVTT (V)	MGTHAVCCPLL (V)
V_{MIN}	1.075	1.075	1.140	1.710
V_{MAX}	1.125	1.125	1.260	1.890

Note: Other FPGA voltages stay at their nominal values.

Table 2: **Temperature Test Conditions**

Condition	Temperature (°C)
T_{-40}	–40
T_0	0
T_{100}	100

Transceiver Selection

Xilinx first performs volume generic transceiver characterization across process, voltage, and temperature. Protocol-specific characterization is subsequently performed using representative transceiver from generic characterization.

Summary of Results

The summary in Table 3 shows a comparison of the Virtex-6 FPGA GTH transceivers against the OIF-CEI-02.0 for SR specifications. Data reported in Table 3 represents the worst-case voltage, temperature, and process corner tested.

Table 3: **CEI-11G-SR Characterization Summary of Results**

Test	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Transmitter Output Jitter at 11.18 Gb/s	TJ	0.3	0.252	UI (p-p)[1]	Yes
	RJ	0.15	0.092	UI (p-p)	Yes
	BUJ[2]	0.15	0.047	UI (p-p)	Yes
Transmitter Output Differential Amplitude	Min	360	Programmable[3]	mV	Yes
Transmitter Output Differential Amplitude	Max	770	Programmable[3]	mV	Yes
Transmitter Output Rise and Fall Times	Rise	> 24	33.1	ps	Yes
	Fall	> 24	34.3	ps	Yes
Transmitter Differential Output Return Loss	Frequency Profile	See Figure 5, page 19		dB	Note[5]
Transmitter Common Mode Output Return Loss	Frequency Profile	See Figure 6, page 19		dB	Yes
Receiver Input Jitter Tolerance at 11.18 Gb/s	TJ (not including SJ)	0.7	0.72[4]	UI	Yes
	SJ = 80 MHz	0.05	0.054	UI	Yes
Receiver Differential Input Return Loss	Frequency Profile	See Figure 16, page 30		dB	Note[5]
Receiver Common Mode Input Loss	Frequency Profile	See Figure 17, page 30		dB	Note [5]

Notes:

1. Peak-to-peak.
2. Measured using a PRBS15 data pattern due to equipment limitations.
3. The programmable transmitter output amplitude settings can be found in the TX Configurable Driver section of UG371, *Virtex-6 FPGA GTH Transceivers User Guide*.
4. Specification required baseline jitter for jitter tolerance testing. The value in the test result column is the amount of jitter injected by the test setup.
5. Return loss is compliant over most of the frequency ranges. Although some frequency ranges are marginal with the frequency profile, the transmitter and receiver jitter performance shows that the Virtex-6 FPGA GTH transceivers meet or exceed OIF-CEI-02.0 and IEEE 802.3ba specifications. Due to board limitations, the return loss measurements included ~1 to 4 inches of channel and the connectors on the transceiver pins under test, of the ML627 characterization platform.

The summary in Table 4, page 8 shows a comparison of the Virtex-6 FPGA GTH transceivers against the OIF-CEI-02.0 for MR (low swing) specifications. Data reported in Table 4 represents the worst-case voltage, temperature, and process corner tested.

Table 4: **CEI-11G-MR (Low Swing) Characterization Summary of Results**

Test	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Transmitter Output Jitter at 11.18 Gb/s	TJ	0.3	0.252	UI (p-p)[1]	Yes
	RJ	0.15	0.092	UI (p-p)	Yes
	DCD [2]	0.05	0.012	UI (p-p)	Yes
	BUJ [2]	0.15	0.047	UI (p-p)	Yes
Transmitter Output Differential Amplitude	Min	360	Programmable [3]	mV	Yes
Transmitter Output Differential Amplitude	Max	770	Programmable [3]	mV	Yes
Transmitter Output Rise and Fall Times	Rise	> 24	33.1	ps	Yes
	Fall	> 24	34.3	ps	Yes
Transmitter Differential Output Return Loss	Frequency Profile	See Figure 5, page 19		dB	Note [5]
Transmitter Common Mode Output Return Loss	Frequency Profile	See Figure 6, page 19		dB	Yes
Receiver Input Jitter Tolerance at 11.18 Gb/s	TJ (not including SJ)	0.7	0.72 [4]	UI	Yes
	SJ = 80 MHz	0.05	0.054	UI	Yes
Receiver Differential Input Return Loss	Frequency Profile	See Figure 16, page 30		dB	Note [5]
Receiver Common Mode Input Loss	Frequency Profile	See Figure 17, page 30		dB	Note [5]

Notes:

1. Peak-to-peak.
2. Measured using a PRBS15 data pattern due to equipment limitations.
3. The programmable transmitter output amplitude settings can be found in the TX Configurable Drive section of UG371, *Virtex-6 FPGA GTH Transceivers User Guide*.
4. Specification required baseline jitter for jitter tolerance testing. The value in the test result column is the amount of jitter injected by the test setup.
5. Return loss is compliant over most of the frequency ranges. Although some frequency ranges are marginal with the frequency profile, the transmitter and receiver jitter performance shows that the Virtex-6 FPGA GTH transceivers meet or exceed OIF-CEI-02.0 and IEEE 802.3ba specification. Due to board limitations, the return loss measurements included ~1 to 4 inches of channel and the connectors on the transceiver pins under test, of the ML627 characterization platform.

The summary in Table 5 shows a comparison of the Virtex-6 FPGA GTH transceivers against the IEEE 802.3ba-2010 for CAUI electrical interface specifications. Data reported in Table 5 represents the worst-case voltage, temperature, and process corner tested.

Table 5: **CAUI Characterization Summary of Results**

Test	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Transmitter Output Jitter at 11.18 Gb/s	TJ	0.32	0.252	UI (p-p)[1]	Yes
	DJ[2]	0.17	0.152	UI (p-p)	Yes
Transmitter Output Differential Amplitude	Max	760	Programmable[3]	mV	Yes
Transmitter Output Rise and Fall Times	Rise	> 24	33.1	ps	Yes
	Fall	> 24	34.3	ps	Yes
Transmitter Differential Output Return Loss	Frequency Profile	See Figure 5, page 19		dB	Note[5]
Transmitter Common Mode Output Return Loss	Frequency Profile	See Figure 6, page 19		dB	Yes
Receiver Input Jitter Tolerance at 11.18 Gb/s	TJ (not including SJ)	0.62	0.69[4]	UI	Yes
	SJ = 80 MHz	0.05	0.078	UI	Yes
Receiver Differential Input Return Loss	Frequency Profile	See Figure 16, page 30		dB	Note[5]

Notes:

1. Peak-to-peak.
2. Measured using a PRBS15 data pattern due to equipment limitations.
3. The programmable transmitter output amplitude settings can be found in the TX Configurable Driver section of UG371, *Virtex-6 FPGA GTH Transceivers User Guide*.
4. Specification required baseline jitter for jitter tolerance testing. The value in the test result column is the amount of jitter injected by the test setup.
5. Return loss is compliant over most of the frequency ranges. Although some frequency ranges are marginal with the frequency profile, the transmitter and receiver jitter performance shows that the Virtex-6 FPGA GTH transceivers meet or exceed OIF-CEI-02.0 and IEEE 802.3ba specification. Due to board limitations, the return loss measurements included ~1 to 4 inches of channel and the connectors on the transceiver pins under test, of the ML627 characterization platform.

CEI-11G-SR, CEI-11G-MR (Low Swing) and CAUI Electrical Characterization Details

This section contains the detailed test methodology and test results for each test summarized in Table 3, page 7, Table 4, page 8, and Table 5, page 9. The GTH transceiver is configured using the GTH transceiver Wizard v1.7, including attribute settings. GTH transceiver attribute settings that differ from the GTH transceiver Wizard default setting are identified in the test setup and conditions table for each test.

Table 6 shows the PLL settings used for the characterization.

Table 6: **PLL Settings**

Data Rate (Gb/s)	PLL Frequency (GHz)	REFCLK Frequency (MHz)	PLL_CFG0[5:0] (N–1)	TXRATE / RXRATE
11.18	5.59	174.6875	31	`2'b00`

Transmitter Near-End Output Eye

Test Methodology

Transmitter Near-End Output Eye was measured using the bench setup shown in Figure 2, page 12. The device is configured to transmit a PRBS15 pattern on each of the TX data pins, and the resulting eye is captured using an Agilent 86100C Infiniium DCA-J/DCA-X wideband oscilloscope for 1000 samples at nominal voltage and room temperature conditions. The test setup and conditions are defined in Table 7.

Table 7: **Transmitter Near-End Output Eye Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J /DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	Nominal
Temperature	Room temperature
Pattern	PRBS15
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude	GTH transceiver attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 174.6875 MHz for 11.18 Gb/s

Test Results

Figure 1 shows the transmitter near-end output eye at 11.18 Gb/s.

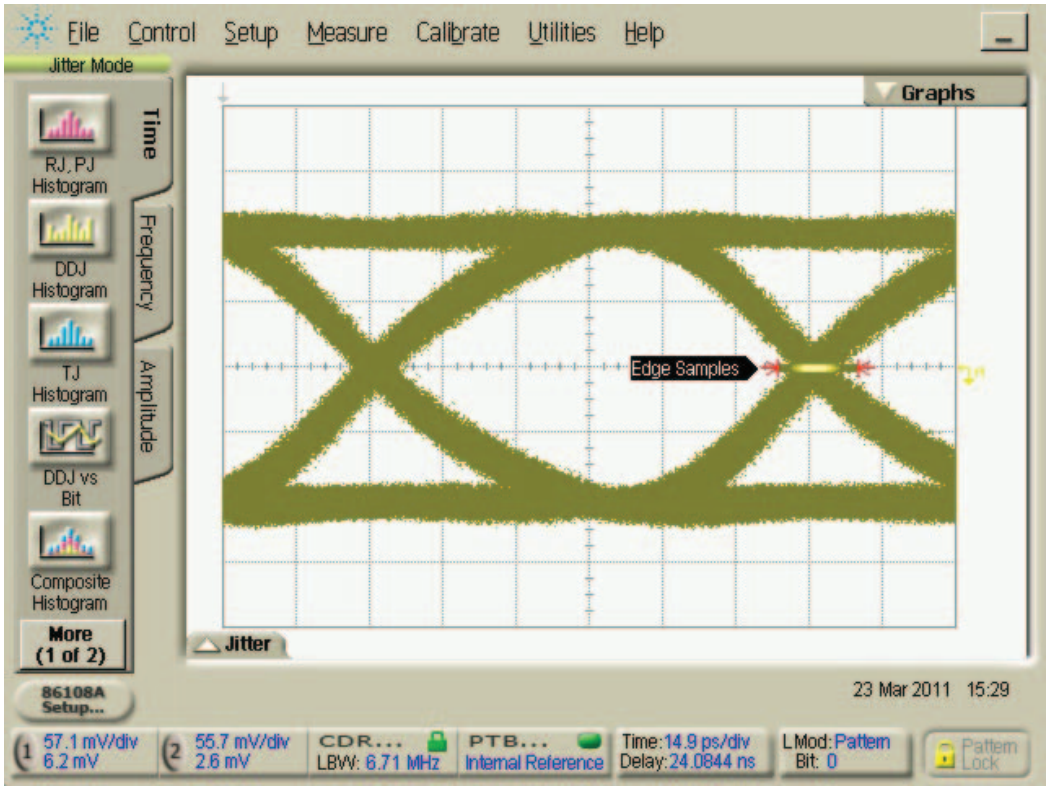

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Figure 1: **Transmitter Near-End Output Eye (11.18 Gb/s with 174.6875 MHz REFCLK)**

Transmitter Output Jitter

Test Methodology

Transmitter output jitter was measured using the bench setup shown in Figure 2. The DCA-J/DCA-X is used with the Agilent 86108A precision waveform analyzer to measure the output jitter. The Agilent 86108A contains a hardware clock recovery unit with adjustable loop bandwidth which is set to line rate/1667 as required by the specifications.

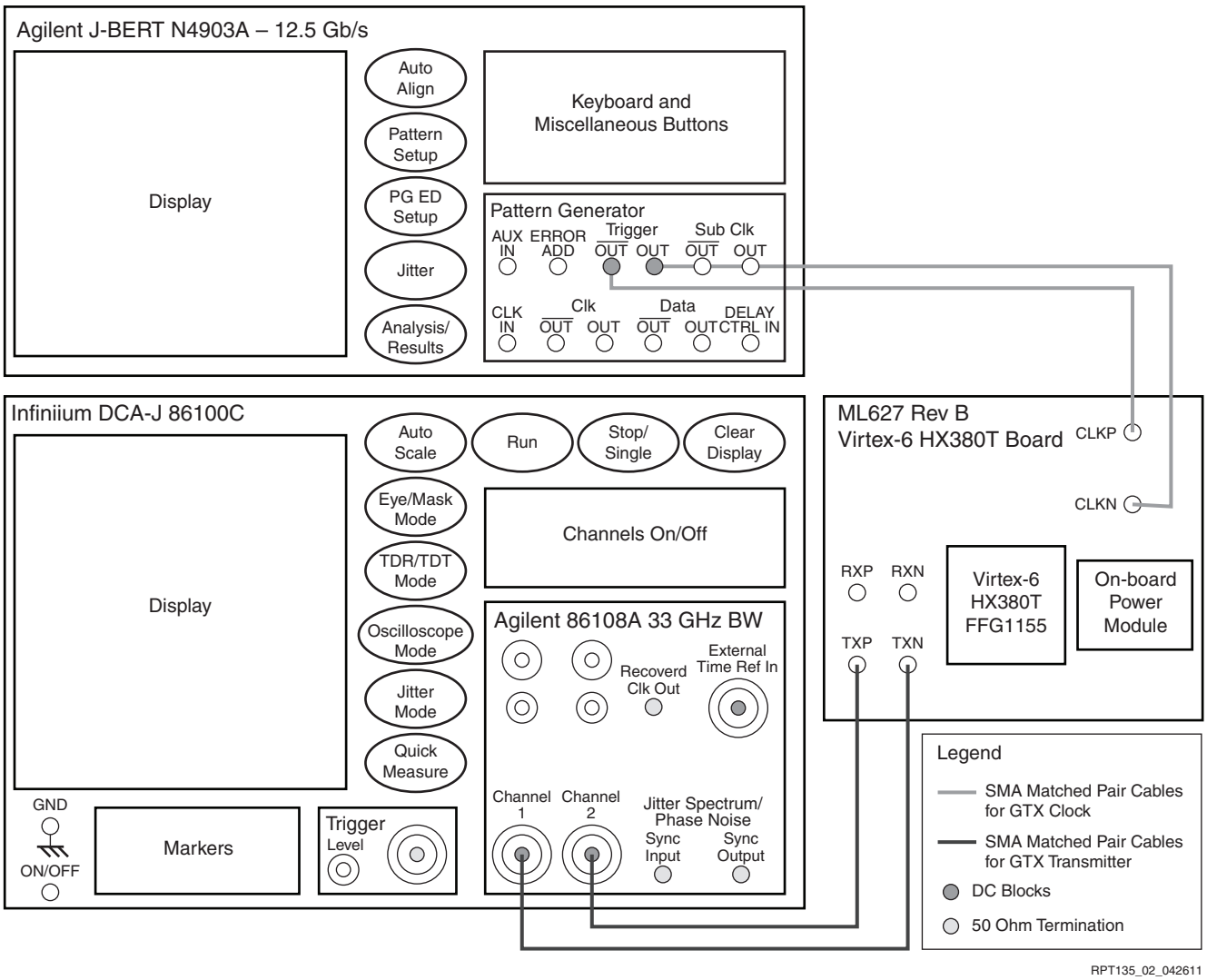

Figure 2: **Transmitter Output Jitter Test Setup Block Diagram**

Due to board limitations, the measurement is taken with ~3 to 4 inches of channel length between the TXP/TXN FPGA pins and the SMA connectors on the ML627 characterization platform. The added FR4 channel contributes additional ISI (DJ) when tested with a PRBS pattern; artificially increasing the output jitter measurement. As a result, the data presented in the figures below are pessimistic.

Table 8 defines the test setup and conditions for the transmitter output jitter.

Table 8: **Transmitter Output Jitter Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J/DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	PRBS31
BER	10^{-15}
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude/Emphasis	GTH transceiver attributes: TX_CFG0_LANE<n>[6:3] = `4'b0111` TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 174.6875 MHz for 11.18 Gb/s

Test Results

Figure 3 shows the transmitter output jitter test results at 11.18 Gb/s with a PRBS31 pattern and a BER of 10^{-15}.

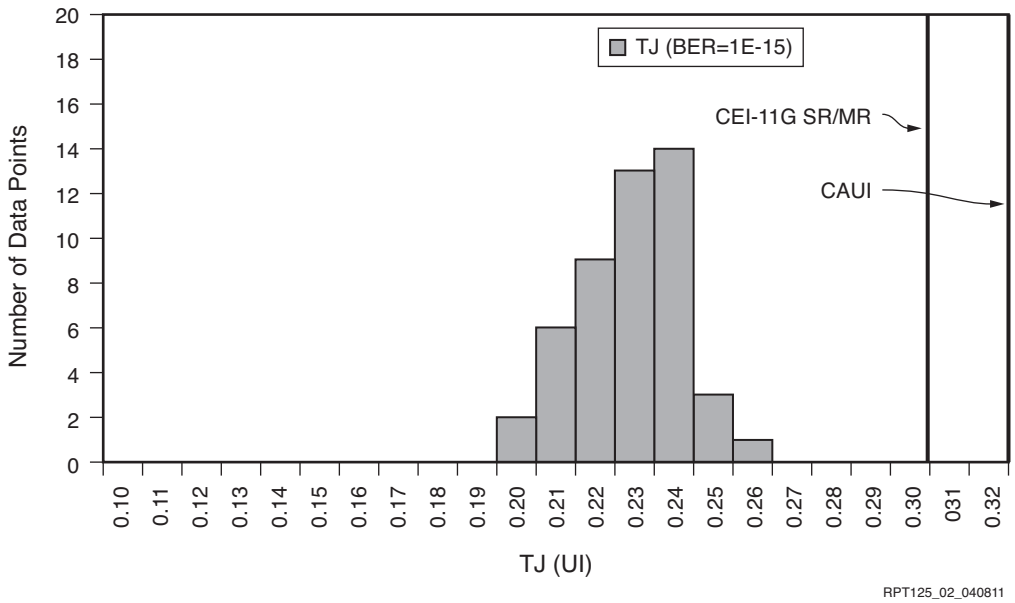

Figure 3: **Transmitter Output Jitter Test Results (11.18 Gb/s, PRBS31, BER = 10^{-15})**

Table 9 shows the maximum transmitter output jitter test result with a PRBS31/PRBS15 pattern and a BER of 10^{-15}.

Table 9: **Transmitter Output Jitter Test Results**

Parameter	Pattern	BER	TJ (UI p-p)[1]	RJ (fs RMS)	DJ (UI p-p)	DCD (UI p-p)	BUJ (UI p-p)
Maximum Transmitter Output Jitter	PRBS31	10^{-15}	0.252	522	N/A	N/A	N/A
	PRBS15	10^{-15}	N/A	N/A	0.152	0.012	0.047

Notes:

1. Peak-to-peak.

Transmitter Output Differential Amplitudes

Test Methodology

Transmitter output electrical specifications defines the transmitter output differential amplitude to be between 360 mV and 770 mV for CEI-11G-SR and CEI-11G-MR (low swing) and <700 mV for CAUI. The transmitter output differential amplitudes are measured using the same test setup as in Transmitter Output Jitter, page 12. Table 10 defines the test setup and conditions.

Table 10: **Transmitter Output Differential Amplitude Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J/DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	Five 1s and five 0s clock pattern (...`11000001111100`...) generated internally in the fabric of the FPGA
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude/ Post-Emphasis	GTH transceiver attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 174.6875 MHz for 11.18 Gb/s

Test Results

Transmitter output differential amplitude test results are shown inTable 11.

Table 11: **Transmitter Output Differential Amplitude Test Results**

Parameter	Min	Max	Units
Differential Amplitude = 11.18 Gb/s	403	515	mV

Transmitter Output Rise and Fall Times

Test Methodology

Transmitter output electrical specifications defines the minimum transmitter output rise and fall times as 24 ps. Transmitter output rise and fall times are measured using the same test setup as in Transmitter Output Jitter, page 12. Table 12 defines the test setup and conditions.

Table 12: **Transmitter Output Rise and Fall Time Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J /DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	Five 1s and five 0s clock pattern (...`11000001111100`...) generated internally in the fabric of the FPGA
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude/ Post-Emphasis	GTH transceiver attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 174.6875 MHz for 11.18 Gb/s

Test Results

The transmitter output rise and fall time test results are shown in Table 13.

Table 13: **Transmitter Output Rise and Fall Time Test Results**

Parameter	Rise Time (Min)	Fall Time (Min)	Units
Differential Amplitude = 11.18 Gb/s	33.1	34.3	ps

Transmitter Differential and Common Mode Output Return Loss

Test Methodology

OIF-CEI-02.0 defines the differential output return loss measurement as follows:

- CEI-11G-SR:
  - –8 dB or better between 100 MHz and 8.385 GHz (0.75 times the baud rate),
  - with a slope of 16.6 dB/dec between 8.385 GHz and 16.77 GHz (3/2 times the baud rate)
- CEI-11G-MR:
  - –8 dB or better between 100 MHz and 8.385 GHz (0.75 times the baud rate),
  - with a slope of 16.6 dB/dec between 8.385 GHz and 11.18 GHz

Differential output return loss for CAUI as per IEEE 802.3ba is defined by the mask as shown in Figure 5.

Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

OIF-CEI-02.0 defines transmit common mode output return loss measurement as follows:

- CEI-11G-SR:
  - –6 dB or better between 100 MHz and 8.385 GHz (0.75 times the baud rate).

Common mode output return loss for CAUI as per IEEE 802.3ba is defined by the mask as shown in Figure 6.

The vector network analyzer (VNA) interfaces to the host PC through the GPIB. After the measurement parameters are set, calibration begins. Four cables are included in the calibration process. VNA measurements are independent of voltage and are accurate up to 16 GHz. A digital multimeter (DVM) confirms the differential resistance is 100Ω before the measurement. Due to board limitations, the measurement is taken with ~1 to 4 inches of channel length between the TXP/TXN FPGA pins and the SMA connectors on the ML627 characterization platform.

Table 14 defines the test setup and conditions.

Table 14: **Differential and Common Mode Output Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES vector network analyzer
TX Coupling/Termination	Differential, DC coupled into 50Ω to GND
Voltage and Temperature	Typical voltage, room temperature
Frequency Sweep	50 MHz to 16 GHz (10 MHz steps)
Test Fixture	ML627 test fixture with 1-inch board trace using low profile, zero insertion force (ZIF) socket
REFCLK	Not available
Source Power	0 dBm

Table 14: **Differential and Common Mode Output Return Loss Test Setup and Conditions *(Cont'd)***

Parameter	Value
Averaging Calibration	1
Intermediate Frequency (IF)	100 Hz

Figure 4 shows the test setup for the return loss measurement.

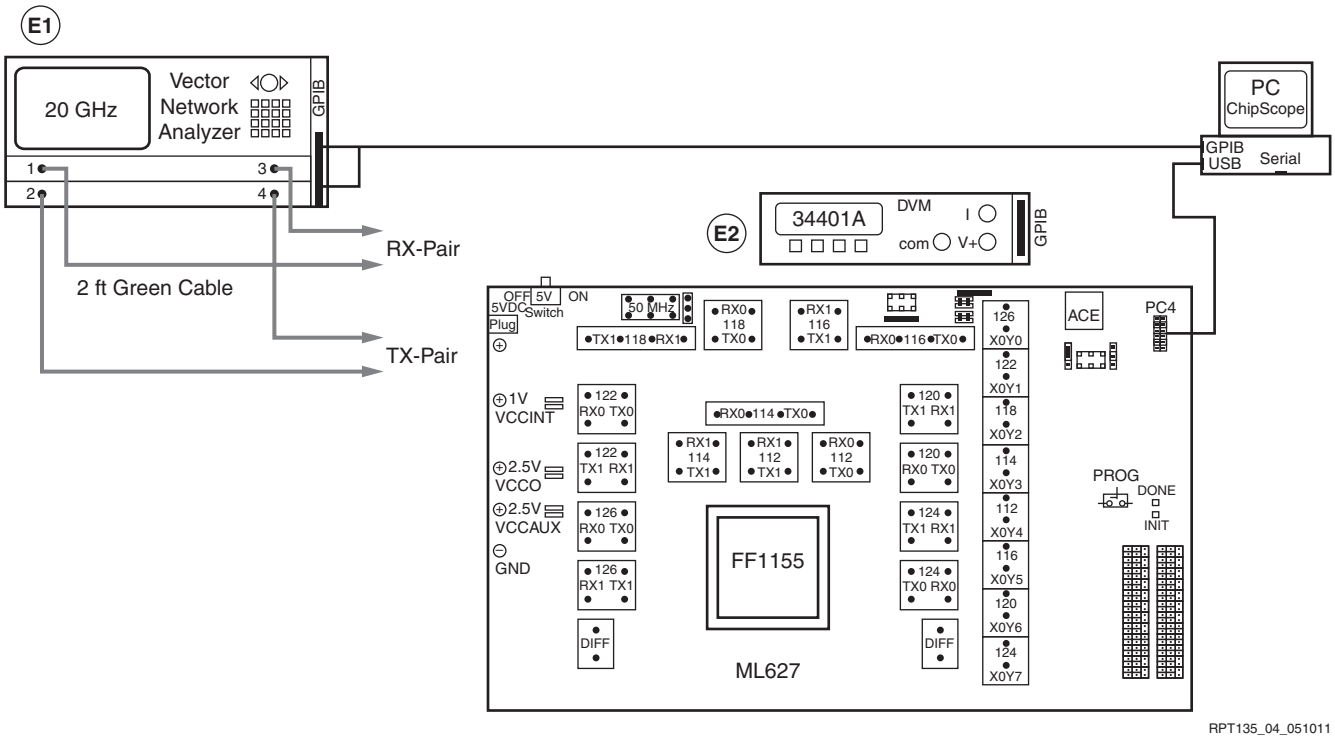

Figure 4: **Return Loss Test Setup Block Diagram**

Test Results

Figure 5 shows the transmitter differential output return loss measurement.

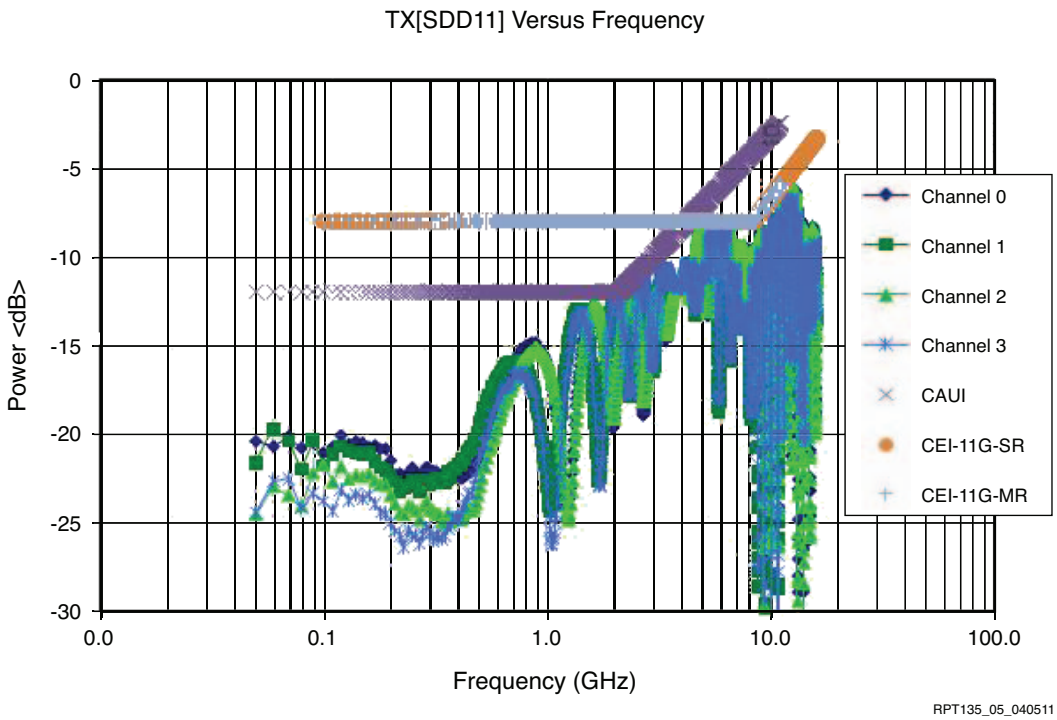

Figure 5: **Transmitter Differential Output Return Loss Measurement**

Figure 6 shows the transmitter common mode output return loss measurement.

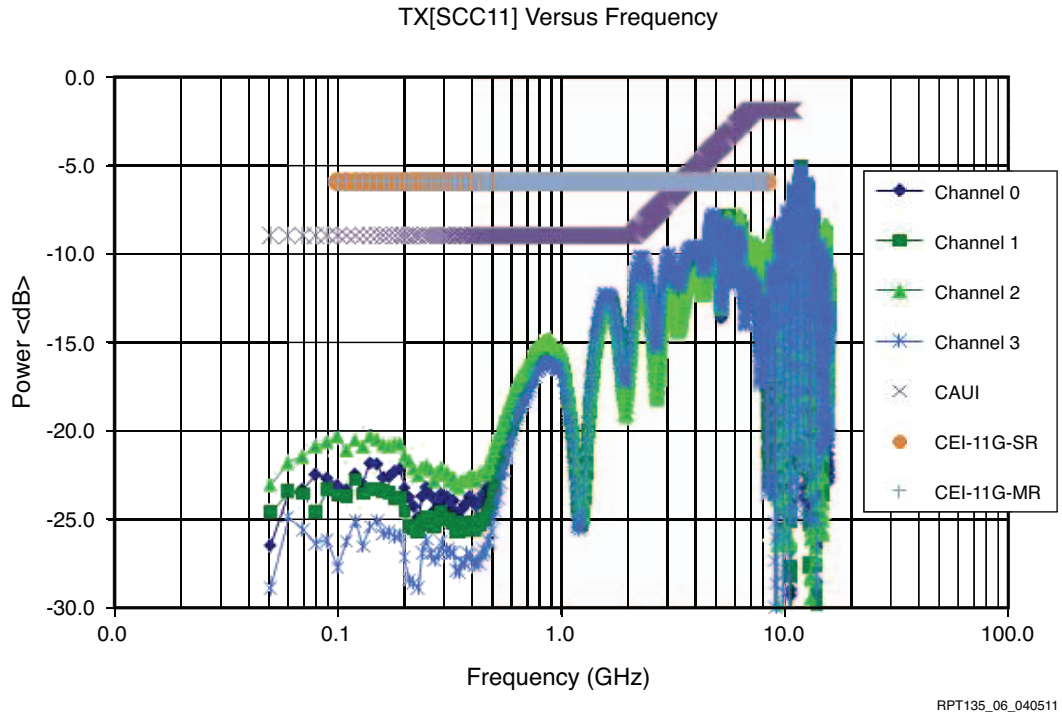

Figure 6: **Transmitter Common Mode Output Return Loss Measurement**

Receiver Input Jitter Tolerance

Test Methodology

Receiver input jitter tolerance is measured using the test setup shown in Figure 7. The J-BERT pattern generator generates a PRBS31 pattern. Random jitter (RJ) and bounded uncorrelated jitter (BUJ) are injected as per specification requirements for CEI-11G SR/MR and CAUI respectively. There is no difference in the specifications between CEI-11G-SR and MR for receiver jitter tolerance. DJ in the form of ISI is added using 9 inches of board trace (5 inches of which are from a BERTScope ISI test board). Sinusoidal jitter (SJ) is swept from 1 kHz to 80 MHz. The GTH transceiver under test recovers the data and transmits the pattern back to the error detector input of the J-BERT, where bit errors are measured. The test is performed with a +200 and –200 PPM offset between the J-BERT data generator and the reference clock provided to the GTH transceiver under test.

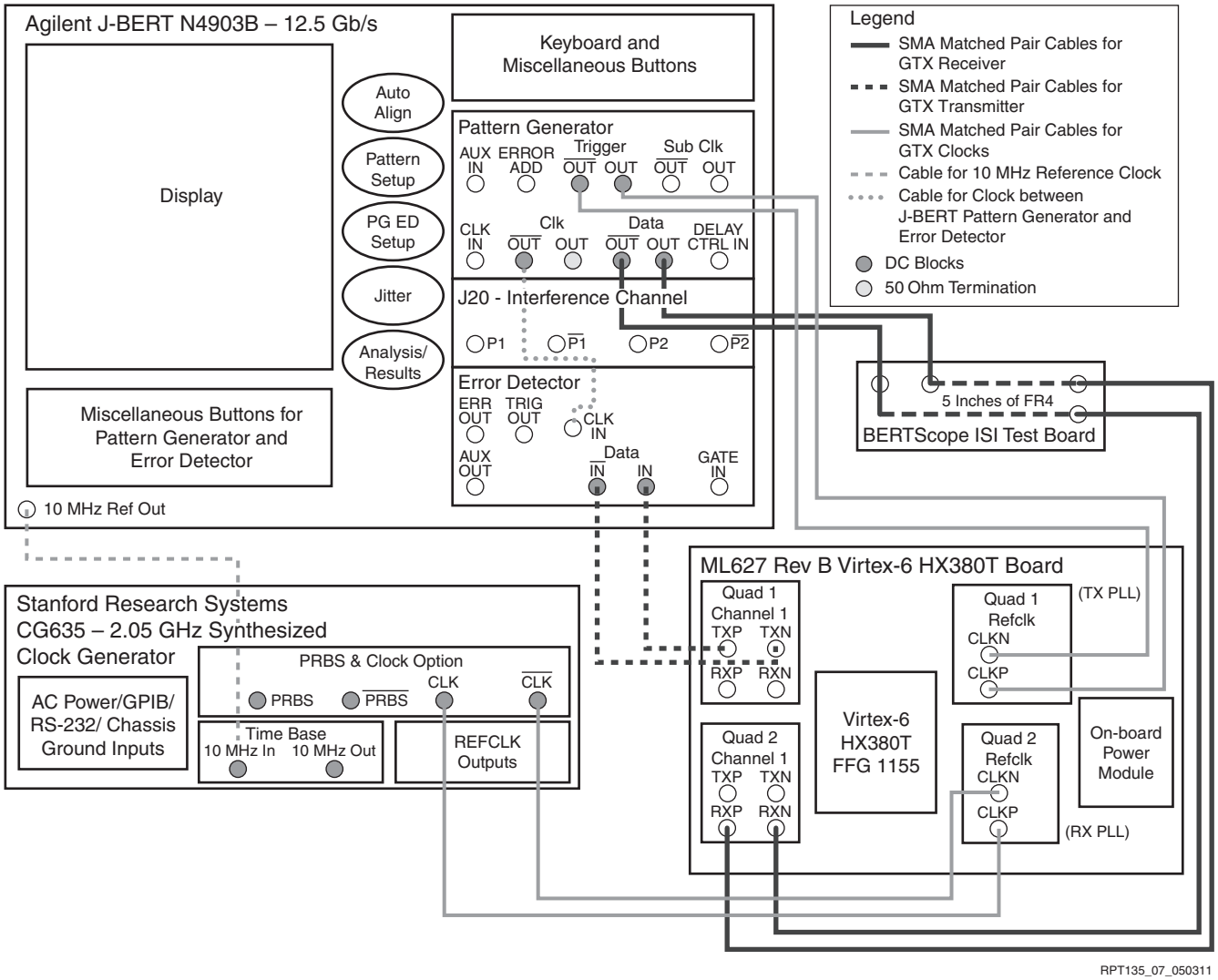

Figure 7: **Receiver Jitter Tolerance Setup Block Diagram**

Figure 8 shows a scope capture of the jitter injected to the GTH transceiver under test for CEI-11G-SR/MR testing. In addition to RJ, BUJ, and DJ, SJ is applied during the test.

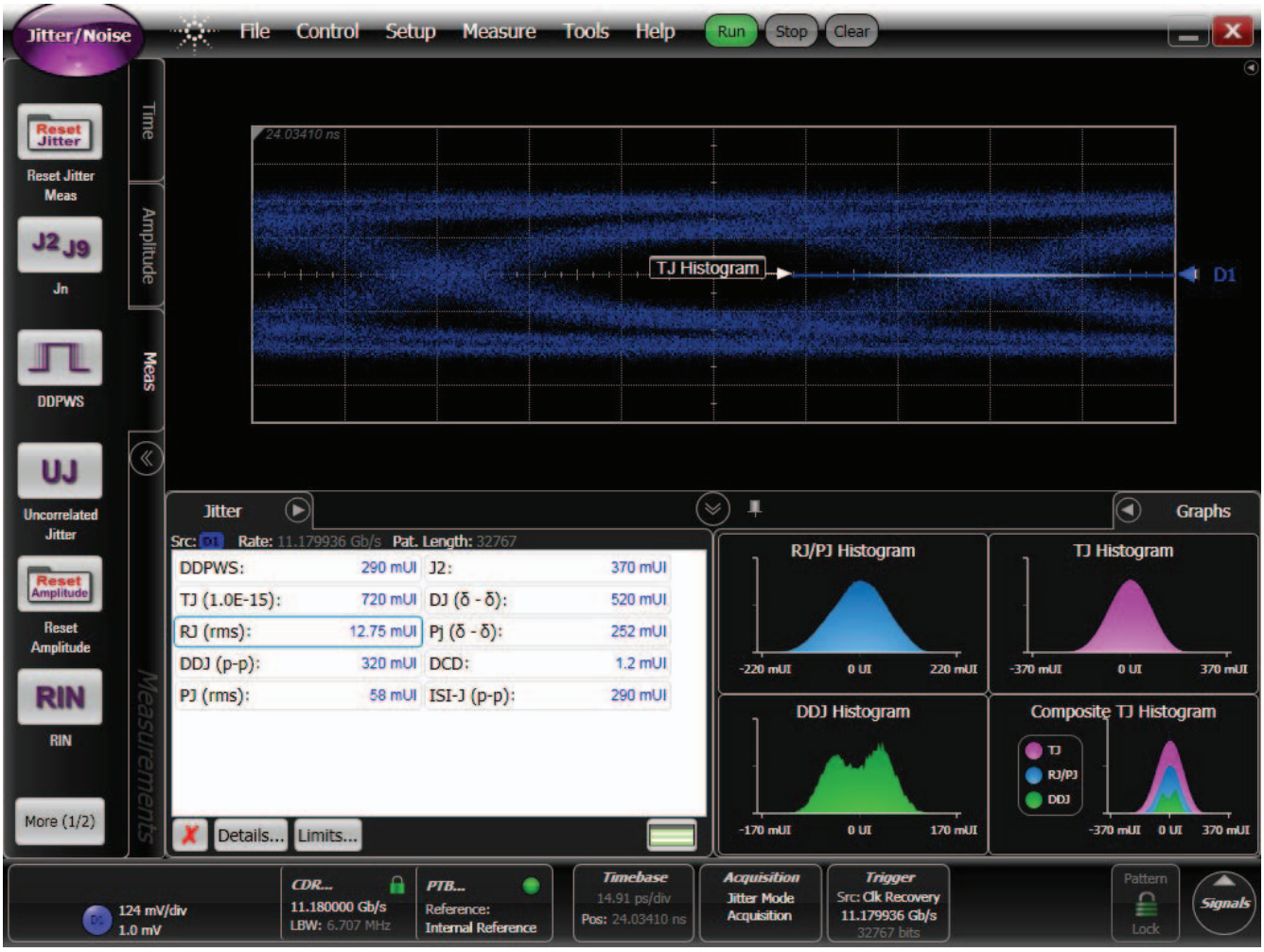

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Figure 8: **CEI-11G-SR/MR Receiver Jitter Tolerance Setup—TJ Breakdown with RJ, BUJ, and DJ Injected on a PRBS15 Data Pattern**

Notes for Figure 8:

1. PRBS31 is used for the actual measurements.

Figure 9 shows a scope capture of the input eye to the GTH transceiver under test for CEI-11G-SR/MR testing.

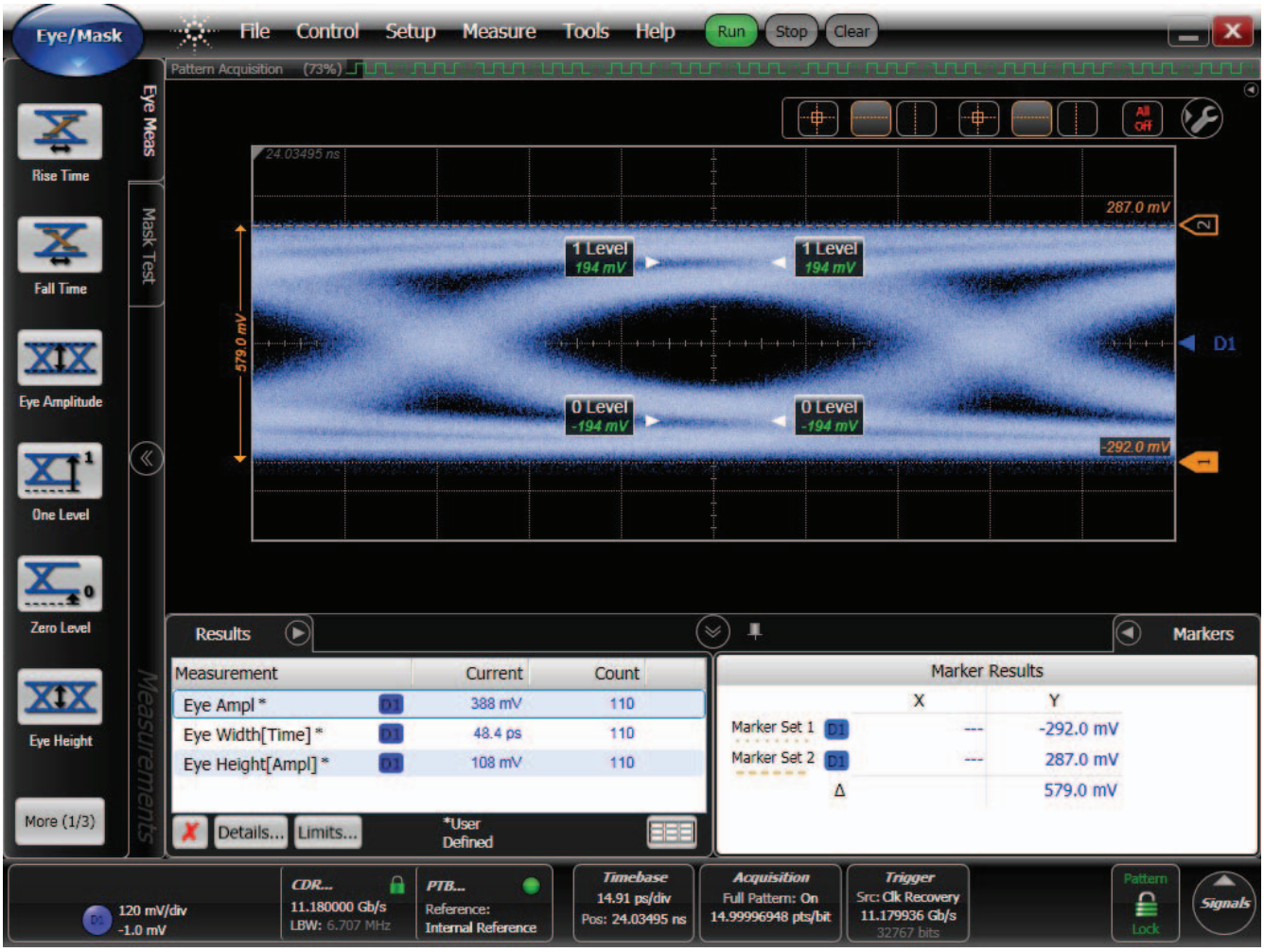

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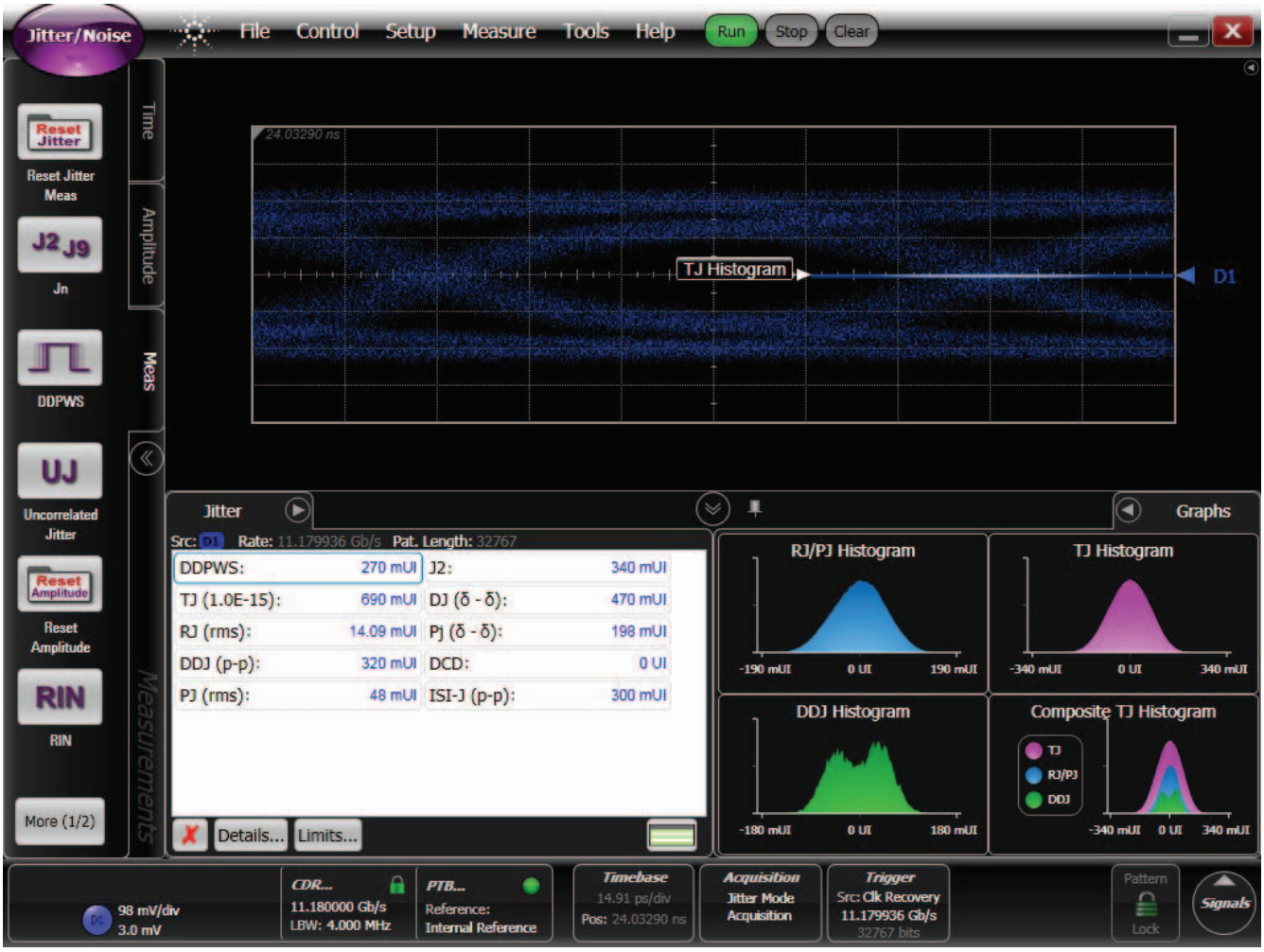
Figure 9: **CEI-11G-SR/MR Receiver Jitter Tolerance Setup—Input Eye with RJ, BUJ, DJ, and SJ Injected on a PRBS15 Data Pattern**

Notes for Figure 9:

1. PRBS31 is used for the actual measurement.
2. RX inner eye opening is chosen to be ~110 mV as required by the specification.

Figure 10 shows a scope capture of the jitter injected to the GTH transceiver under test for CAUI testing. In addition to RJ, BUJ, and DJ, SJ is applied during the test.



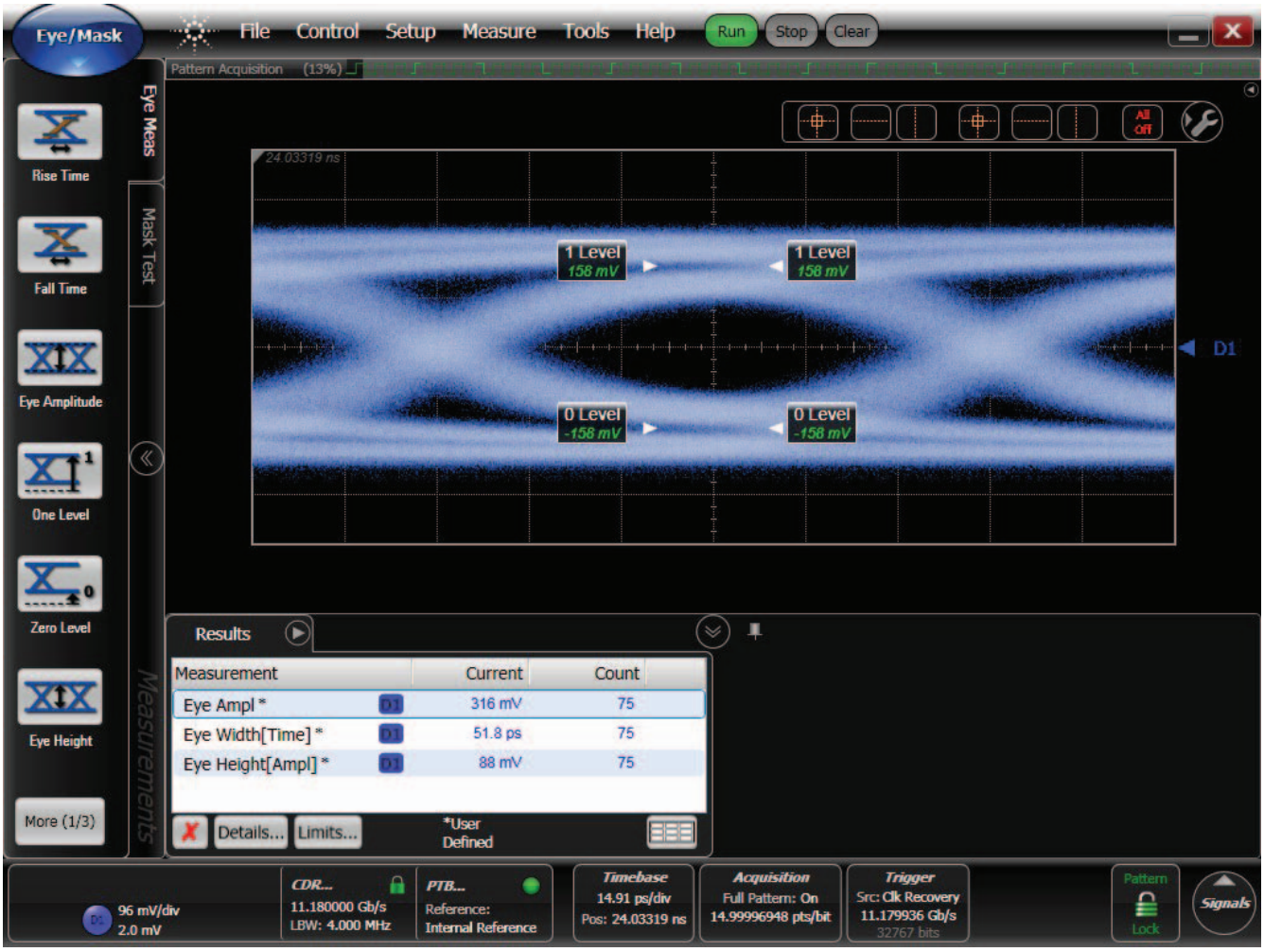
RPT135_10_040811

Figure 10: **CAUI Receiver Jitter Tolerance Setup—TJ Breakdown with RJ, BUJ, and DJ Injected on a PRBS15 Data Pattern**

Notes for Figure 10:

1. PRBS31 is used for the actual measurements.

Figure 11 shows a scope capture of the input eye to the GTH transceiver under test for CAUI testing.



RPT135_11_040811

Figure 11: **CAUI Receiver Jitter Tolerance Setup—Input Eye with RJ, BUJ, DJ, and SJ Injected on a PRBS15 Data Pattern**

Notes for Figure 11:

1. PRBS31 is used for the actual measurement.
2. RX inner eye opening is chosen to be ~85 mV as required by the specification.

Table 15 defines the test setup and conditions for the receiver jitter tolerance.

Table 15: **Receiver Jitter Tolerance Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent J-BERT N4903B
RX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	PRBS31

Injected Jitter	CEI-11G-SR/MR:
	Sum of the following.
	TJ = 0.720 UI_{p-p} (BER = 10^{-15})
	• RJ = 0.200 UI_{p-p}
	• DJ = 0.520 UI_{p-p}
	  • BUJ = 0.250 UI_{p-p}
	  • ISI = 0.290 UI_{p-p}
	SJ = Tested to failure; Frequency sweep = {1 kHz–80 MHz}
	
	CAUI:
	TJ = 0.690 UI_{p-p} (BER = 10^{-15})
	• RJ = 0.220 UI_{p-p}
	• DJ = 0.470 UI_{p-p}
	  • BUJ = 0.198 UI_{p-p}
	  • ISI = 0.300 UI_{p-p}
	SJ = Tested to failure; Frequency sweep = {1 kHz–80 MHz}

J-BERT Output Amplitude Setting (pk-pk)	CEI-11G-SR/MR: • 680 mV CAUI: • 560 mV
BER	10^{-15} (measured at 10^{-9}, extrapolated to 10^{-15})
Load Board	ML627 characterization platform, Revision B(FF1155)
Attributes	GTH transceiver attributes: (1) • RX_CTLE_CTRL=`16'h00CF` • RX_AGC_CTRL= `16'h0030` • RX_AEQ_VAL0 = `16'h03C0` • RX_AEQ_VAL1 =`16'h0000`
REFCLK	174.6875 MHz sourced from the J-BERT 174.6875 MHz ±200 ppm offset from CG635 Stanford Research synthesized clock generator

Notes:

1. AGC is set to fixed decimal value 16. DFE is set in AUTO mode. CTLE is set to decimal value 12.

Test Results

Figure 12 shows the receiver jitter tolerance SJ sweep results for CEI-11G-SR/MR. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 15.

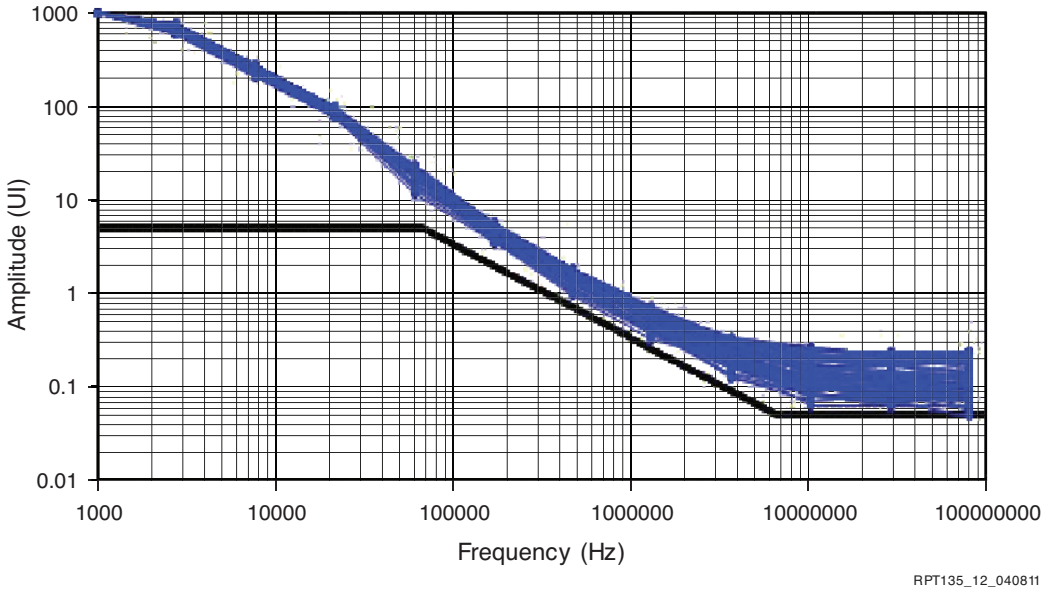


Figure 12: **CEI-11G-SR/MR Receiver Jitter Tolerance SJ Sweep Test Results**

Notes for Figure 12:

1. PRBS31, BER = 10^{-15}

Figure 13 shows the SJ tolerance at SJ frequency of 80 MHz for CEI-11G-SR/MR. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 15.

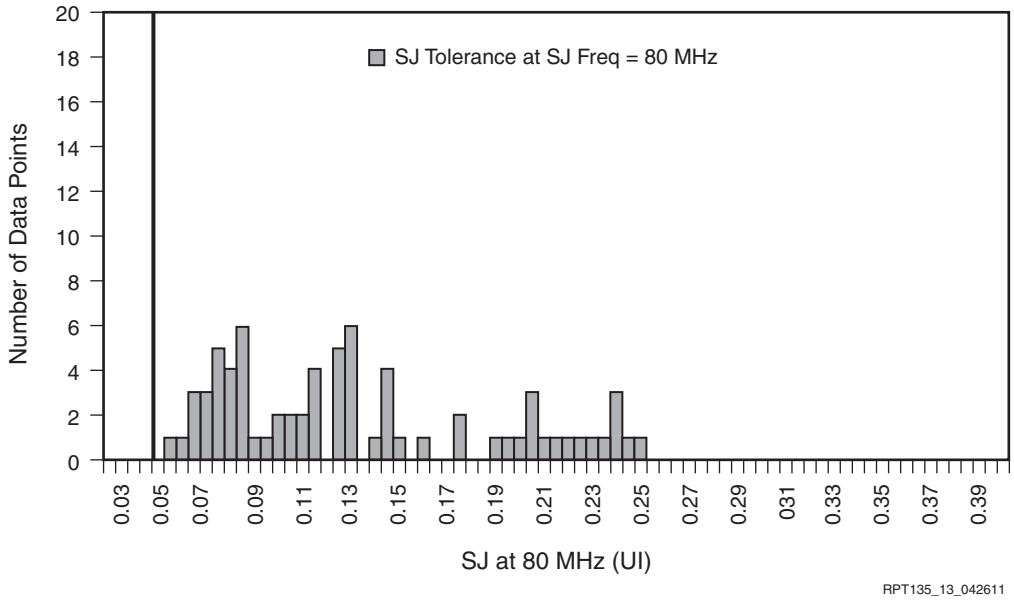


Figure 13: **CEI-11G-SR/MR Receiver Sinusoidal Jitter Tolerance at 80 MHz Test Results**

Notes for Figure 13:

1. PRBS31, BER = 10^{-15}

Table 16 shows the minimum receiver SJ tolerance for 80 MHz for CEI-11G-SR/MR. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 15.

Table 16: **CEI-11G-SR/MR Receiver Jitter Tolerance Test Results**

Parameter	Test Condition	BER	Min SJ Tolerance	Units
CEI-11G-SR/MR Receiver Jitter Tolerance	SJ = 80 MHz	10^{-15}	0.0540	UI

Figure 14 shows the receiver jitter tolerance SJ sweep for single channel of CAUI. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 15.

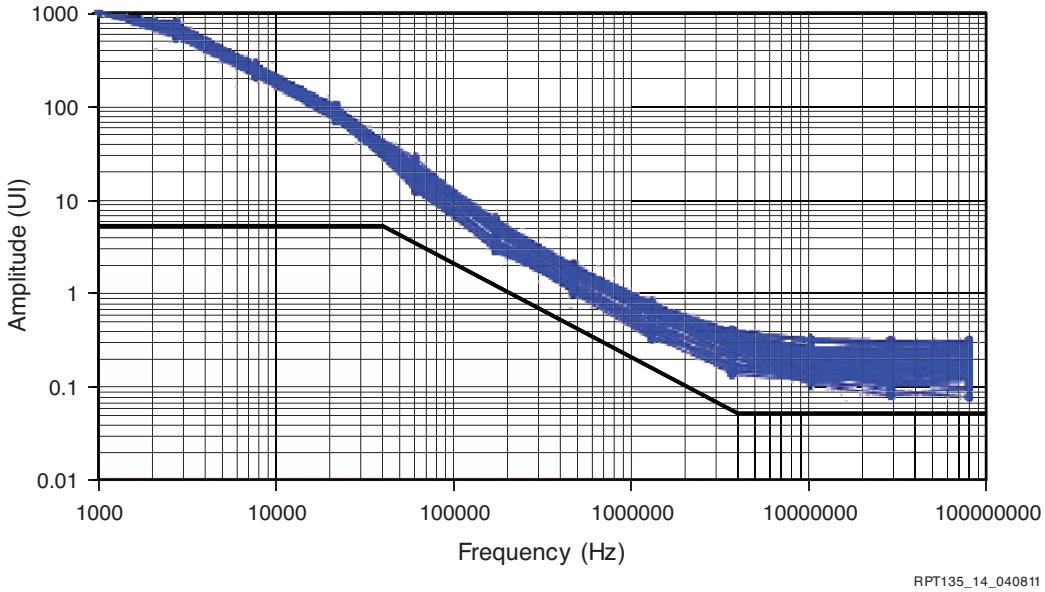


Figure 14: **CAUI Receiver Jitter Tolerance SJ Sweep Test Results**

Notes for Figure 14:

1. PRBS31, BER = 10^{-15}

Figure 15 shows the SJ at 80 MHz for CAUI. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 15.

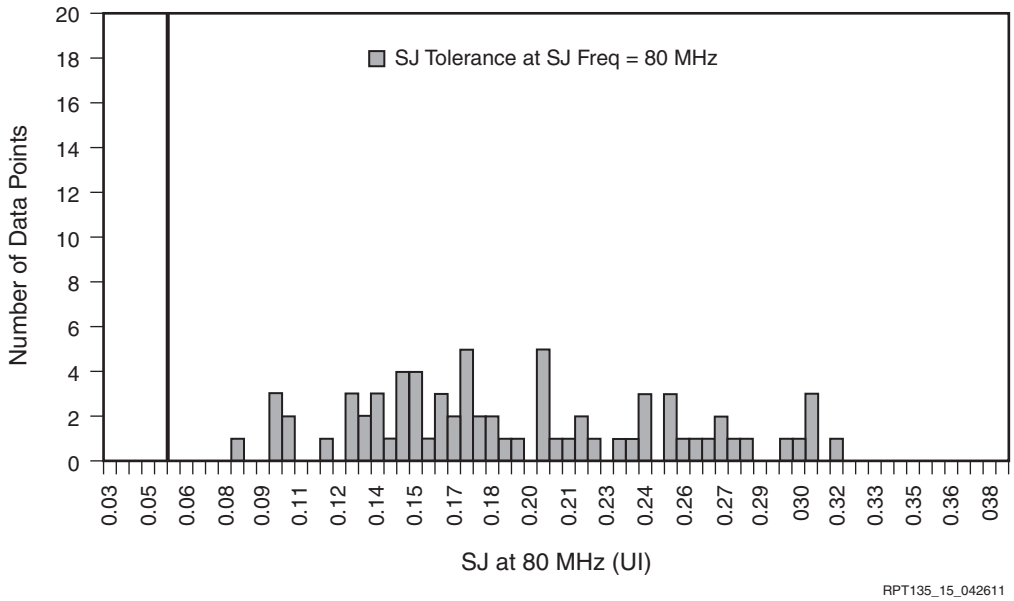


Figure 15: **CAUI Receiver Sinusoidal Jitter Tolerance at 80 MHz Test Results**

Notes for Figure 15:

1. PRBS31, BER = 10^{-15}

Table 17 shows the minimum receiver SJ tolerance for 80 MHz for CAUI. SJ is applied in addition to RJ, BUJ, and DJ as defined in Table 15.

Table 17: **CEI-6G-SR Receiver Jitter Tolerance Test Results**

Parameter	Test Condition	BER	Min SJ Tolerance	Units
CAUI Receiver Jitter Tolerance	SJ = 80 MHz	10^{-15}	0.0781	UI

Receiver Differential and Common Mode Input Return Loss

Test Methodology

Receiver input differential and common mode return loss setup is the same as in Transmitter Differential and Common Mode Output Return Loss, page 17.

Table 18 defines the test setup and conditions. Due to board limitations, the measurement is taken with ~1 to 4 inches of channel length between the FPGA pins and the SMA connectors on the ML627 characterization platform.

Table 18: **Receiver Differential and Common Mode Input Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES vector network analyzer
RX Configuration/Amplitude	RX configured for 100Ω differential termination (center tap to GND), AC coupled using both internal and external caps
Voltage and Temperature	Typical voltage, room temperature
Frequency Sweep	50 MHz to 16 GHz (10 MHz steps)
Test Fixture	ML627 characterization platform, Revision B(FF1155)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency (IF)	100 Hz

Test Results

Figure 16 shows the receiver differential input return loss measurement.

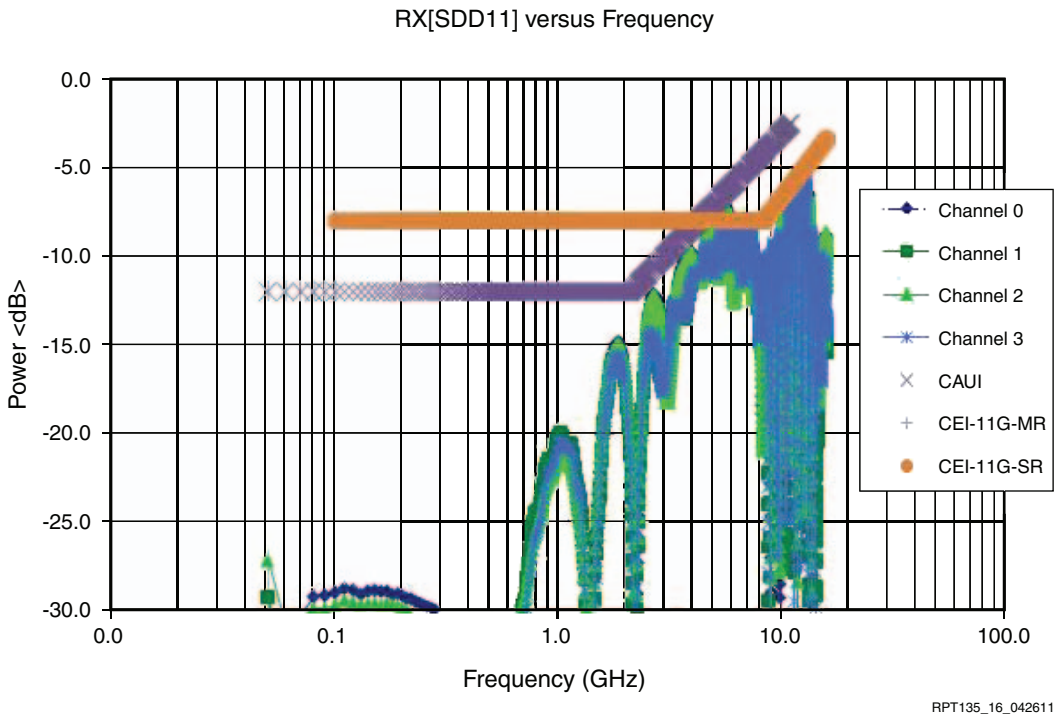


Figure 16: **Receiver Differential Input Return Loss Measurement**

Figure 17 shows the receiver common mode input return loss measurement.

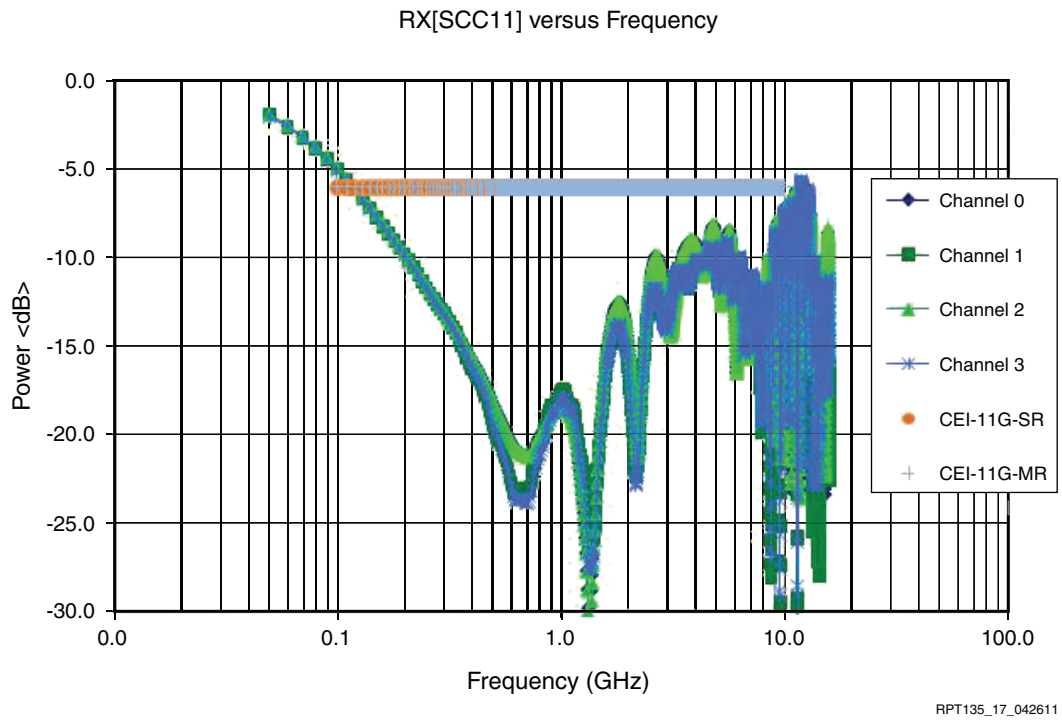


Figure 17: **Receiver Common Mode Input Return Loss Measurement**