Virtex-6 FPGA GTH Transceivers SFP+ Electrical Specification

Characterization Report

RPT136 (v1.0) June 10, 2011

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/10/2011	1.0	Initial Xilinx release.

Table of Contents

Revision History 2

Virtex-6 FPGA GTH Transceivers SFP+ Electrical Specification

Introduction 5
Test Conditions 6
Transceiver Selection 6
Summary of Results 7
SFP+ Electrical Characterization Details 8
Transmitter Near-End Output Eye 8
Test Methodology 8
Test Results 9
Transmitter Output Jitter 11
Test Methodology 11
Test Results 12
Transmitter Output Differential Amplitudes 14
Test Methodology 14
Test Results 14
Transmitter Output Rise and Fall Times 15
Test Methodology 15
Test Results 15
Transmitter Differential and Common Mode Output Return Loss 16
Test Methodology 16
Test Results 18
Receiver Input Jitter Tolerance 20
Test Methodology 20
Test Results 26
Receiver Differential and Common Mode Input Return Loss 29
Test Methodology 29
Test Results 30

Virtex-6 FPGA GTH Transceivers SFP+ Electrical Specification

Introduction

This characterization report compares the electrical performance of the Virtex®-6 FPGA GTH transceiver against the SFP+ (SFI) SFF-8431 electrical specification. The characterization is performed as per SFF-8431 specification at a line rate of 10.3125 Gb/s, 11.1 Gb/s across voltage, temperature, and process corners.

The following tests are included in this report:

- Transmitter Near-End Output Eye, page 8
- Transmitter Output Jitter, page 11
- Transmitter Output Differential Amplitudes, page 14
- Transmitter Output Rise and Fall Times, page 15
- Transmitter Differential and Common Mode Output Return Loss, page 16
- Receiver Input Jitter Tolerance, page 20
- Receiver Differential and Common Mode Input Return Loss, page 29

Test Conditions

Table 1 and Table 2 show the supply voltage and temperature conditions, respectively.

Table 1: **Supply Voltage Test Conditions**

Condition	MGTHAVCC (V)	MGTHAVCCRX (V)	MGTHAVTT (V)	MGTHAVCCPLL (V)
V_{MIN}	1.075	1.075	1.140	1.710
V_{MAX}	1.125	1.125	1.260	1.890

Note: Other FPGA voltages stay at their nominal values.

Table 2: **Temperature Test Conditions**

Condition	Temperature (°C)
T_{-40}	–40
T_0	0
T_{100}	100

Transceiver Selection

Xilinx first performs volume generic transceiver characterization across process, voltage, and temperature. Protocol-specific characterization is subsequently performed using representative transceivers from generic characterization.

Summary of Results

The summary in Table 3 shows a comparison of the Virtex-6 FPGA GTH transceiver against the SFP+ SFF-8431 specifications. Data reported in Table 3 represents the worst-case voltage, temperature, and process corner tested.

Table 3: **SFP+ Characterization Summary of Results**

Test	Parameter	Specification	Worst-Case Test Result	Units	Compliant
Transmitter Output Jitter at 10.3125 Gb/s	TJ	0.28	0.251	UI (p-p)[1]	Yes
	DDJ	0.1	0.0950	UI (p-p)	Yes
	DDPWS	0.055	0.0285	UI (p-p)	Yes
	UJ	0.023	0.008	UI (RMS)	Yes
Transmitter Output Jitter at 11.1 Gb/s	TJ	0.28	0.234	UI (p-p)	Yes
	DDJ	0.1	0.0915	UI (p-p)	Yes
	DDPWS	0.055	0.0146	UI (p-p)	Yes
	UJ	0.023	0.0102	UI (RMS)	Yes
Transmitter Output Differential Amplitude	Min	190	Programmable[2]	mV	Yes
	Max	700	Programmable[2]	mV	Yes
Transmitter Output Rise and Fall Times	Rise	>24	33.9	ps	Yes
	Fall	>24	33	ps	Yes
Transmitter Differential Output Return Loss	Frequency Profile	See Figure 6, page 17		dB	Note [4]
Transmitter Common Mode Output Return Loss	Frequency Profile	See Figure 7, page 18		dB	Note [4]
Receiver Input Jitter Tolerance at 10.3125 Gb/s	TJ (not including SJ)	0.70	>0.72[3]	UI	Yes
	SJ = 40 MHz	0.05	0.064	UI	Yes
Receiver Input Jitter Tolerance at 11.1 Gb/s	TJ (not including SJ)	0.70	>0.72[3]	UI	Yes
	SJ = 40 MHz	0.05	0.064	UI	Yes
Receiver Differential Input Return Loss	Frequency Profile	See Figure 15, page 26		dB	Note [4]
Receiver Common Mode Input Loss	Frequency Profile	See Figure 16, page 27		dB	N/A

Notes:

1. Peak-to-peak.
2. The programmable transmitter output amplitude settings can be found in the TX Configurable Driver section of UG371, *Virtex-6 FPGA GTH Transceivers User Guide*.
3. Specification required baseline jitter for jitter tolerance testing. The value in the test result column is the amount of jitter injected by the test setup.
4. Return loss is compliant over most of the frequency ranges. Although some frequency ranges are marginal with the frequency profile, the transmitter and receiver jitter performance shows that the Virtex-6 FPGA GTH transceiver meets or exceeds SFF-8431.

SFP+ Electrical Characterization Details

This section contains the detailed SFP+ test methodology and test results for each test summarized in Table 3, page 7. The GTH transceiver is configured using the Virtex-6 FPGA GTH transceiver Wizard v1.7, including attribute settings. GTH transceiver attribute settings that differ from the GTH transceiver Wizard default setting are identified in the test setup and conditions table for each test.

Table 4 shows the PLL settings used for the characterization.

Table 4: **PLL Settings**

Data Rate (Gb/s)	PLL Frequency (Gb/s)	REFCLK Frequency (MHz)	PLL_CFG0[5:0] (N–1)	TXRATE / RXRATE
10.3125	5.15625	156.25	32	`2'b00`
11.1	5.550	173.4375	31	`2'b00`

Transmitter Near-End Output Eye

Test Methodology

The device is configured to transmit a PRBS15 pattern on each of the TX data pins, and the resulting eye is captured using an Agilent 86100C Infiniium DCA-J wideband oscilloscope for 1000 samples at nominal voltage and T_0 conditions. The test setup and conditions are defined in Table 5.

Table 5: **Transmitter Near-End Output Eye Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	Nominal
Temperature	T_0
Pattern	PRBS15
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude	GTH attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 156.25 MHz for 10.3125 Gb/s • 173.4375 MHz for 11.1 Gb/s

Test Results

Figure 1 shows the transmitter near-end output eye at 10.3125 Gb/s. Figure 1 is provided as a representative diagram, and does not quantify device performance.

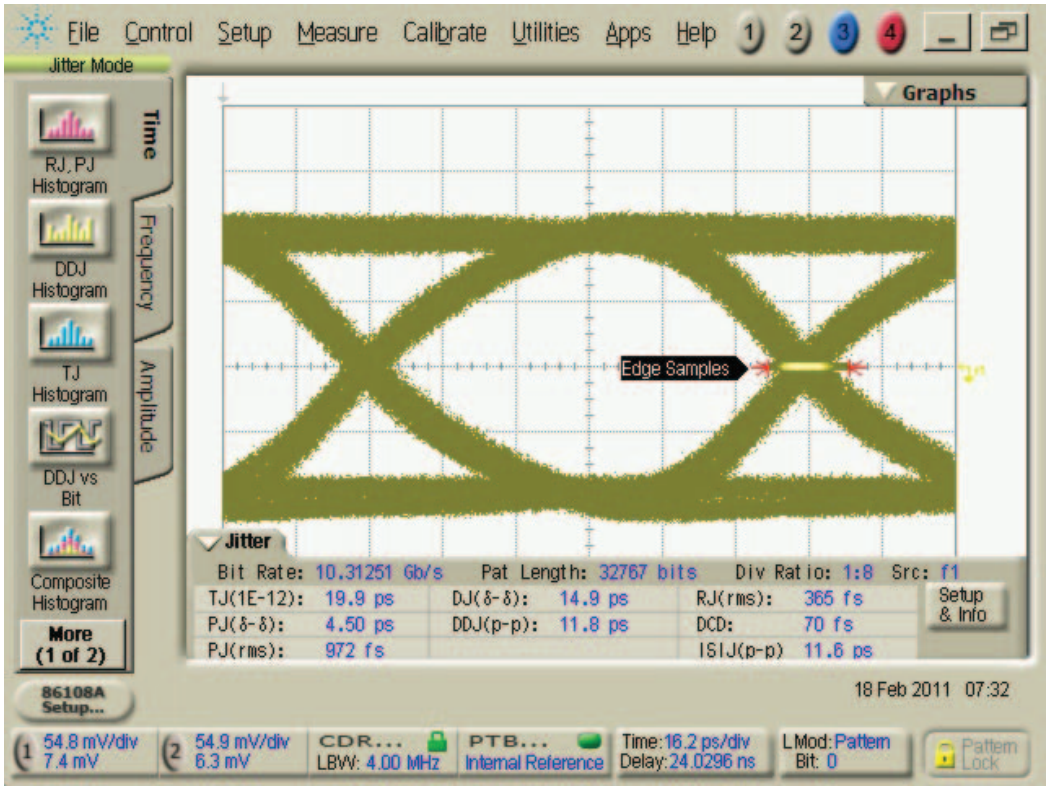

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Figure 1: **Transmitter Near-End Output Eye (10.3125 Gb/s with 156.25 MHz REFCLK)**

Figure 2 shows the transmitter near-end output eye at 11.1 Gb/s. Figure 2 is provided as a representative diagram, and does not quantify device performance.

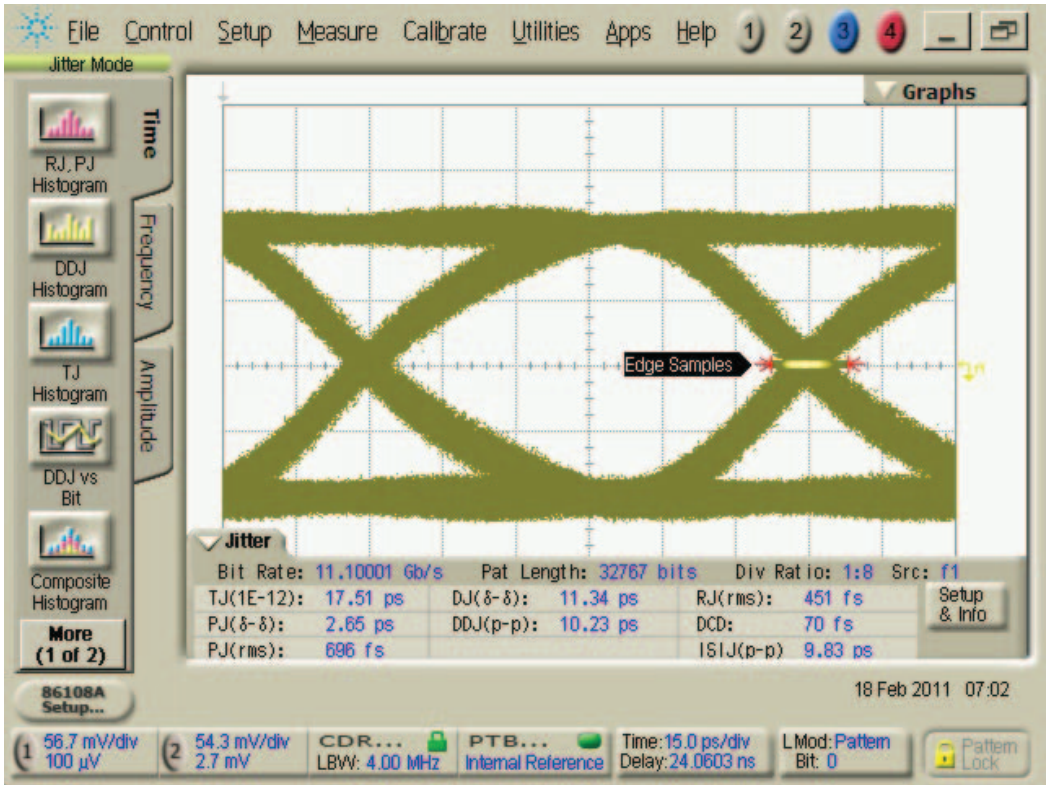

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Figure 2: **Transmitter Near-End Output Eye (11.1 Gb/s with 173.4375 MHz REFCLK)**

Transmitter Output Jitter

Test Methodology

Transmitter output jitter was measured using the bench setup shown in Figure 3. The DCA-J/DCA-X is used with the Agilent 86108A precision waveform analyzer to measure the output jitter. The Agilent 86108A contains a hardware clock recovery unit with adjustable loop bandwidth which is set to 4 MHz as required by the specifications.

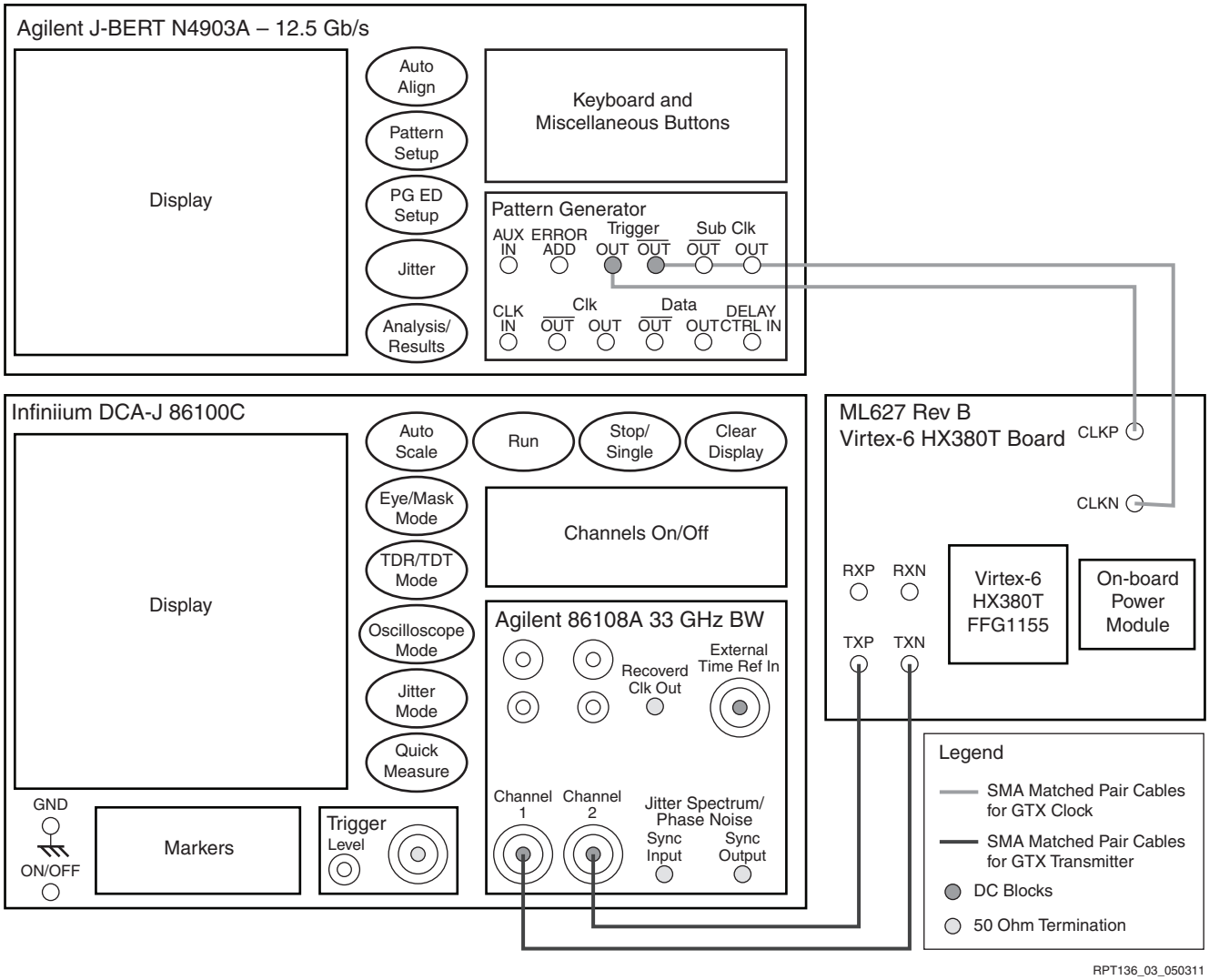

Figure 3: **Transmitter Output Jitter Test Setup Block Diagram**

The measurement is taken with ~3 to 4 inches of channel length between the TXP/TXN FPGA pins and the SMA connectors on the ML627 characterization platform.

Table 6 defines the test setup and conditions for the transmitter output jitter.

Table 6: **Transmitter Output Jitter Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J/DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	PRBS31
BER	10^{-12}
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude/ Emphasis	GTH Attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 156.25 MHz for 10.3125 Gb/s • 173.4375 MHz for 11.1 Gb/s

Test Results

Figure 4 shows the transmitter output jitter test results at 10.3125 Gb/s with a PRBS31 pattern and a BER of 10^{-12}.

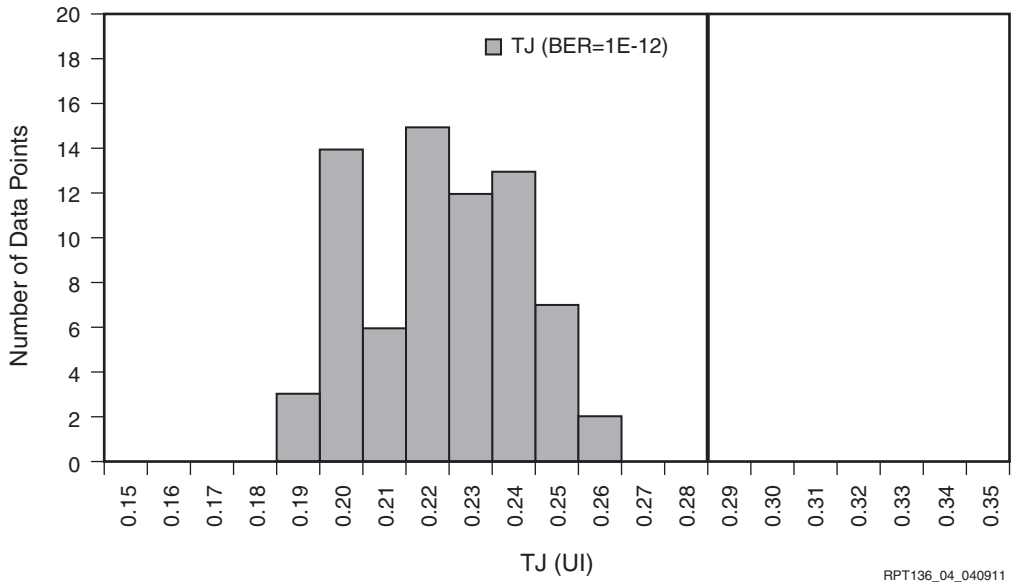

Figure 4: **Jitter Test Results for 10.3125 Gb/s**

Note for Figure 4:

1. 10.3125 Gb/s, PRBS31, BER = 10^{-12}.

Table 7 shows the maximum transmitter output jitter test result with PRBS patterns and a BER of 10^{-12}.

Table 7: **Transmitter Output Jitter Test Results for 10.3125 Gb/s**

Parameter	Pattern	BER	TJ (UI p-p)(1)	RJ (fs RMS)	DDJ (UI p-p)	DDPWS (UI p-p)	UJ (UI RMS)
Maximum Transmitter Output Jitter	PRBS31	10^{-12}	0.251	565	N/A	N/A	N/A
	PRBS9	10^{-12}	N/A	N/A	0.095	0.0285	0.0077

Notes:

1. Peak-to-peak.

Figure 5 shows the transmitter output jitter test results at 11.1 Gb/s with a PRBS31 pattern and a BER of 10^{-12}.

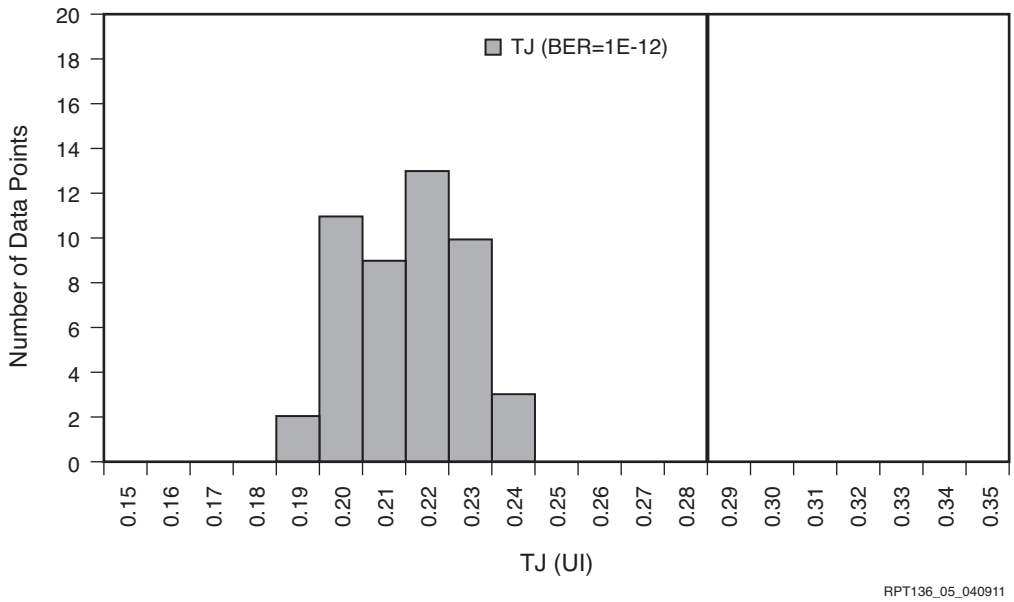

Figure 5: **Jitter Test Results for 11.1 Gb/s**

Note for Figure 5:

1. 11.1 Gb/s, PRBS31, BER = 10^{-12}.

Table 8 shows the maximum transmitter output jitter test result with PRBS patterns and a BER of 10^{-12}.

Table 8: **Transmitter Output Jitter Test Results for 11.1 Gb/s**

Parameter	Pattern	BER	TJ (UI p-p)(1)	RJ (fs RMS)	DDJ (UI p-p)	DDPWS (UI p-p)	UJ (UI RMS)
Maximum Transmitter Output Jitter	PRBS31	10^{-12}	0.234	516	N/A	N/A	N/A
	PRBS9	10^{-12}	N/A	N/A	0.0915	0.0146	0.0102

Notes:

1. Peak-to-peak.

Transmitter Output Differential Amplitudes

Test Methodology

SFF-8431 defines the transmitter output differential amplitude to be between 190 mV and 700 mV. The transmitter output differential amplitudes are measured using the same test setup as in Transmitter Output Jitter, page 11. Table 9 defines the test setup and conditions.

Table 9: **Output Differential Amplitude Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J/DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	Five 1s and five 0s clock pattern (`...11000001111100...`) generated internally in the fabric of the FPGA
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude/ Post-Emphasis	GTH attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 156.25 MHz for 10.3125 Gb/s • 173.4375 MHz for 11.1 Gb/s

Test Results

Transmitter output differential amplitude test results are shown in Table 10.

Table 10: **Transmitter Output Differential Amplitude Test Results**

Parameters	Min	Max	Units
Differential Amplitude at 10.3125 Gb/s	410	525	mV
Differential Amplitude at 11.1 Gb/s	404	515	mV

Transmitter Output Rise and Fall Times

Test Methodology

SFF-8431 defines the minimum transmitter output rise and fall times as 24 ps. Transmitter output rise and fall times are measured using the same test setup as in Transmitter Output Jitter, page 11. Table 11 defines the test setup and conditions.

Table 11: **Output Rise and Fall Time Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent 86100C DCA-J/DCA-X wideband oscilloscope with Agilent 86108A precision waveform analyzer plug-in module
TX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	Five 1s and five 0s clock pattern (`...11000001111100...`) generated internally in the fabric of the FPGA
Load Board	ML627 characterization platform, Revision B(FF1155)
TX Amplitude/ Post-Emphasis	GTH attributes: • TX_CFG0_LANE<n>[6:3] = `4'b0111` • TX_PREEMPH_LANE<n>[7:4] is set to `4'b1010` • TX_PREEMPH_LANE<n>[3:0] is set to `4'b0001`
REFCLK	Sourced from Agilent N4903A: • 156.25 MHz for 10.3125 Gb/s • 173.4375 MHz for 11.1 Gb/s

Test Results

The transmitter output rise and fall time test results are shown in Table 12.

Table 12: **Transmitter Output Rise and Fall Time Test Results**

Parameters	Rise Time (Min)	Fall Time (Min)	Units
Differential Amplitude at 10.3125 Gb/s	34.5	33.2	ps
Differential Amplitude at 11.1 Gb/s	33.9	33.0	ps

Transmitter Differential and Common Mode Output Return Loss

Test Methodology

SFF-8431 defines the differential output return loss measurement as –12 dB or better between 10 MHz and 2.8 GHz. The differential output return loss measurement between 2.8 GHz and 11.1 GHz is defined by the equation of $-8.15 + 13.33\log_{10}(f/5.5)$ where f is frequency in GHz. Differential return loss includes contributions from on-chip circuitry, chip packaging, and any off-chip components related to the driver. This output impedance requirement applies to all valid output levels. The reference impedance for differential return loss measurements is 100Ω.

The transmit common mode output return loss measurement is defined as –9 dB or better between 100 MHz and 4.74 GHz. The common mode output return loss measurement between 4.74 GHz and 11.1 GHz is defined by the equation of $-8.15 + 13.33\log_{10}(f/5.5)$, where f is frequency in GHz.

The vector network analyzer (VNA) interfaces to the host PC through the GPIB. After the measurement parameters are set, calibration begins. Four cables are included in the calibration process. VNA measurements are independent of voltage and are accurate up to 16 GHz. A digital multimeter (DVM) confirms the differential resistance is 100Ω before the measurement.

The measurement is taken with ~1 to 4 inches of channel length between the TXP/TXN FPGA pins and the SMA connectors on the ML627 characterization platform. Table 13 defines the test setup and conditions.

Table 13: **Differential and Common Mode Output Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES vector network analyzer
TX Coupling/Termination	Differential, DC coupled into 50Ω to GND
Voltage	Typical voltage
Temperature	Room temperature
Frequency Sweep	50 MHz to 16 GHz (10 MHz steps)
Load Board	ML627 characterization platform, Revision B(FF1155)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency (IF)	100 Hz

Figure 6 shows the setup for the return loss measurement.

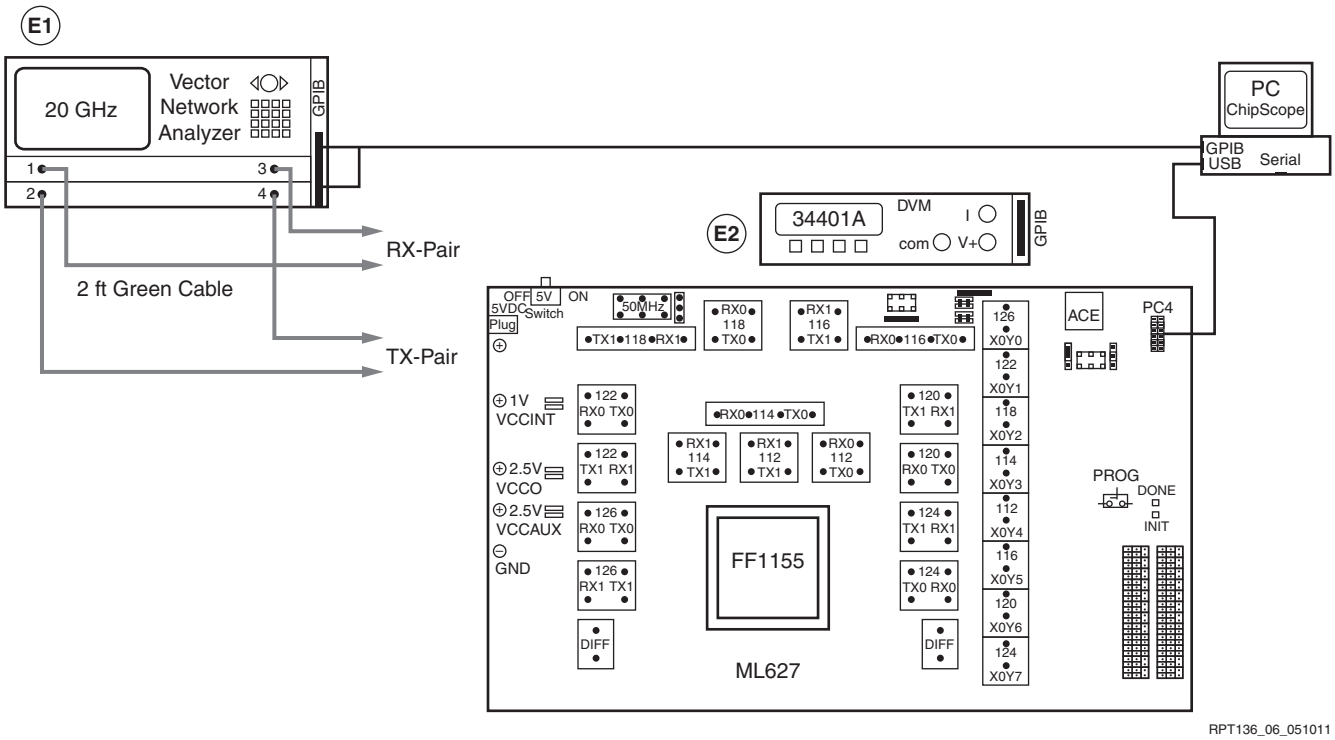

Figure 6: **Return Loss Test Setup Block Diagram**

Test Results

Figure 7 shows the transmitter differential output return loss measurement without de-embedding the channel.

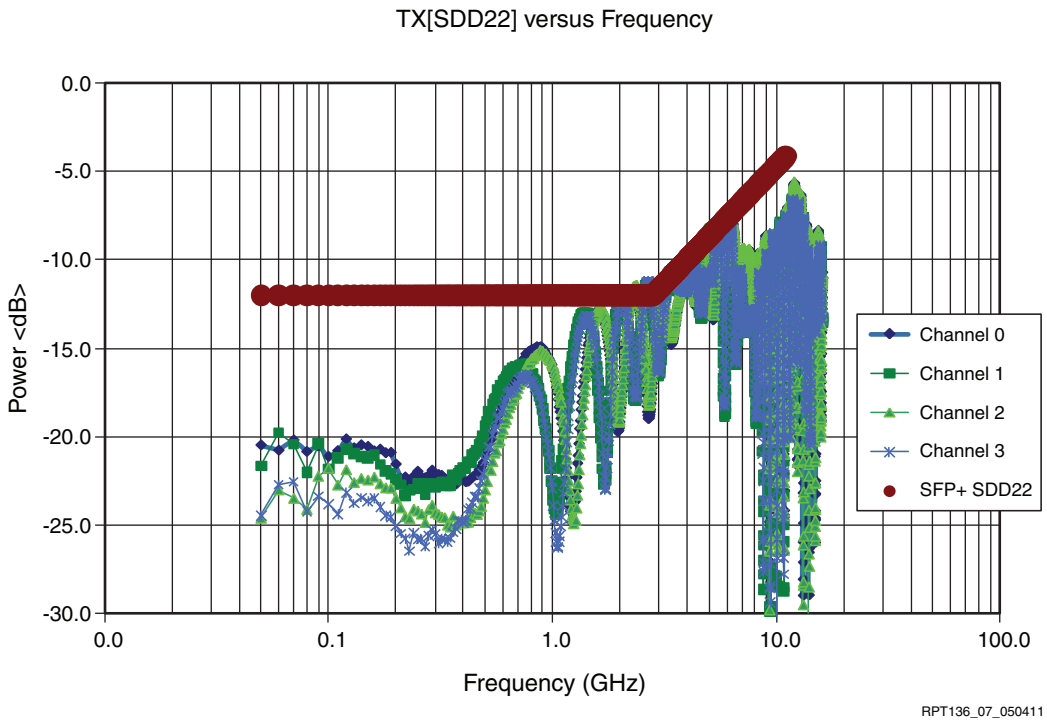

Figure 7: **Transmitter Differential Output Return Loss Measurement**

Figure 8 shows the transmitter common mode output return loss measurement without de-embedding the channel.

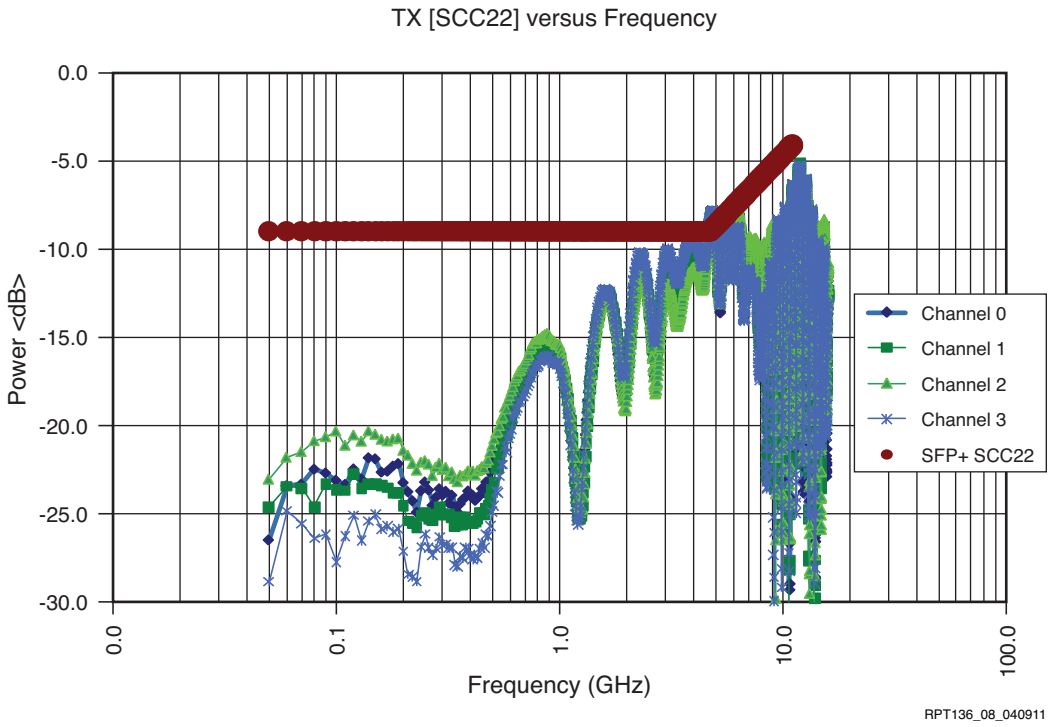

Figure 8: **Transmitter Common Mode Output Return Loss Measurement**

Receiver Input Jitter Tolerance

Test Methodology

Receiver input jitter tolerance is measured using the test setup shown in Figure 9. The J-BERT pattern generator generates a PRBS31 pattern. Random jitter (RJ) and bounded uncorrelated jitter (BUJ) are injected to meet the target value as per specification requirements for SFP+. DJ in the form of ISI is added with 10.75 x 13 inches of board trace (6.75 x 9 inches of which are from a BERTScope ISI test board). Sinusoidal jitter (SJ) is swept from 40 kHz to 40 MHz. The GTH transceiver under test recovers the data and transmits the pattern back to the error detector input of the J-BERT, where bit errors are measured. The test is performed with a +200 and –200 PPM offset between the J-BERT data generator and the reference clock provided to the GTH transceiver under test.

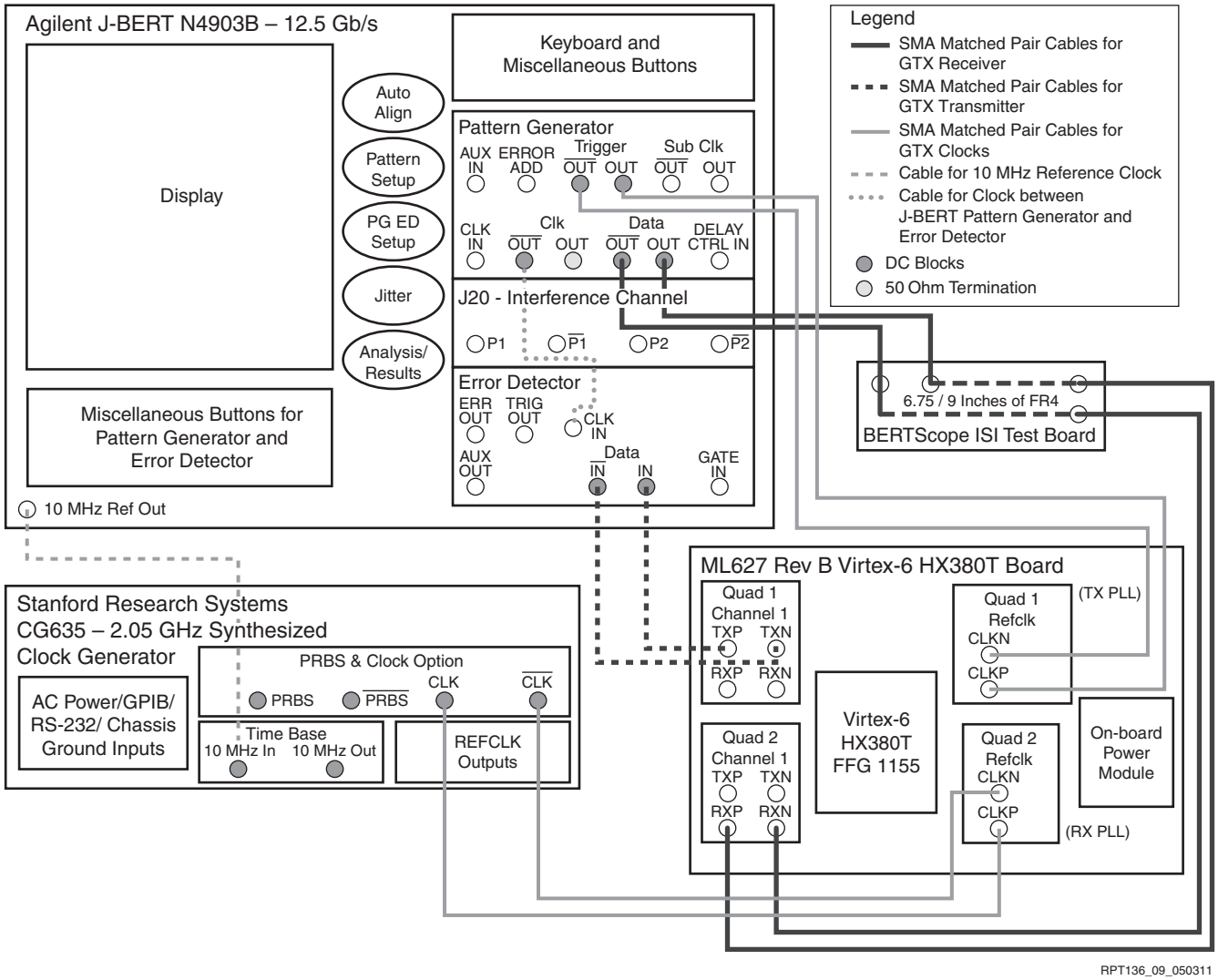

Figure 9: **Receiver Jitter Tolerance Setup Block Diagram**

Figure 10 shows a scope capture of the jitter injected to the GTH transceiver under test for 10.3125 Gb/s SFP+ testing. In addition to J2 and DDPWS, SJ is applied during the test.

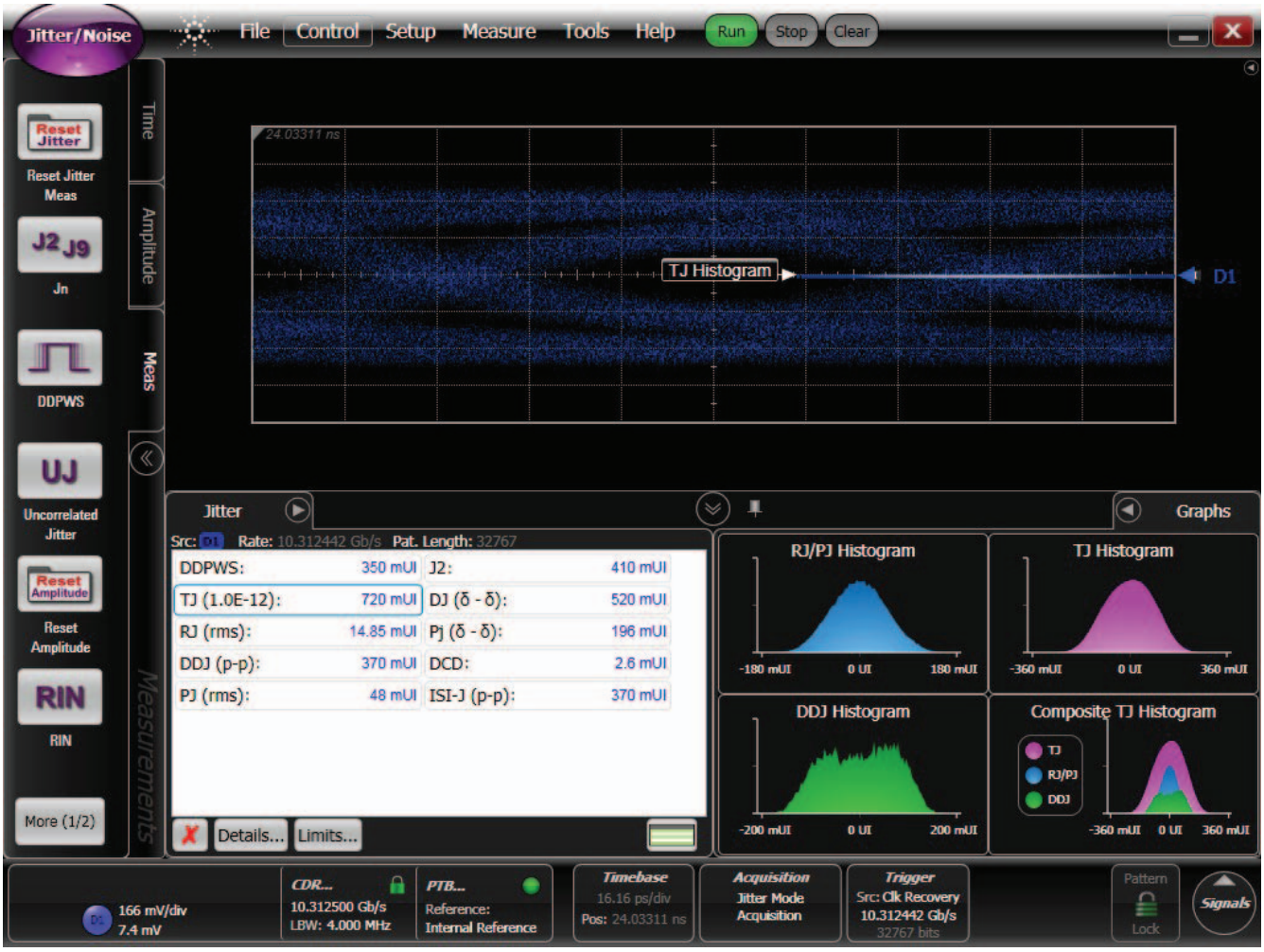

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Figure 10: **10.3125 Gb/s—Stressed Eye Jitter Tolerance Setup using PRBS15 Data Pattern**

Note for Figure 10:

1. PRBS31 is used for the actual measurement.

Figure 11 shows a scope capture of the stressed eye input to the GTH transceiver under test for 10.3125 Gb/s SFP+ testing.

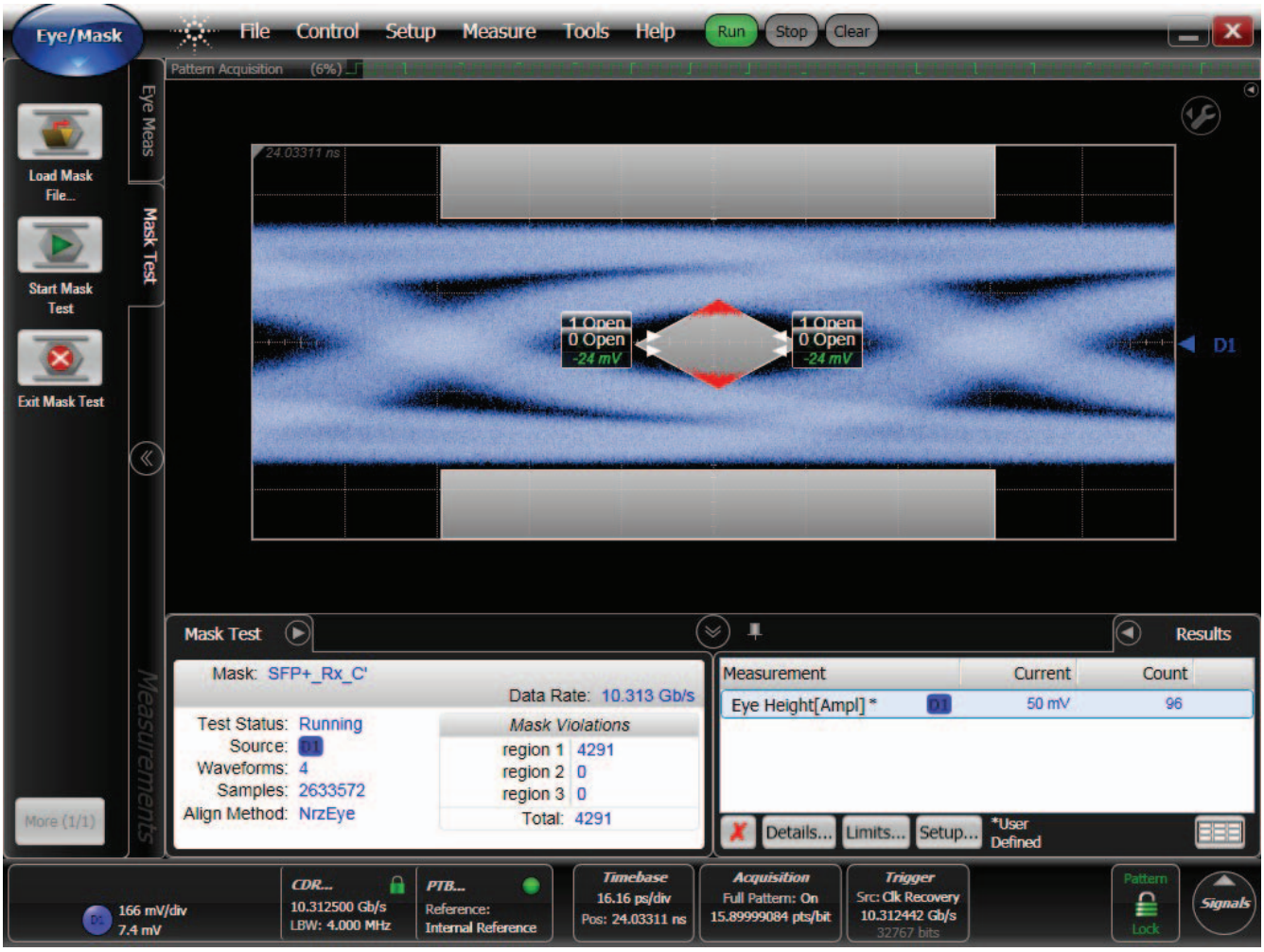

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Figure 11: **10.3125 Gb/s—Stressed Eye Jitter Tolerance with SFP+ Eye Mask Using PRBS15 Data Pattern**

Note for Figure 11:

1. PRBS31 is used for the actual measurement.

Figure 12 shows a scope capture of the jitter injected to the GTH transceiver under test for 11.1 Gb/s SFP+ testing. In addition to J2 and DDPWS, SJ is applied during the test.

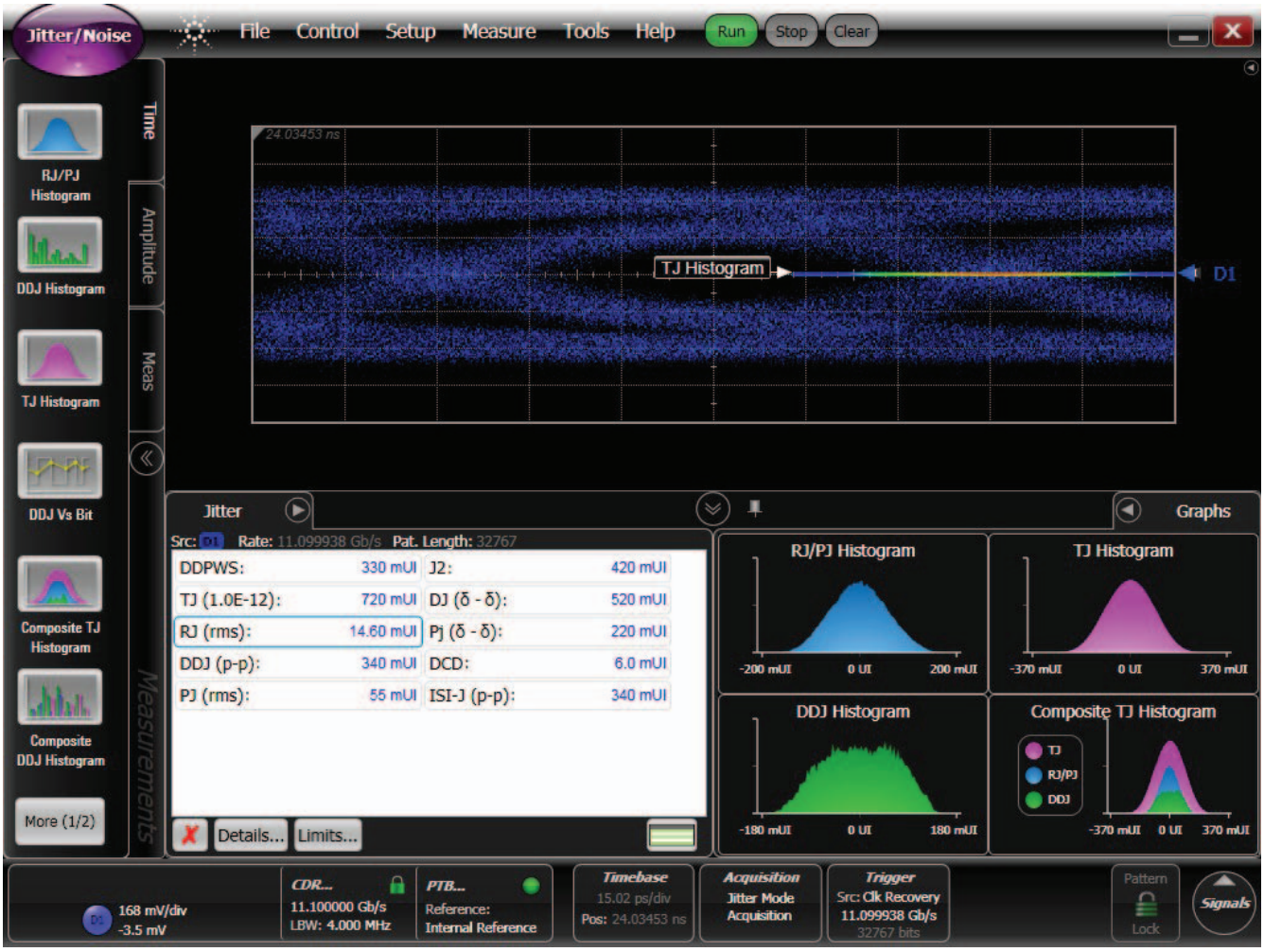

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Figure 12: **11.1 Gb/s—Stressed Eye Jitter Tolerance Setup using PRBS15 Data Pattern**

Note for Figure 12:

1. PRBS31 is used for the actual measurement.

Figure 13 shows a scope capture of the stressed eye input to the GTH transceiver under test for 11.1 Gb/s SFP+ testing.

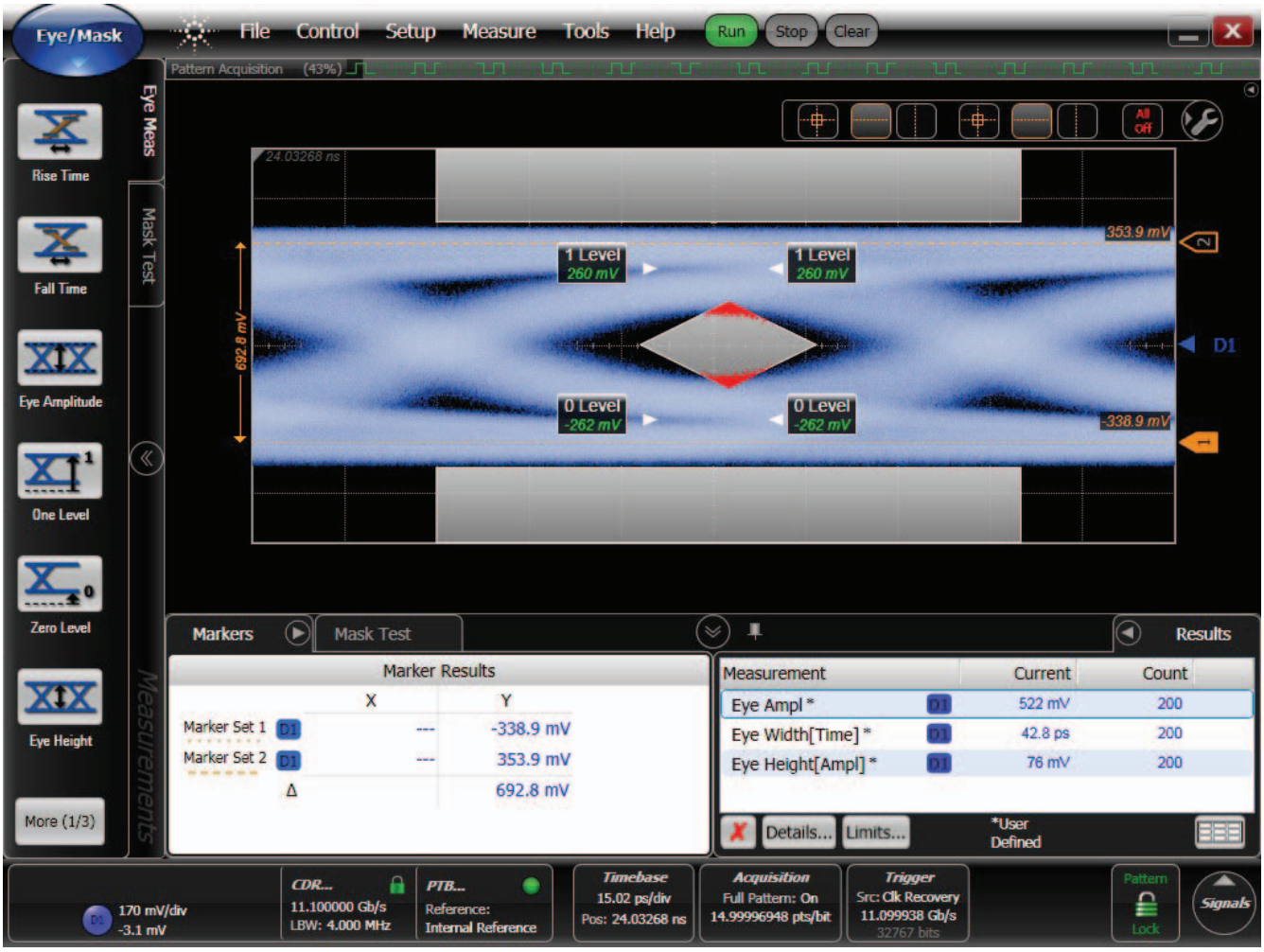

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Figure 13: **11.1 Gb/s - Stressed Eye Jitter Tolerance with SFP+ Eye Mask using PRBS15 Data Pattern**

Note for Figure 13:

1. PRBS31 is used for the actual measurement.

Table 14 defines the test setup and conditions for the receiver jitter tolerance.

Table 14: **Receiver Jitter Tolerance Test Setup and Conditions**

Parameter	Value
Measurement Instrument	Agilent J-BERT N4903B
RX Coupling	AC coupled using DC blocks
Voltage	V_{MIN}, V_{MAX}
Temperature	T_{-40}, T_0, T_{100}
Pattern	PRBS31

Table 14: **Receiver Jitter Tolerance Test Setup and Conditions *(Cont'd)***

Parameter	Value
Injected Jitter	SFP+ at 10.3125 Gb/s: • TJ = 0.720 UI (p-p)[1] • J2 = 0.410 UI (p-p) • DDPWS = 0.350 UI (p-p) • SJ = Tested to failure; Frequency sweep = {40 kHz–40 MHz} SFP+ at 11.1 Gb/s: • TJ = 0.720 UI (p-p) • J2 = 0.420 UI (p-p) • DDPWS = 0.330 UI (p-p) • SJ = Tested to failure; Frequency sweep = {40 kHz–40 MHz}
J-Bert Output Amplitude Setting	10.3125 Gb/s with 9 inches external FR4: • 960 mV (p-p differential) 11.1 Gb/s with 6.75 inches external FR4: • 960 mV (p-p differential)
BER	10^{-12} (measured at 10^{-9}, extrapolated to 10^{-12})
Load Board	ML627 characterization platform, Revision B(FF1155)
Attributes	GTH transceiver attributes for 10.3125 Gb/s:[2] • RX_CTLE_CTRL = `16'h00EF` • RX_AGC_CTRL = `16'h0000` • RX_AEQ_VAL0 = `16'h03C0` • RX_AEQ_VAL1 = `16'h0000` GTH transceiver attributes for 11.1 Gb/s:[3] • RX_CTLE_CTRL = `16'h00CF` • RX_AGC_CTRL = `16'h0000` • RX_AEQ_VAL0 = `16'h03C0` • RX_AEQ_VAL1 = `16'h0000`
REFCLK	Sourced from Agilent J-BERT N4903B: • 156.25 MHz for 10.3125 Gb/s • 173.4375 MHz for 11.1 Gb/s Sourced from CG635 Stanford Research synthesized clock generator: • 156.25 MHz ±200 ppm offset for 10.3125 Gb/s • 173.4375 MHz ±200 ppm offset for 11.1 Gb/s

Notes:

1. Peak-to-peak.
2. AGC is set in AUTO mode. DFE is set in AUTO mode. CTLE is set to a decimal value of 14.
3. AGC is set in AUTO mode. DFE is set in AUTO mode. CTLE is set to a decimal value of 12.

Test Results

Figure 14 shows the receiver jitter tolerance SJ sweep results for SFP+ at 10.3125 Gb/s. SJ is applied in addition to specified jitter components as defined in Table 14, page 24.

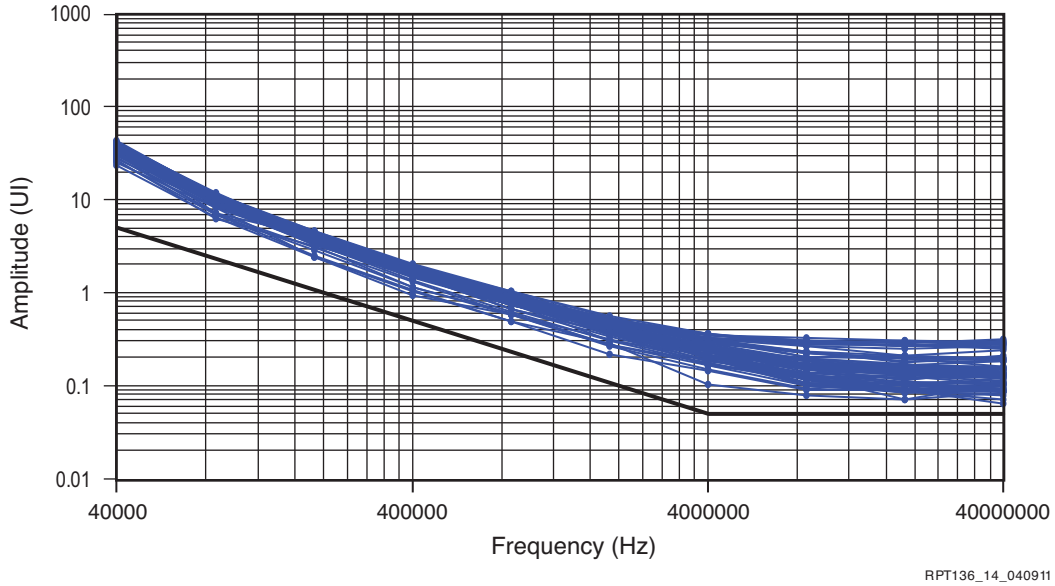

Figure 14: **Receiver Jitter Tolerance SJ Sweep Test Results at 10.3125 Gb/s**

Note for Figure 14:

1. PRBS31, BER = 10^{-12}.

Figure 15 shows the SJ tolerance at SJ frequency of 40 MHz for SFP+ at 10.3125 Gb/s. SJ is applied in addition to specified jitter components as defined in Table 14, page 24.

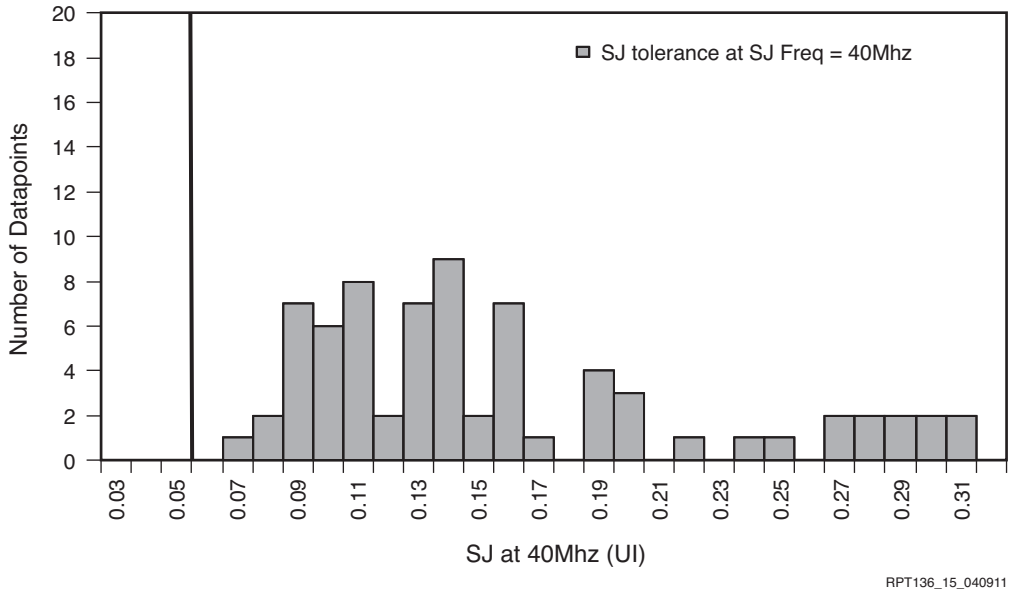

Figure 15: **Receiver Sinusoidal Jitter Tolerance at 40 MHz Test Results**

Note for Figure 15:

1. PRBS31, BER = 10^{-12}.

Table 15 shows the minimum receiver SJ tolerance at 40 MHz for SFP+. SJ is applied in addition to specified jitter components as defined in Table 14, page 24.

Table 15: **Receiver Jitter Tolerance Test Results**

Parameter	Test Condition	BER	Min SJ Tolerance	Units
Receiver Jitter Tolerance at 10.3125 Gb/s	SJ = 40 MHz	10^{-12}	0.064	UI

Figure 16 shows the receiver jitter tolerance SJ sweep results for SFP+ at 11.1 Gb/s. SJ is applied in addition to specified jitter components as defined in Table 14, page 24.

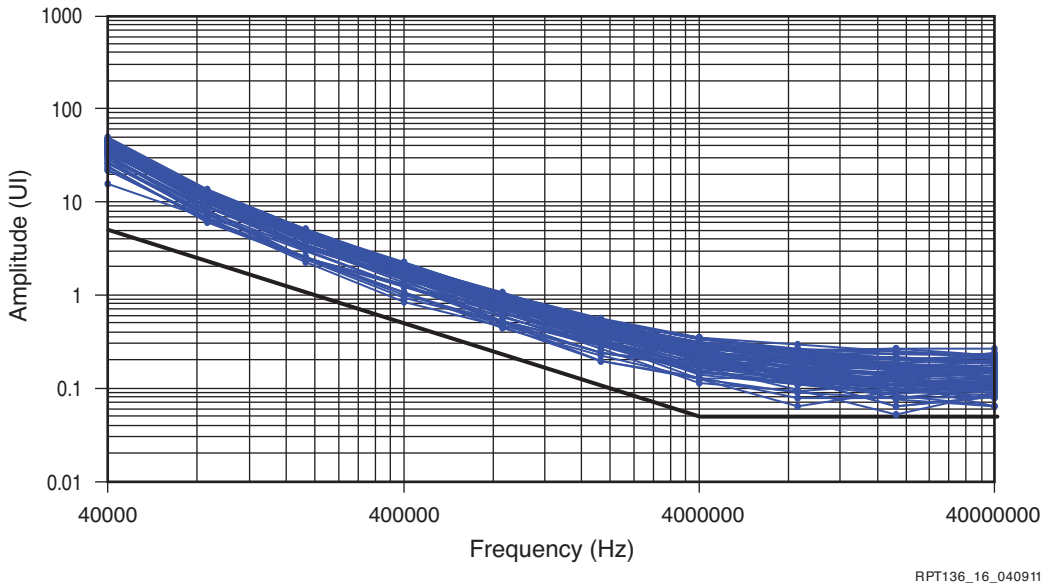

Figure 16: **SJ Sweep Test Results at 11.1 Gb/s**

Note for Figure 16:

1. PRBS31, BER = 10^{-12}.

Figure 17 shows the SJ at 40 MHz for SFP+ at 11.1 Gb/s. SJ is applied in addition to specified jitter components as defined in Table 14, page 24.

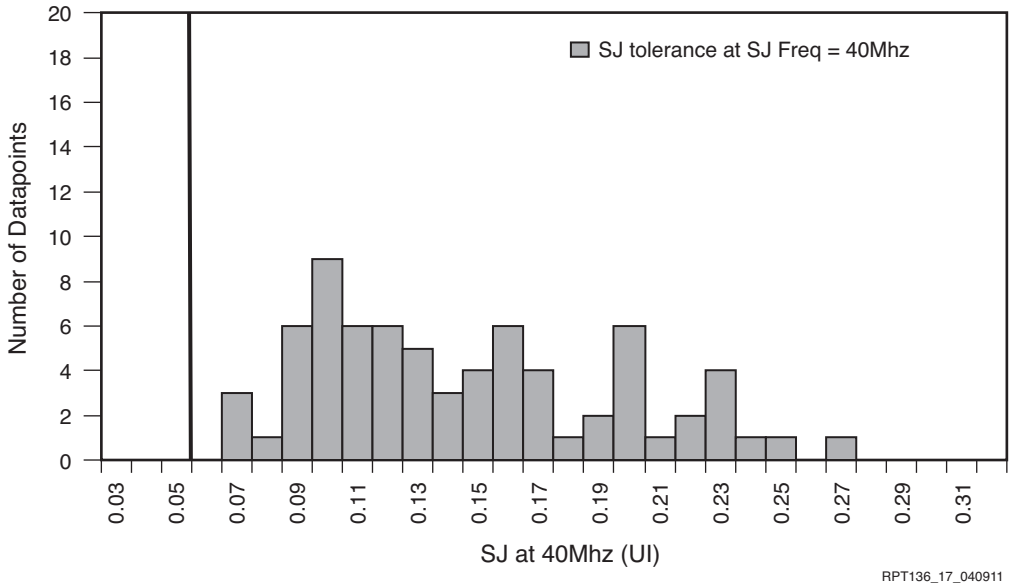

Figure 17: **Receiver Sinusoidal Jitter Tolerance at 40 MHz Test Results**

Note for Figure 17:

1. PRBS31, BER = 10^{-12}.

Table 16 shows the minimum receiver SJ tolerance for 40 MHz for SFP+. SJ is applied in addition to specified jitter components as defined in Table 15, page 27.

Table 16: **Receiver Jitter Tolerance Test Results**

Parameter	Test Condition	BER	Min SJ Tolerance	Units
Receiver Jitter Tolerance at 11.1 Gb/s	SJ = 40 MHz	10^{-12}	0.064	UI

Receiver Differential and Common Mode Input Return Loss

Test Methodology

Receiver input differential and common mode return loss specification and setup are the same as in Transmitter Differential and Common Mode Output Return Loss, page 16. The measurement is taken with ~1 to 4 inches of channel length between the RXP/RXN FPGA pins and the SMA connectors on the ML627 characterization platform. Table 17 defines the test setup and conditions.

Table 17: **Receiver Differential and Common Mode Input Return Loss Test Setup and Conditions**

Parameter	Value
Measurement Instrument	HP8720ES vector network analyzer
RX Configuration/Amplitude	RX is configured for 100Ω differential termination (center tap to GND), and AC coupled using both internal and external capacitors.
Voltage	Typical voltage
Temperature	Room temperature
Frequency Sweep	50 MHz to 16 GHz (10 MHz steps)
Test Fixture	ML627 characterization platform, Revision B(FF1155)
REFCLK	Not available
Source Power	0 dBm
Averaging Calibration	1
Intermediate Frequency (IF)	100 Hz

Test Results

Figure 18 shows the receiver differential input return loss measurement without de-embedding of the channel.

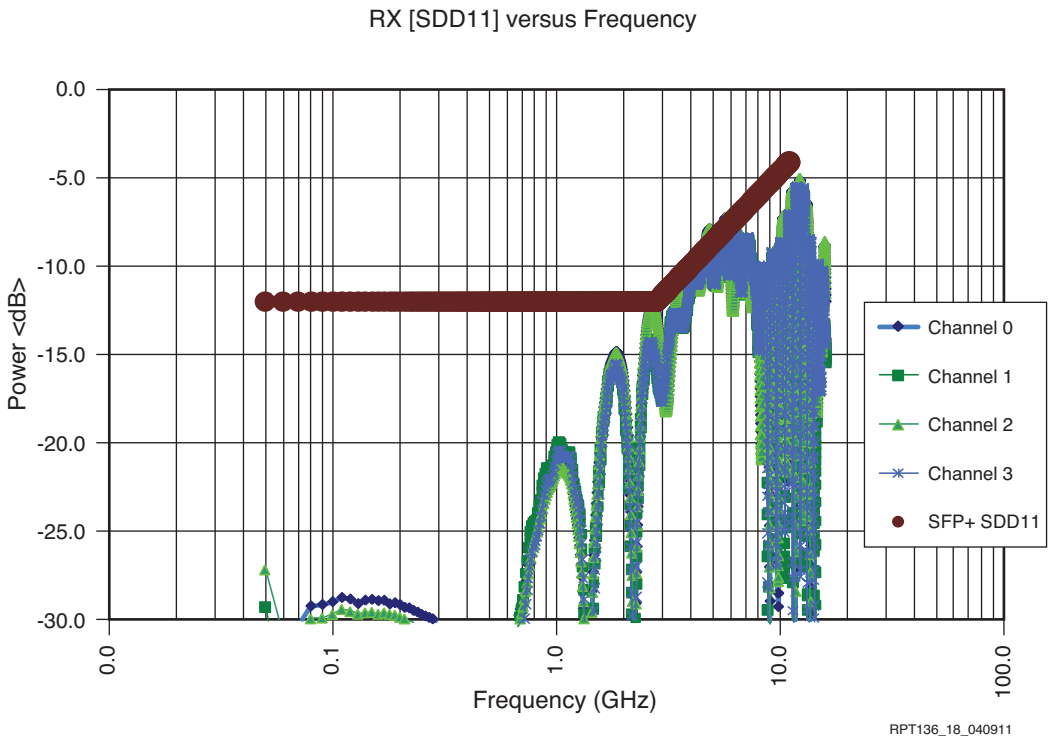

Figure 18: **Receiver Differential Input Return Loss Measurement**

Figure 19 shows the receiver common mode input return loss measurement without de-embedding of the channel.

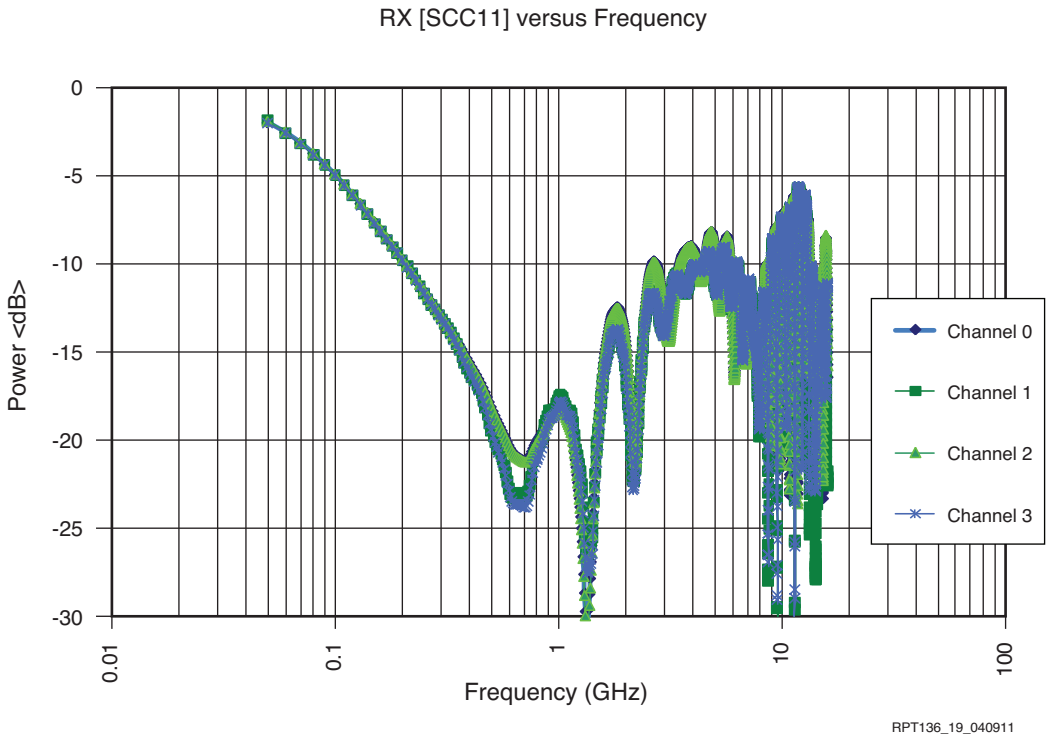

Figure 19: **Receiver Common Mode Input Return Loss Measurement**