<table>
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<th>Notes:</th>
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<tr>
<td>1. 2LE ($T_j = 0°C$ to $110°C$). For more details, see the Ordering Information section in DS890, UltraScale Architecture and Product Overview.</td>
</tr>
<tr>
<td>2. Maximum achievable performance is device and package dependent; consult the associated data sheet for details.</td>
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<tr>
<td>3. For full part number details, see the Ordering Information section in DS890, UltraScale Architecture and Product Overview.</td>
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<tr>
<td>4. GTY transceiver line rates are package limited: B784 to 12.5 Gb/s; A676, D900, and A1156 to 16.3 Gb/s. Refer to data sheet for details.</td>
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<tr>
<td>5. The B784 package is only offered in 0.8mm ball pitch. All other packages are 1.0mm ball pitch.</td>
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<table>
<thead>
<tr>
<th>Device Name</th>
<th>KU3P</th>
<th>KU5P</th>
<th>KU9P</th>
<th>KU11P</th>
<th>KU13P</th>
<th>KU15P</th>
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<tr>
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<th>Dimensions (mm)</th>
<th>HD I/O, HP I/O, GTH 16.3Gb/s, GTY 32.75Gb/s</th>
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<td>23x23$^{(5)}$</td>
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<td>A676$^{(4)}$</td>
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<td>100G Ethernet w/ KR4 RS-FC</td>
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<td>Max. Single-Ended HP I/Os</td>
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<td>GTY 32.75Gb/s Transceivers</td>
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<td>GTM 58Gb/s PAM4 Transceivers</td>
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<td>Dim. (mm)</td>
<td>HP I/O, GTY</td>
<td>HP I/O, GTY, GTM</td>
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</tbody>
</table>

1. A CCIX port requires the use of a PCIe Gen3 x16 / Gen4 x8 block.
2. -2LE (Tj = 0°C to 110°C). See Ordering Information in DS890.
3. For full part number details, see DS890, UltraScale Architecture and Product Overview.
4. All packages are 1.0mm ball pitch.
6. The GTY transceiver line rate in the F1924 footprint is package limited to 16.3Gb/s. Refer to data sheet for details.
7. These 52.5x52.5mm packages have the same PCB ball footprint as the 47.5x47.5mm packages and are footprint compatible.

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UltraScale and UltraScale+ families provide footprint compatibility to enable users to migrate designs from one device or family to another. Any two packages with the same footprint identifier code are footprint compatible.

### UltraScale Architecture Migration Table

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<tr>
<th>Footprint</th>
<th>Kintex® UltraScale™</th>
<th>Kintex UltraScale+™</th>
<th>Virtex® UltraScale</th>
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**Legend**

- **Device**
- **Migration Path**

**Notes:**

1. The body size of the VU13P device in the A2104, B2104, C2104, and D2104 packages is 52.5mm. These packages are footprint compatible with the corresponding 47.5mm body size packages. See [UG583, UltraScale Architecture PCB Design User Guide](https://www.xilinx.com) for important migration details.

2. Virtex UltraScale+ HBM devices migrate among each other but do not migrate to other devices.
# Kintex® UltraScale+™ FPGA Speed Grades

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Notes:
1. For full part number details, see the Ordering Information section in [DS890](https://www.xilinx.com), UltraScale Architecture and Product Overview.
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in [DS890](https://www.xilinx.com), UltraScale Architecture and Product Overview.

- •: available
- -: not offered
# Virtex® UltraScale+™ FPGA Speed Grades

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Notes:
1. For full part number details, see the Ordering Information section in [DS890, UltraScale Architecture and Product Overview](#).
2. -2LE (Tj = 0°C to 110°C). For more details, see the Ordering Information section in [DS890, UltraScale Architecture and Product Overview](#).

- ● : available
- - : not offered
### UltraScale+ Device Ordering Information

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<td>UltraScale</td>
<td>Value Index</td>
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<td>F: Lid</td>
<td>V: RoHS 6/6</td>
<td>Package Designator</td>
<td>Package Pin Count</td>
<td>Temperature Grade</td>
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<td>-1 = Slowest</td>
<td>L1 = Low Power</td>
<td>-2 = Mid</td>
<td>-L2 = Low Power</td>
<td>-3 = Fastest</td>
<td>(1.0mm)</td>
<td>L: Lid SSI</td>
<td>B: Lidless</td>
<td>G: RoHS 6/6 w/ Exemption 15</td>
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</tr>
<tr>
<td>E = Extended (Tj = 0°C to +100°C)</td>
<td>I: Overhang SSI</td>
<td>H: Overhang SSI Stiffener</td>
<td>I: Overhang Lidless Stiffener</td>
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</table>

#### Important:
- Verify all data in this document with the device data sheets found at [www.xilinx.com](http://www.xilinx.com).
- For valid part/package combinations, go to [DS890, UltraScale Architecture and Product Overview: Device-Package Combinations and Maximum I/Os Tables](http://www.xilinx.com).
- Denotes UltraScale+ Device.

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References

DS890, *UltraScale™ Architecture and Product Overview*

DS922, *Kintex® UltraScale+™ FPGAs Data Sheet: DC and AC Switching Characteristics*

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UG570, *UltraScale Architecture Configuration User Guide*

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