Versal™ ACAP
AI Core Series
Product Selection Guide

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Industry's First Adaptive Compute Acceleration Platform (ACAP)

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Versal™ AI Core Series – Resources

			VC1352	VC1502	VC1702	VC1802	VC1902
Intelligent Engines	AI Engines		128	248	320	300	400
	AI Engine Data Memory Blocks (#)		1024	1984	2560	2400	3200
	AI Engine Data Memory (Mb)		32	62	80	75	100
	DSP Engines		928	1,312	1,696	1,600	1,968
Adaptable Engines	System Logic Cells (K)		540	797	1,051	1,586	1,968
	LUTs		246,784	364,544	480,256	725,000	899,840
	Distributed RAM (Mb)		8	11	15	22	27
Memory	Total Block RAM (Mb)		16	19	29	28	34
	UltraRAM (Mb)		59	60	113	91	130
	Accelerator RAM (Mb)		32	0	32	0	0
	Total SRAM Capacity (Mb)		115	90	189	141	191
Scalar Engines	Application Processing Unit		Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC				
	Real-time Processing Unit		Dual-core Arm Cortex-R5, 32KB/32KB L1 Cache, and 256KB TCM w/ECC				
	Memory		256KB On-Chip Memory w/ECC				
	Connectivity		Ethernet (x2); UART (x2); CAN-FD (x2); USB 2.0 (x1); SPI (x2); I2C (x2)				
Foundational Platform	NoC Master / NoC Slave Ports		10	14	18	28	28
	DDR Bus Width		128	128	128	256	256
	DDR Memory Controllers		2	2	2	4	4
	CCIX & PCIe® w/DMA (CPM)		–	1 x Gen4x16, CCIX	–	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX
	PCI Express®		1 x Gen4x8	4 x Gen4x8	1 x Gen4x8	4 x Gen4x8	4 x Gen4x8
	100G Multirate Ethernet MAC		1	4	3	4	4
	SD-FEC		2	0	5	0	0
	Platform Management Controller		Boot, Security, Safety, Monitoring, and High Speed Debug				
Package Footprint	Package Dimensions (mm)	Ball Pitch (mm)	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY	XPIO, HDIO, MIO, GTY
A1024	31x31	0.92	378, 22, 78, 8	378, 22, 78, 8			
E1369	35x35	0.92	378, 44, 78, 8		378, 44, 78, 24		
G1369	35x35	0.92		378, 44, 78, 24			
A1596	37.5x37.5(2)	0.92		378, 44, 78, 32	378, 44, 78, 16	378, 44, 78, 32	378, 44, 78, 32
D1760	40x40	0.92				648, 0, 78, 24	648, 0, 78, 24
A2197	45x45	0.92		378, 44, 78, 44		648, 44, 78, 44	648, 44, 78, 44

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Notes:
1. GTY transceivers operate at data rates up to 32.75Gb/s
2. VSVA1596 package dimensions are 37.5x37.5mm, VIVA1596 package dimensions are 40x40mm

All parameters listed are maximum values. Verify all data in this document with the device data sheets or product guides found at: www.xilinx.com.
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Versal™ AI Core Series – Figures of Merit

			VC1352	VC1502	VC1702	VC1802	VC1902
Intelligent Engines	AI Engine Peak Perf – INT8	TOPs	43	83	106	100	133
	AI Engine Peak Perf – INT8x16	TOPs	21	41	53	50	67
	AI Engine Peak Perf – INT16	TOPs	11	21	27	25	33
	AI Engine Peak Perf – CINT16	Complex TOPs	3	5	7	6	8
	AI Engine Peak Perf – FP32	TFLOPs	3	5	7	6	8
	AI Engine Peak SRAM Bandwidth	Tb/s	170	330	426	399	532
	DSP Engine Peak Perf – INT8	TOPs	6.4	9.1	11.7	11.0	13.6
	DSP Engine Peak Perf – INT24	TOPs	2.1	3.0	3.9	3.7	4.5
	DSP Engine Peak Perf – CINT18	Complex TOPs	0.9	1.3	1.7	1.6	1.9
	DSP Engine Peak Perf – FP32	TFLOPs	1.5	2.1	2.7	2.6	3.2
Adaptable Engines	Adaptable Engine Peak Perf – INT1	TOPs	258	381	502	758	941
	Adaptable Engine Peak Perf – INT2	TOPs	118	175	230	347	431
	Adaptable Engine Peak Perf – INT4	TOPs	31	45	60	90	112
	Adaptable Engine Peak Perf – INT8	TOPs	8	12	15	23	29
Scalar Engines	Arm® Cortex-A72 Performance	DMIPs	15,980	15,980	15,980	15,980	15,980
	Arm Cortex-R5 Performance	DMIPs	2,505	2,505	2,505	2,505	2,505
Memory	Total Bandwidth - Block RAM	Tb/s	64	79	119	115	139
	Total Bandwidth - Ultra RAM	Tb/s	22	23	43	35	49
	Total Bandwidth - Accelerator RAM	Tb/s	0.4	0.0	0.4	0.0	0.0
	Total SRAM Bandwidth	Tb/s	86	102	162	150	188
I/O	Transceiver Bandwidth	Tb/s	0.26	1.44	0.79	1.44	1.44
	Sensor I/O Bandwidth	Gb/s	0	691	0	0	1,478
Platform Engines	DDR4 Memory Bandwidth	GB/s	51.2	51.2	51.2	102.4	102.4
	LPDDR4 Memory Bandwidth	GB/s	68.3	68.3	68.3	136.5	136.5
	NoC Cross-sectional Bandwidth	Tb/s	1.2	1.2	1.2	2.5	2.5

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Versal™ ACAP Ordering Information

Device Name				Device Attributes				Footprint			
XC	V	M	1802	-1	M	S	E	V	F	V	XXX
Xilinx XC: Commercial XA: Automotive XQ: Defense	**Architecture** Versal	**Series Name** **C**: AI Core **M**: Prime	**Device Number** Digits 1-3: Value Identifier Digit 4: # of Primary Cores	**Speed Grade** -1: Slowest -2: Mid -3: Highest	**Voltage** L: Low (0.7V) M: Mid (0.80V) H: High (0.88V) D: Low and Mid G: Mid and High	**Static Screen** S: Standard L: Low Static	**Temp Grade** E: 0 to 110°C(1) I: –40 to 110°C(1)	**Ball Pitch** V: 0.92mm S: 0.8mm L: 1.0mm	**Lid** S: Stiffener Ring F: Forged (Lidded) B: Bare Die H: Lidded Overhang I: Stiffener Ring Overhang	**RoHS6 Code** G: Eutectic Bump V: Pb-free Bump	**Package Pin Count**

Note:
1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).

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