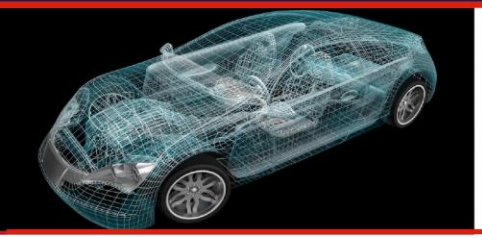
XA Automotive Portfolio
Product Selection Guide



SPARTAN ARTIX KINTEX ZYNQ

XILINX

All Programmable Automotive SoC Comparison

	XA Zynq UltraScale+™ MPSoC ZU2/3EG, ZU4/5EV Devices	XA Zynq®-7000 SoC Z-7010/7020/7030 Devices
Application Processor	**Quad**-core Arm® Cortex®-A53 MPCore™ up to **1.2GHz**	**Dual**-core Arm Cortex-A9 MPCore up to **667MHz**
Real-Time Processor	Dual-core Arm Cortex-R5 MPCore up to **500MHz**	N/A
Graphics Processor	Mali™-400 MP2 up to 600MHz	N/A
External Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC	x16/x32: DDR3L, DDR3, DDR2, LPDDR2 w/ECC (supports 16-bit)
Programmable Logic	103K–256K System Logic Cells	28K–125K Logic Cells
DSP Slices	240–1,248	80–400
Speed Grades	-1, -1L	-1
Automotive Standards	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process
Power Management	Separate Voltage on PS & PL, Full (PL+PS) / Full power domain / Low power domain / Battery Power Domains (PS)	Full (PS +PL), Separate Voltage on PS & PL

All Programmable Automotive FPGA Comparison

	XA Artix®-7	XA Kintex®-7	XA Spartan®-7	XA Spartan-6
Core Voltage	1.0V	1.0V	1.0V	1.2V
Logic Cell	12K–101K	162K	6K–102K	3K–74K
Total Block RAM (K)	720–4,860	2,188	180–4,320	216–3,096
CMTs	3–6	8	2–8	2–6
DSP Slices	40–240	600	10–160	8–132
PCIe®	1 @ Gen2 up to x4	1 @ Gen2 up to x 8	0	0–1 @ Gen1 x1
Serial Transceivers	2–4	8	0	0–4
Speed Grades	-1, -2	-1	-1, -2	-2, -3
Automotive Standards	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process	AEC-Q100, Production Part Approval Process

XA Zynq® UltraScale+™ MPSoCs

		Device Name[1]	ZU2EG	ZU3EG	ZU4EV	ZU5EV
Processing System (PS)	Application Processor Unit	Processor Core	**Quad-core** Arm® Cortex®-A53 MPCore™ up to 1.2GHz			
		Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB			
	Real-Time Processor Unit	Processor Core	**Dual-core** Arm Cortex-R5 MPCore up to 500MHz			
		Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core			
	Graphic & Video Acceleration	Graphics Processing Unit	Mali™-400 MP2 up to 600MHz			
		Memory	L2 Cache 64KB			
	External Memory	Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC			
		Static Memory Interfaces	NAND, 2x Quad-SPI			
	Connectivity	High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet			
		General Connectivity	2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO			
	Integrated Block Functionality	Power Management	Full / Low / PL / Battery Power Domains			
		Security	RSA, AES, and SHA			
		AMS - System Monitor	10-bit, 1MSPS - Temperature, Voltage, and Current Monitor			
PS to PL Interface			12 x 32/64/128b AXI Ports			
Programmable Logic (PL)	Programmable Functionality	System Logic Cells (K)	103	154	192	256
		CLB Flip-Flops (K)	94	141	176	234
		CLB LUTs (K)	47	71	88	117
	Memory	Max. Distributed RAM (Mb)	1.2	1.8	2.6	3.5
		Total Block RAM (Mb)	5.3	7.6	4.5	5.1
		UltraRAM (Mb)	-	-	14.0	18.0
	Clocking	Clock Management Tiles (CMTs)	3	3	4	4
	Integrated IP	DSP Slices	240	360	728	1,248
		VCU	-	-	1	1
		PCI Express Gen 3x16 / Gen4x8	-	-	2	2
		150G Interlaken	-	-	-	-
		100G Ethernet MAC/PCS w/RS-FEC	-	-	-	-
		AMS - System Monitor	1	1	1	1
	Transceivers	GTH 12.5Gb/s Transceivers	-	-	16	16
	Speed Grades	I-Grade	-1 (0.85V), -L1 (0.72V)			
		Q-Grade	-1 (0.85V)			

Notes:
1. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.

XA Zynq® UltraScale+™ MPSoCs

PS I/Os(1), 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os
PS-GTR 6Gb/s, GTH 12.5Gb/s

Pkg Footprint(2)	Dimensions (mm)	XAZU2EG	XAZU3EG	XAZU4EV	XAZU5EV
SBVA484(3)	19x19	170, 24, 58 4, 0	170, 24, 58 4, 0		
SFVA625(3)	21x21	170, 24, 156 4, 0	170, 24, 156 4, 0		
SFVC784(3)	23x23	214, 96, 156 4, 0	214, 96, 156 4, 0	214, 96, 156 4, 4	214, 96, 156 4, 4

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. For full part number details, see the Ordering Information section in DS891, *Zynq UltraScale+ MPSoC Overview*.
3. These packages are only offered in 0.8mm ballpitch.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

XA Zynq®-7000 SoCs

		Device Name[1]	XA7Z010	XA7Z020	XA7Z030
Processing System (PS)	Application Processor Unit	Processor Core	**Dual** Arm® Cortex®-A9 MPCore™ up to 667MHz		
		Processor Extension	NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per Processor		
	Memory	L1 Cache	32KB I / D per Core		
		L2 Cache	512KB		
		On-Chip Memory	256KB		
	External Memory	Dynamic Memory Interface	x32/x64: DDR3, DDR3L, DDR2, LPDDR2		
		Static Memory Interfaces	NAND, NOR, 2x Quad-SPI		
	Connectivity	High-Speed Connectivity	2x Tri-mode Gigabit Ethernet		
		General Connectivity	2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO		
	Integrated Block Functionality	Security	RSA, AES, and SHA		
		AMS - System Monitor	2x12-bit, 1MSPS - Temperature, Voltage, and Current Monitor		
PS to PL Interface			9 x 32/64 AXI Ports		
Programmable Logic (PL)	Programmable Functionality	Xilinx 7 Series PL Equivalent	Artix-7	Artix-7	Kintex-7
		Logic Cells	28,160	85,280	125,760
		CLB Flip-Flops	35,300	106,400	157,200
		CLB LUTs	17,600	53,300	78,600
	Memory	Total Block RAM (KB) (# 36 Kb Blocks)	240 (60)	560 (140)	1,060 (265)
	Integrated IP	DSP Slices	80	220	400
		Peak DSP Performance	100 GMACs	276 GMACs	593 GMACs
		PCI Express	-	-	Gen2 x4
		AMS / XADC	AES and SHA 256b Decryption and Authentication for Secure Programmable Configuration		
	Speed Grades	I-Grade	-1		
		Q-Grade	-1		
	Package[1]	Size (mm) / Pitch (mm)	HR I/O[2], HP I/O[3], PS I/O[4], GTX Transceiver		
Package	CLG225	13x13 / 0.8	54, 0, 84, 0		
	CLG400	17x17 / 0.8	100, 0, 128, 0	125, 0, 128, 0	
	CLG484	19x19 / 0.8		200, 0, 128, 0	
	FBV484	23x23 / 1.0			100, 63, 128, 4

Notes:
1. All packages listed are Pb-free.
2. HR = High Range I/O with support for I/O voltage from 1.2V up to 3.3V.
3. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.
4. PS I/O includes user I/O and DDR I/O.

XA Artix®-7 FPGAs

		Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)						
	Part Number	XA7A12T	XA7A15T	XA7A25T	XA7A35T	XA7A50T	XA7A75T	XA7A100T
Logic Resources	Logic Cells	12,800	16,640	23,360	33,280	52,160	75,520	101,440
	Slices	2,000	2,600	3,650	5,200	8,150	11,800	15,850
	CLB Flip-Flops	16,000	20,800	29,200	41,600	65,200	94,400	126,800
Memory Resources	Maximum Distributed RAM (Kb)	171	200	313	400	600	892	1,188
	Block RAM/FIFO w/ ECC (36 Kb each)	20	25	45	50	75	105	135
	Total Block RAM (Kb)	720	900	1,620	1,800	2,700	3,780	4,860
Clock Resources	CMTs (1 MMCM + 1 PLL)	3	5	3	5	5	6	6
I/O Resources	Maximum Single-Ended I/O	150	250	150	250	250	285	285
	Maximum Differential I/O Pairs	72	120	72	120	120	137	137
Embedded Hard IP Resources	DSP Slices	40	45	80	90	120	180	240
	PCIe® Gen2[1]	1	1	1	1	1	1	1
	Analog Mixed Signal (AMS) / XADC	1	1	1	1	1	1	1
	Configuration AES / HMAC Blocks	1	1	1	1	1	1	1
	GTP Transceivers (6.25Gb/s Max Rate)[2]	2	4	4	4	4	4	4
Speed Grades	I-Grade	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2	-1, -2
	Q-Grade	-1	-1	-1	-1	-1	-1	-1

Package[3]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)						
CPG236	10 x 10	0.5	106 (2)	106 (2)	106 (2)	106 (2)	106 (2)		
CSG324	15 x 15	0.8		210 (0)		210 (0)	210 (0)	210 (0)	210 (0)
CSG325	15 x 15	0.8	150 (2)	150 (4)	150 (4)	150 (4)	150 (4)		
FGG484	23 x 23	1.0						285 (4)	285 (4)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the CSG324 devices are available without transceivers. See the Package section of this table for details.
3. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

XA Kintex®-7 FPGAs

		Optimized for Best Price-Performance (1.0V, 0.95V, 0.9V)
	Part Number	XA7K160T
Logic Resources	Logic Cells	162,240
	Slices	25,350
	CLB Flip-Flops	202,800
Memory Resources	Maximum Distributed RAM (Kb)	2,188
	Block RAM/FIFO w/ ECC (36 Kb each)	325
	Total Block RAM (Kb)	11,700
Clock Resources	CMTs (1 MMCM + 1 PLL)	8
I/O Resources	Maximum Single-Ended I/O	400
	Maximum Differential I/O Pairs	192
Embedded Hard IP Resources	DSP Slices	600
	PCIe® Gen2[1]	1
	Analog Mixed Signal (AMS) / XADC	1
	Configuration AES / HMAC Blocks	1
	GTX Transceivers (8.0Gb/s Max Rate)[2]	8
Speed Grades	Q-Grade	-1

Package[3]	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTX Transceivers)
FFG676	27 x 27	1.0	106 (2)

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available.
3. Device migration is not supported between other 7 series families.

XA Spartan®-7 FPGAs

			I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V)					
Part Number			XA7S6	XA7S15	XA7S25	XA7S50	XA7S75	XA7S100
Logic Cells			6,000	12,800	23,360	52,160	76,800	102,400
Slices			938	2,000	3,650	8,151	12,000	16,000
CLB Flip-Flops			7,500	16,000	29,200	65,200	96,000	128,000
Max. Distributed RAM (Kb)			70	150	313	600	832	1,100
Block RAM/FIFO w/ ECC (36Kb each)			5	10	45	75	90	120
Total Block RAM (Kb)			180	360	1,620	2,700	3,240	4,320
Clock Mgmt Tiles (1 MMCM + 1 PLL)			2	2	3	5	8	8
Max. Single-Ended I/O Pins			100	100	150	250	400	400
Max. Differential I/O Pairs			48	48	72	120	192	192
DSP Slices			10	20	80	120	140	160
Analog Mixed Signal (AMS) / XADC			0	0	1	1	1	1
Configuration AES / HMAC Blocks			0	0	1	1	1	1
I-Grade			-1,-2	-1,-2	-1,-2	-1,-2	-1,-2	-1,-2
Q-Grade			-1	-1	-1	-1	-1	-1
Package	Dimensions (mm)	Ball Pitch (mm)	Available User I/O: 3.3V SelectIO™ HR I/O					
CPGA196	8x8	0.5	100	100				
CSGA225	13x13	0.8	100	100	150			
CSGA324	15x15	0.8			150	210		
FGGA484	23x23	1.0				250	338	338
FGGA676	27x27	1.0					400	400

XA Spartan®-6 FPGAs

Transceiver Optimization at the Lowest Cost (1.2V)

	Part Number	XA6SLX4	XA6SLX9	XA6SLX16	XA6SLX25	XA6SLX45	XA6SLX75	XA6SLX100	XA6SLX25T	XA6SLX45T	XA6SLX75T
Logic Resources	Logic Cells	3,840	9,152	14,579	24,051	43,661	74,637	101,262	24,051	43,661	74,637
	Slices	600	1,430	2,278	3,758	6,822	11,662	15,822	3,758	6,822	11,662
	CLB Flip-Flops	4,800	11,440	18,224	30,064	54,576	93,296	126,576	30,064	54,576	93,296
Memory Resources	Maximum Distributed RAM (Kb)	75	90	136	229	401	692	976	229	401	692
	Block RAM (18Kb ea.)	12	32	32	52	116	172	268	52	116	172
	Total Block RAM (Kb)	216	576	576	936	2,088	3,096	4,824	936	2,088	3,096
Clock Resources	CMTs (2 DCM + 1 PLL)	2	2	2	2	4	6	6	2	4	6
Embedded Hard IP Resources	Memory Controller Blocks (Max)	0	2	2	2	2	2	2	2	2	2
	Endpoint Blocks PCIe®	0	0	0	0	0	0	0	1	1	1
	GTP Transceivers (3.2Gb/s Max Rate)	0	0	0	0	0	0	0	2	4	4
	Total I/O Banks	4	4	4	4	4	4	4	4	4	4
	Max User I/O	132	200	232	266	320	328	326	250	296	268
Speed Grades	I-Grade	-2, -3									
	Q-Grade	-2, -3									

Package	Dimensions (mm)	Ball Pitch (mm)	**Available User I/O**: 3.3V SelectIO™ HR I/O (GTP Transceivers)									
CSG225	13 x 13	0.8	132 (0)	160 (0)	160 (0)							
FTG256	17 x 17	1.0		186 (0)	186 (0)	186 (0)						
CSG324	15 x 15	0.8		200 (0)	232 (0)	226 (0)	218 (0)			190 (2)	190 (4)	
CSG484	19 x 19	0.8					320 (0)	328 (0)				
FGG484	23 x 23	1.0				266 (0)	316 (0)	280 (0)	326 (0)	250 (2)	296 (4)	268 (4)

Device Ordering Information

ZYNQ UltraSCALE+

XA	ZU	#	E	G	-1	S	B	V	A	484	I
Xilinx Automotive	Generation	Value Index	Processor System E: Dual RPU Quad APU Single GPU	Engine Type G: General Purpose V: Video	Speed Grade -1 = Standard -1L = Low Power	S: Flip-Chip (.8mm)	F: Lid B: Lidless	V: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (I, Q)

ZYNQ

XA	7	Z	###	-1	FB	V	484	Q
Xilinx Automotive	Generation	Family	Value Index	Speed Grade -1 = Standard	CL: Wire-bond (.8 mm) FB: Flip-Chip (1 mm)	V: RoHS 6/6 G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

SPARTAN 7

XA	7	S	###	-1	FG	G	A	484	Q
Xilinx Automotive	Generation	Family	Logic Cells in 1K Units	Speed Grade -1 = Standard -2 = Medium	CP: Wire-bond (.5 mm) FT: Wire-bond (1mm) CS: Wire-bond (.8 mm) FG: Wire-bond (1 mm)	G: RoHS 6/6	Package Designator	Package Pin Count	Temperature Grade (I, Q)

KINTEX 7

XA	7	K	160T	-1	FF	G	676	I
Xilinx Automotive	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Standard	FF: Wire-bond (1mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

ARTIX 7

XA	7	A	###	-1	CP	G	236	I
Xilinx Automotive	Generation	Family	Logic Cells In 1K units	Speed Grade -1 = Standard -2 = Medium	CP: Wire-bond (.5mm) CS: Wire-bond (.8mm) FG: Wire-bond (1mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

SPARTAN 6

XA	6	S	LX LXT	###	-1	FG	G	484	Q
Xilinx Automotive	Generation	Family	Sub-families LX: Logic LXT: Logic + Transceivers	Logic Cells in 1K Units	Speed Grade -2 = Mid -3 = Highest	CS: Wire-bond (.8 mm) FT: Wire-bond (1mm) FG: Wire-bond (1 mm)	G: RoHS 6/6	Package Pin Count	Temperature Grade (I, Q)

I = Tj from –40°C to +100°C ; Q = Tj from –40°C to +125°C

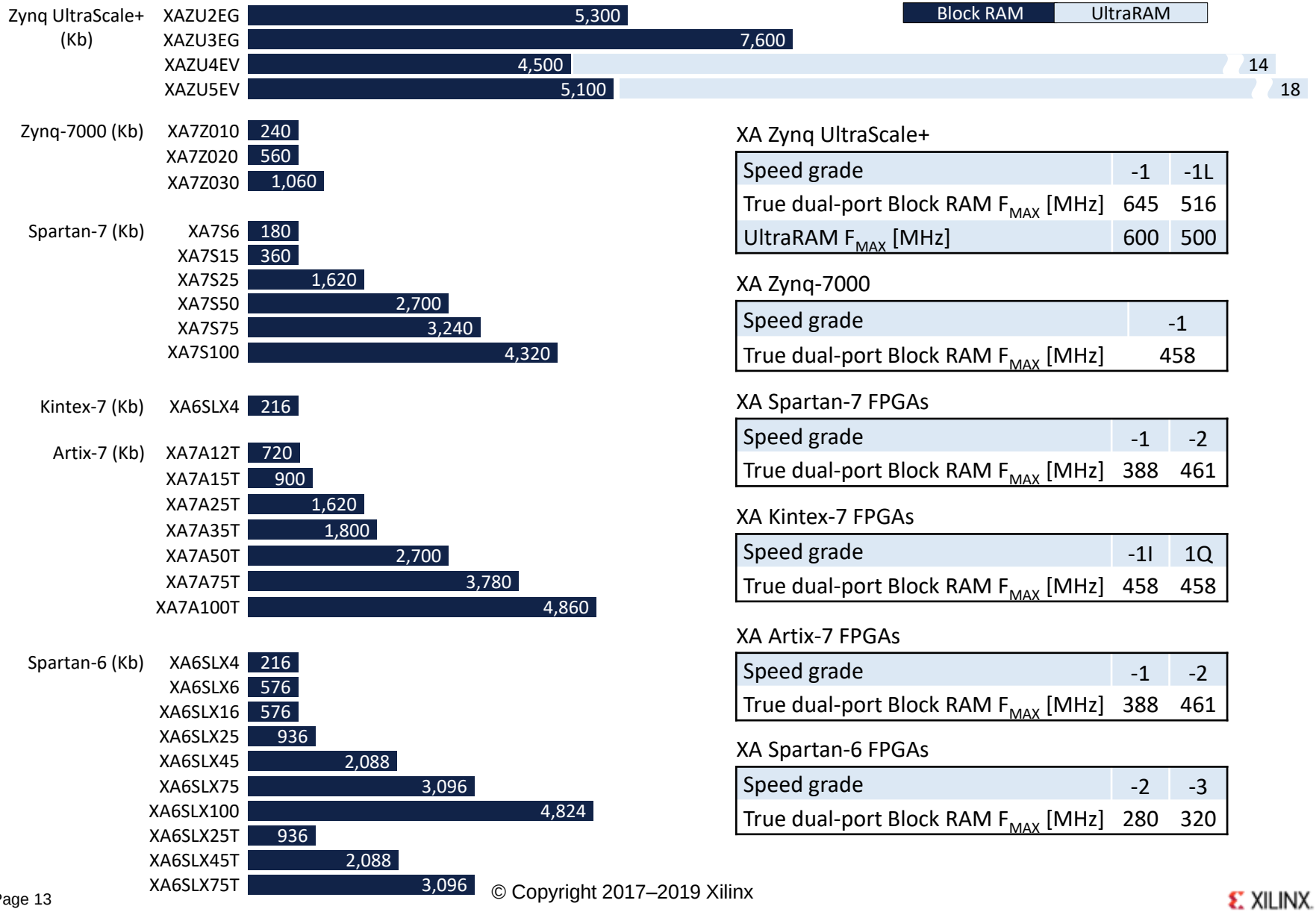
Important: Verify all data in this document with the device data sheets found at www.xilinx.com

External Memory Controller Maximum Bandwidth (Mb/s)

	XA Zynq® UltraScale+™				XA Zynq-7000				XA Spartan®-7			XA Kintex-7	XA Artix®-7			XA Spartan-6
Core Voltage	-1I/Q (0.85V)		-L1 (0.72V)		-1I (1.0V)		-1Q (1.0V)		-1I (1.0V)	-1Q (1.0V)	-2I (1.0V)	-1Q (1.0V)	-1I (1.0V)	-1Q (1.0V)	-2I (1.0V)	-2, -3 (1.2V)
	PL	PS	PL	PS	PL	PS	PL	PS	–	–	–	–	–	–	–	–
DDR4	2400	2400	2133	2400	–	–	–	–	–	–	–	–	–	–	–	–
DDR3	2133	2133	1866	2133	800	1066	667	1066	667	667	800	800	800	667	800	800
DDR3L	1866	1866	1600	1866	667	1066	–	1066	667	667	800	800	667	N/A	800	–
DDR2	–	–	–	–	667	800	533	800	667	667	800	667	667	533	800	400
DDR	–	–	–	–	–	355	–	355	–	–	–	–	–	–	–	400
LPDDR4	–	2400	–	2400	–	–	–	–	–	–	–	–	–	–	–	–
LPDDR3	1600	1600	1600	1600	–	–	–	–	–	–	–	–	–	–	–	–
LPDDR2	–	–	–	–	533	800	400	800	–	–	–	533	–	–	–	–
LPDDR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	–	400

Important: Verify all data in this document with the device data sheets found at www.xilinx.com

Internal Memory Block RAM Metrics



XA Zynq UltraScale+

Speed grade	-1	-1L
True dual-port Block RAM F_{MAX} [MHz]	645	516
UltraRAM F_{MAX} [MHz]	600	500

XA Zynq-7000

Speed grade	-1
True dual-port Block RAM F_{MAX} [MHz]	458

XA Spartan-7 FPGAs

Speed grade	-1	-2
True dual-port Block RAM F_{MAX} [MHz]	388	461

XA Kintex-7 FPGAs

Speed grade	-1I	1Q
True dual-port Block RAM F_{MAX} [MHz]	458	458

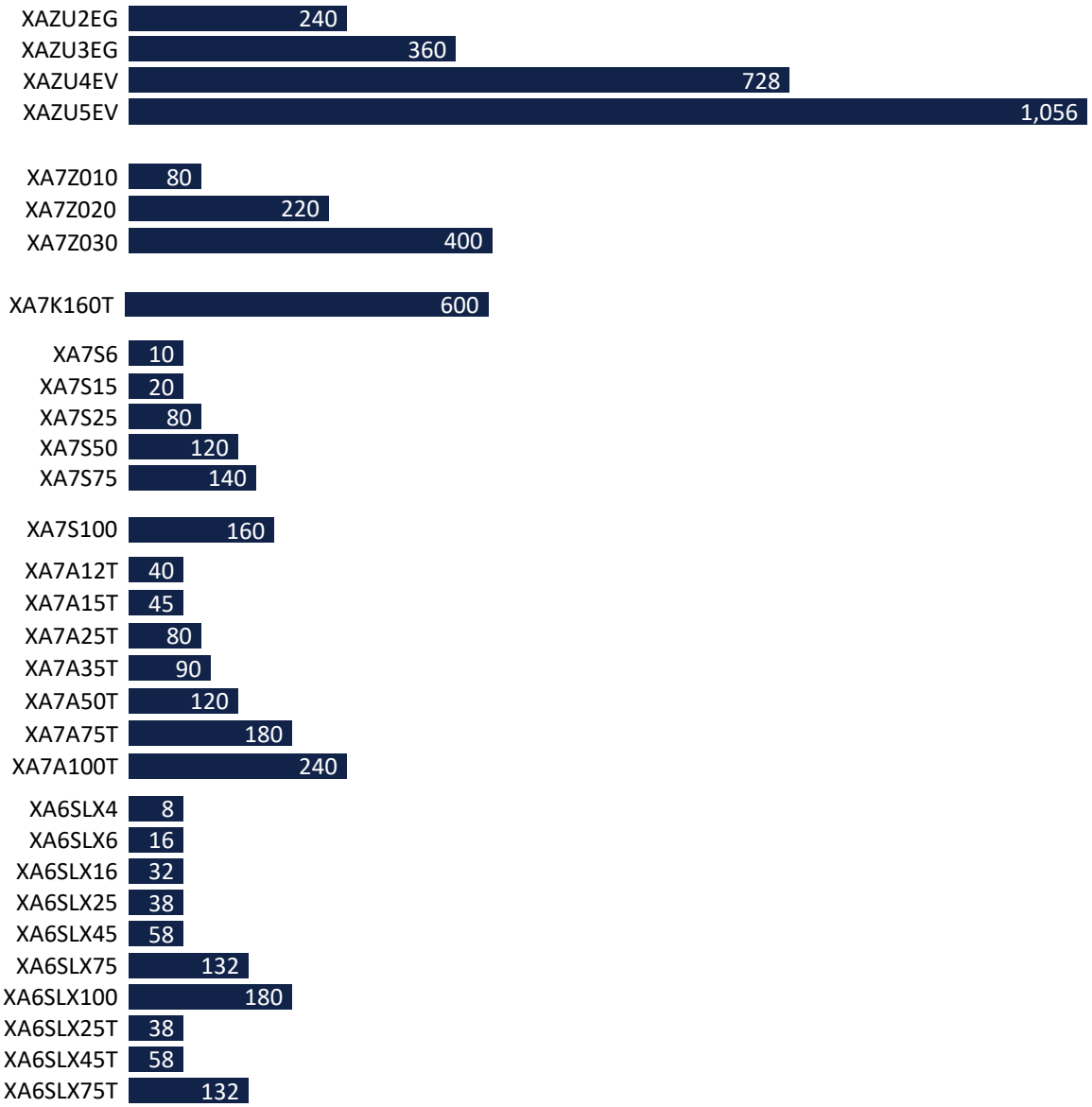
XA Artix-7 FPGAs

Speed grade	-1	-2
True dual-port Block RAM F_{MAX} [MHz]	388	461

XA Spartan-6 FPGAs

Speed grade	-2	-3
True dual-port Block RAM F_{MAX} [MHz]	280	320

Digital Signal Processing Metrics



XA Zynq UltraScale+ MPSoC

Speed grade	-1	-1L
F_{MAX} [MHz]	645	600
Max GMAC/s	1,362	1,267

XA Zynq-7000 SoC

Speed grade	-1
F_{MAX} [MHz]	547
Max GMAC/s	438

XA Kintex-7 FPGAs

Speed grade	-1I	-1Q
F_{MAX} [MHz]	547	547
Max GMAC/s	352	352

XA Spartan-7 FPGAs

Speed grade	-1	-2
F_{MAX} [MHz]	464	550
Max GMAC/s	148	176

XA Artix-7 FPGAs

Speed grade	-1	-2
F_{MAX} [MHz]	464	550
Max GMAC/s	223	264

XA Spartan-6 FPGAs

Speed Grade	-2	-3
F_{MAX} [MHz]	333	390
Max GMAC/s	120	103 (LX75)

References

DS894, XA Zynq UltraScale+ MPSoC Data Sheet: Overview

DS925, Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics

DS180, 7 Series FPGAs Data Sheet: Overview

DS197, XA Artix-7 FPGAs Data Sheet: Overview

DS181, Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics

DS188, XA Zynq-7000 All Programmable SoC Data Sheet: Overview

DS187, Zynq-7000 SoC Data Sheet: DC and AC Switching Characteristics

DS175, XA Kintex-7 FPGA Data Sheet: Overview

DS189, Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics

DS170, XA Spartan-6 Automotive FPGA Family Data Sheet: Overview

DS162, Spartan-6 FPGAs Data Sheet: DC and AC Switching Characteristics

UG1085, Zynq UltraScale+ MPSoC Technical Reference Manual

UG1213, Zynq Migration Guide – Zynq-7000 AP SoC to Zynq UltraScale+ MPSoC Devices

For more information on Automotive products, go to https://www.xilinx.com/applications/automotive.html