# All Programmable Automotive SoC Comparison

<table>
<thead>
<tr>
<th><strong>XA Zynq UltraScale+™ MPSoC</strong>&lt;br&gt;ZU2/3EG, ZU4/5EV Devices</th>
<th><strong>XA Zynq®-7000 SoC</strong>&lt;br&gt;Z-7010/7020/7030 Devices</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Application Processor</strong></td>
<td><strong>Dual-core Arm Cortex-A9 MPCore</strong>&lt;br&gt;up to <strong>667MHz</strong></td>
</tr>
<tr>
<td><strong>Real-Time Processor</strong></td>
<td><strong>Quad-core Arm® Cortex®-A53 MPCore™</strong>&lt;br&gt;up to <strong>1.2GHz</strong></td>
</tr>
<tr>
<td><strong>Graphics Processor</strong></td>
<td><strong>Dual-core Arm Cortex-R5 MPCore up to 500MHz</strong></td>
</tr>
<tr>
<td><strong>Mali™-400 MP2 up to 600MHz</strong></td>
<td><strong>N/A</strong></td>
</tr>
<tr>
<td><strong>External Dynamic Memory Interface</strong></td>
<td><strong>Quad-core Arm® Cortex®-A53 MPCore™</strong>&lt;br&gt;up to <strong>1.2GHz</strong></td>
</tr>
<tr>
<td><strong>x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 w/ ECC</strong></td>
<td><strong>Dual-core Arm Cortex-A9 MPCore</strong>&lt;br&gt;up to <strong>667MHz</strong></td>
</tr>
<tr>
<td><strong>Programmable Logic</strong></td>
<td><strong>x16/x32: DDR3L, DDR3, DDR2, LPDDR2 w/ECC</strong>&lt;br&gt;(supports 16-bit)</td>
</tr>
<tr>
<td><strong>103K–256K System Logic Cells</strong></td>
<td><strong>28K–125K Logic Cells</strong></td>
</tr>
<tr>
<td><strong>DSP Slices</strong></td>
<td><strong>80–400</strong></td>
</tr>
<tr>
<td><strong>240–1,248</strong></td>
<td><strong>80–400</strong></td>
</tr>
<tr>
<td><strong>Speed Grades</strong></td>
<td><strong>-1, -1L</strong></td>
</tr>
<tr>
<td><strong>Automotive Standards</strong></td>
<td><strong>-1</strong></td>
</tr>
<tr>
<td><strong>AEC-Q100, Production Part Approval Process</strong></td>
<td><strong>AEC-Q100, Production Part Approval Process</strong></td>
</tr>
<tr>
<td><strong>Power Management</strong></td>
<td><strong>Separate Voltage on PS &amp; PL, Full (PL+PS) / Full power domain / Low power domain / Battery Power Domains (PS)</strong></td>
</tr>
<tr>
<td><strong>Full (PS +PL), Separate Voltage on PS &amp; PL</strong></td>
<td><strong>N/A</strong></td>
</tr>
</tbody>
</table>
# All Programmable Automotive FPGA Comparison

<table>
<thead>
<tr>
<th></th>
<th>XA Artix®-7</th>
<th>XA Kintex®-7</th>
<th>XA Spartan®-7</th>
<th>XA Spartan-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Voltage</td>
<td>1.0V</td>
<td>1.0V</td>
<td>1.0V</td>
<td>1.2V</td>
</tr>
<tr>
<td>Logic Cell</td>
<td>12K–101K</td>
<td>162K</td>
<td>6K–102K</td>
<td>3K–74K</td>
</tr>
<tr>
<td>Total Block RAM (K)</td>
<td>720–4,860</td>
<td>2,188</td>
<td>180–4,320</td>
<td>216–3,096</td>
</tr>
<tr>
<td>CMTs</td>
<td>3–6</td>
<td>8</td>
<td>2–8</td>
<td>2–6</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>40–240</td>
<td>600</td>
<td>10–160</td>
<td>8–132</td>
</tr>
<tr>
<td>PCIe®</td>
<td>1 @ Gen2 up to x4</td>
<td>1 @ Gen2 up to x 8</td>
<td>0</td>
<td>0–1 @ Gen1 x1</td>
</tr>
<tr>
<td>Serial Transceivers</td>
<td>2–4</td>
<td>8</td>
<td>0</td>
<td>0–4</td>
</tr>
<tr>
<td>Speed Grades</td>
<td>-1, -2</td>
<td>-1</td>
<td>-1, -2</td>
<td>-2, -3</td>
</tr>
<tr>
<td>Automotive Standards</td>
<td>AEC-Q100, Production Part Approval Process</td>
<td>AEC-Q100, Production Part Approval Process</td>
<td>AEC-Q100, Production Part Approval Process</td>
<td>AEC-Q100, Production Part Approval Process</td>
</tr>
</tbody>
</table>
# XA Zynq® UltraScale+™ MPSoCs

<table>
<thead>
<tr>
<th></th>
<th>Device Name(^{(1)})</th>
<th>ZU2EG</th>
<th>ZU3EG</th>
<th>ZU4EV</th>
<th>ZU5EV</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Application</strong></td>
<td>Processor Core</td>
<td>Quad-core Arm® Cortex®-A53 MPCore™ up to 1.2GHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Processor Unit</strong></td>
<td>Memory w/ECC</td>
<td>L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Real-Time Processor</strong></td>
<td>Processor Core</td>
<td>Dual-core Arm Cortex-R5 MPCore up to 500MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Unit</strong></td>
<td>Memory w/ECC</td>
<td>L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Graphic &amp; Video Acceleration</strong></td>
<td>Graphics Processing Unit Memory</td>
<td>Mali™-400 MP2 up to 600MHz</td>
<td>L2 Cache 64KB</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>External Memory</strong></td>
<td>Dynamic Memory Interface</td>
<td>x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC</td>
<td>Dynamic Memory Interface</td>
<td>Static Memory Interfaces</td>
<td>PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet</td>
</tr>
<tr>
<td><strong>Connectivity</strong></td>
<td>Power Management</td>
<td>Full / Low / PL / Battery Power Domains</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>PS to PL Interface</strong></td>
<td>Security</td>
<td>RSA, AES, and SHA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Integrated Block Functionality</strong></td>
<td>AMS - System Monitor</td>
<td>10-bit, 1MSPS - Temperature, Voltage, and Current Monitor</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Programmable Logic (PL)</strong></td>
<td>System Logic Cells (K)</td>
<td>103</td>
<td>154</td>
<td>192</td>
<td>256</td>
</tr>
<tr>
<td></td>
<td>CLB Flip-Flops (K)</td>
<td>94</td>
<td>141</td>
<td>176</td>
<td>234</td>
</tr>
<tr>
<td></td>
<td>CLB LUTs (K)</td>
<td>47</td>
<td>71</td>
<td>88</td>
<td>117</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>Max. Distributed RAM (Mb)</td>
<td>1.2</td>
<td>1.8</td>
<td>2.6</td>
<td>3.5</td>
</tr>
<tr>
<td></td>
<td>Total Block RAM (Mb)</td>
<td>5.3</td>
<td>7.6</td>
<td>4.5</td>
<td>5.1</td>
</tr>
<tr>
<td></td>
<td>UltraRAM (Mb)</td>
<td>-</td>
<td>-</td>
<td>14.0</td>
<td>18.0</td>
</tr>
<tr>
<td><strong>Clocking</strong></td>
<td>Clock Management Tiles (CMTs)</td>
<td>3</td>
<td>3</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td><strong>Programmable Logic (PL)</strong></td>
<td>DSP Slices</td>
<td>240</td>
<td>360</td>
<td>728</td>
<td>1,248</td>
</tr>
<tr>
<td></td>
<td>VCU</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Integrated IP</strong></td>
<td>PCI Express Gen 3x16 / Gen4x8</td>
<td>-</td>
<td>-</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td></td>
<td>150G Interlaken</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>100G Ethernet MAC/PCS w/RS-FEC</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td></td>
<td>AMS - System Monitor</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td><strong>Transceivers</strong></td>
<td>GTH 12.5Gb/s Transceivers</td>
<td>-</td>
<td>-</td>
<td>16</td>
<td>16</td>
</tr>
<tr>
<td><strong>Speed Grades</strong></td>
<td>I-Grade</td>
<td>-1 (0.85V), -L1 (0.72V)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Q-Grade</td>
<td>-1 (0.85V)</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Notes:
1. For full part number details, see the Ordering Information section in DS891, Zynq UltraScale+ MPSoC Overview.

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### XA Zynq® UltraScale+™ MPSoCs
PS I/Os(1), 3.3V High-Density (HD) I/O, 1.8V High-Performance (HP) I/Os
PS-GTR 6Gb/s, GTH 12.5Gb/s

<table>
<thead>
<tr>
<th>Pkg Footprint(2)</th>
<th>Dimensions (mm)</th>
<th>XAZU2EG</th>
<th>XAZU3EG</th>
<th>XAZU4EV</th>
<th>XAZU5EV</th>
</tr>
</thead>
<tbody>
<tr>
<td>SBVA484(3)</td>
<td>19x19</td>
<td>170, 24, 58</td>
<td>170, 24, 58</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4, 0</td>
<td>4, 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFVA625(3)</td>
<td>21x21</td>
<td>170, 24, 156</td>
<td>170, 24, 156</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>4, 0</td>
<td>4, 0</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SFVC784(3)</td>
<td>23x23</td>
<td>214, 96, 156</td>
<td>214, 96, 156</td>
<td>214, 96, 156</td>
<td>214, 96, 156</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4, 0</td>
<td>4, 0</td>
<td>4, 4</td>
<td>4, 4</td>
</tr>
</tbody>
</table>

Notes:
1. PS I/O is a combination of PS MIO and PS DDRIO.
2. For full part number details, see the Ordering Information section in [DS891, Zynq UltraScale+ MPSoC Overview](#).
3. These packages are only offered in 0.8mm ballpitch.

Important: Verify all data in this document with the device data sheets found at www.xilinx.com
# XA Zynq®-7000 SoCs

<table>
<thead>
<tr>
<th>Device Name</th>
<th>XA7Z010</th>
<th>XA7Z020</th>
<th>XA7Z030</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Application</strong></td>
<td>Processor Core</td>
<td>Dual Arm® Cortex®-A9 MPCore™ up to 667MHz</td>
<td></td>
</tr>
<tr>
<td><strong>Processor Unit</strong></td>
<td>Processor Extension</td>
<td>NEON™ SIMD Engine and Single/Double Precision Floating Point Unit per Processor</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L1 Cache</td>
<td>32KB I / D per Core</td>
<td></td>
</tr>
<tr>
<td></td>
<td>L2 Cache</td>
<td>512KB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>On-Chip Memory</td>
<td>256KB</td>
<td></td>
</tr>
<tr>
<td><strong>External Memory</strong></td>
<td>Dynamic Memory Interface</td>
<td>x32/x64: DDR3, DDR3L, DDR2, LPDDR2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Static Memory Interfaces</td>
<td>NAND, NOR, 2x Quad-SPI</td>
<td></td>
</tr>
<tr>
<td><strong>Connectivity</strong></td>
<td>High-Speed Connectivity</td>
<td>2x Tri-mode Gigabit Ethernet</td>
<td></td>
</tr>
<tr>
<td></td>
<td>General Connectivity</td>
<td>2xUSB 2.0, 2x SD/SDIO/eMMC, 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO</td>
<td></td>
</tr>
<tr>
<td><strong>Integrated Block</strong></td>
<td>Security</td>
<td>RSA, AES, and SHA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Functionality</td>
<td>2x12-bit, 1MSPS - Temperature, Voltage, and Current Monitor</td>
<td></td>
</tr>
<tr>
<td><strong>PS to PL Interface</strong></td>
<td></td>
<td>9 x 32/64 AXI Ports</td>
<td></td>
</tr>
</tbody>
</table>

| Programmable Logic (PL) | | | |
|-------------------------|---------|---------|
| **Programmable Functionality** | Xilinx 7 Series PL Equivalent | Artix-7 | Artix-7 | Kintex-7 |
| | Logic Cells | 28,160 | 85,280 | 125,760 |
| | CLB Flip-Flops | 35,300 | 106,400 | 157,200 |
| | CLB LUTs | 17,600 | 53,300 | 78,600 |
| **Memory** | Total Block RAM (KB) | 240 | 560 | 1,060 |
| | (# 36 Kb Blocks) | (60) | (140) | (265) |
| | DSP Slices | 80 | 220 | 400 |
| **Integrated IP** | Peak DSP Performance | 100 GMACs | 276 GMACs | 593 GMACs |
| | PCI Express | - | - | Gen2 x4 |
| | AMS / XADC | AES and SHA 256b Decryption and Authentication for Secure Programmable Configuration | | |
| **Speed Grades** | | I-Grade | -1 | |
| | Q-Grade | -1 | | |
| **Package** | Size (mm) | Pitch (mm) | HR I/O(2), HP I/O(3), PS I/O(4), GTX Transceiver |
| CLG225 | 13x13 | 0.8 | 54, 0, 84, 0 |
| CLG400 | 17x17 | 0.8 | 100, 0, 128, 0 |
| CLG484 | 19x19 | 0.8 | 125, 0, 128, 0 |
| FBV484 | 23x23 | 1.0 | 200, 0, 128, 0 |

Notes:
1. All packages listed are Pb-free.
2. HR = High Range I/O with support for I/O voltage from 1.2V up to 3.3V.
3. HP = High Performance I/O with support for I/O voltage from 1.2V to 1.8V.
4. PS I/O includes user I/O and DDR I/O.

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## XA Artix®-7 FPGAs

Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Logic Cells</th>
<th>Slices</th>
<th>CLB Flip-Flops</th>
<th>Transceiver Optimization at the Lowest Cost and Highest DSP Bandwidth (1.0V, 0.95V, 0.9V)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>(1.0V, 0.95V, 0.9V)</td>
</tr>
<tr>
<td>12,800</td>
<td>2,000</td>
<td>16,000</td>
<td>20,800</td>
<td>XA7A12T</td>
</tr>
<tr>
<td>16,640</td>
<td>2,600</td>
<td>29,200</td>
<td>23,360</td>
<td>XA7A15T</td>
</tr>
<tr>
<td>23,360</td>
<td>3,650</td>
<td>41,600</td>
<td>33,280</td>
<td>XA7A25T</td>
</tr>
<tr>
<td>33,280</td>
<td>5,200</td>
<td>65,200</td>
<td>52,160</td>
<td>XA7A35T</td>
</tr>
<tr>
<td>52,160</td>
<td>8,150</td>
<td>94,400</td>
<td>75,520</td>
<td>XA7A50T</td>
</tr>
<tr>
<td>75,520</td>
<td>11,800</td>
<td>126,800</td>
<td>101,440</td>
<td>XA7A75T</td>
</tr>
<tr>
<td>101,440</td>
<td>15,850</td>
<td></td>
<td></td>
<td>XA7A100T</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Logic Resources</th>
<th>XA7A12T</th>
<th>XA7A15T</th>
<th>XA7A25T</th>
<th>XA7A35T</th>
<th>XA7A50T</th>
<th>XA7A75T</th>
<th>XA7A100T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>12,800</td>
<td>16,640</td>
<td>23,360</td>
<td>33,280</td>
<td>52,160</td>
<td>75,520</td>
<td>101,440</td>
</tr>
<tr>
<td>Slices</td>
<td>2,000</td>
<td>2,600</td>
<td>3,650</td>
<td>5,200</td>
<td>8,150</td>
<td>11,800</td>
<td>15,850</td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>16,000</td>
<td>20,800</td>
<td>29,200</td>
<td>41,600</td>
<td>65,200</td>
<td>94,400</td>
<td>126,800</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory Resources</th>
<th>XA7A12T</th>
<th>XA7A15T</th>
<th>XA7A25T</th>
<th>XA7A35T</th>
<th>XA7A50T</th>
<th>XA7A75T</th>
<th>XA7A100T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Distributed RAM (Kb)</td>
<td>171</td>
<td>200</td>
<td>313</td>
<td>400</td>
<td>600</td>
<td>892</td>
<td>1,188</td>
</tr>
<tr>
<td>Block RAM/FIFO w/ ECC (36 Kb each)</td>
<td>20</td>
<td>25</td>
<td>45</td>
<td>50</td>
<td>75</td>
<td>105</td>
<td>135</td>
</tr>
<tr>
<td>Total Block RAM (Kb)</td>
<td>720</td>
<td>900</td>
<td>1,620</td>
<td>1,800</td>
<td>2,700</td>
<td>3,780</td>
<td>4,860</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Clock Resources</th>
<th>XA7A12T</th>
<th>XA7A15T</th>
<th>XA7A25T</th>
<th>XA7A35T</th>
<th>XA7A50T</th>
<th>XA7A75T</th>
<th>XA7A100T</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMTs (1 MMCM + 1 PLL)</td>
<td>3</td>
<td>5</td>
<td>3</td>
<td>5</td>
<td>5</td>
<td>6</td>
<td>6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>I/O Resources</th>
<th>XA7A12T</th>
<th>XA7A15T</th>
<th>XA7A25T</th>
<th>XA7A35T</th>
<th>XA7A50T</th>
<th>XA7A75T</th>
<th>XA7A100T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum Single-Ended I/O</td>
<td>150</td>
<td>250</td>
<td>150</td>
<td>250</td>
<td>250</td>
<td>285</td>
<td>285</td>
</tr>
<tr>
<td>Maximum Differential I/O Pairs</td>
<td>72</td>
<td>120</td>
<td>72</td>
<td>120</td>
<td>120</td>
<td>137</td>
<td>137</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Embedded Hard IP Resources</th>
<th>XA7A12T</th>
<th>XA7A15T</th>
<th>XA7A25T</th>
<th>XA7A35T</th>
<th>XA7A50T</th>
<th>XA7A75T</th>
<th>XA7A100T</th>
</tr>
</thead>
<tbody>
<tr>
<td>DSP Slices</td>
<td>40</td>
<td>45</td>
<td>80</td>
<td>90</td>
<td>120</td>
<td>180</td>
<td>240</td>
</tr>
<tr>
<td>PCIe® Gen2(1)</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Analog Mixed Signal (AMS) / XADC</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Configuration AES / HMAC Blocks</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>GTP Transceivers (6.25Gb/s Max Rate)(2)</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>I-Grade</td>
<td>-1, -2</td>
<td>-1, -2</td>
<td>-1, -2</td>
<td>-1, -2</td>
<td>-1, -2</td>
<td>-1, -2</td>
<td>-1, -2</td>
</tr>
<tr>
<td>Q-Grade</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Speed Grades</th>
<th>XA7A12T</th>
<th>XA7A15T</th>
<th>XA7A25T</th>
<th>XA7A35T</th>
<th>XA7A50T</th>
<th>XA7A75T</th>
<th>XA7A100T</th>
</tr>
</thead>
<tbody>
<tr>
<td>I-Grade</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
<tr>
<td>Q-Grade</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
</tbody>
</table>

### Package(3) | Dimensions (mm) | Ball Pitch (mm) | Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers) |
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>CPG236</td>
<td>10 x 10</td>
<td>0.5</td>
<td>106 (2)</td>
</tr>
<tr>
<td>CSG324</td>
<td>15 x 15</td>
<td>0.8</td>
<td>210 (0)</td>
</tr>
<tr>
<td>CSG325</td>
<td>15 x 15</td>
<td>0.8</td>
<td>150 (2)</td>
</tr>
<tr>
<td>FGG484</td>
<td>23 x 23</td>
<td>1.0</td>
<td>285 (4)</td>
</tr>
</tbody>
</table>

Notes:
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available. Note that the CSG324 devices are available without transceivers. See the Package section of this table for details.
3. Device migration is available within the Artix-7 family for like packages but is not supported between other 7 series families.

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### XA Kintex®-7 FPGAs

**Optimized for Best Price-Performance**
(1.0V, 0.95V, 0.9V)

<table>
<thead>
<tr>
<th>Logic Resources</th>
<th>Part Number</th>
<th>XA7K160T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>162,240</td>
<td></td>
</tr>
<tr>
<td>Slices</td>
<td>25,350</td>
<td></td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>202,800</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Memory Resources</th>
<th>Maximum Distributed RAM (Kb)</th>
<th>2,188</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Block RAM/FIFO w/ ECC (36 Kb each)</td>
<td>325</td>
</tr>
<tr>
<td></td>
<td>Total Block RAM (Kb)</td>
<td>11,700</td>
</tr>
</tbody>
</table>

| Clock Resources  | CMTs (1 MMCM + 1 PLL)          | 8     |

| I/O Resources    | Maximum Single-Ended I/O       | 400   |
|------------------| Maximum Differential I/O Pairs | 192   |

<table>
<thead>
<tr>
<th>Embedded Hard IP Resources</th>
<th>PCIe® Gen2(^{(1)})</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Analog Mixed Signal (AMS) / XADC</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>Configuration AES / HMAC Blocks</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>GTX Transceivers (8.0Gb/s Max Rate)(^{(2)})</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Q-Grade</td>
<td>-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Speed Grades</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Package(^{(3)})</td>
<td>Dimensions (mm)</td>
</tr>
<tr>
<td>FFG676</td>
<td>27 x 27</td>
</tr>
</tbody>
</table>

**Notes:**
1. Supports PCI Express Base 2.1 specification at Gen1 and Gen2 data rates.
2. Represents the maximum number of transceivers available.
3. Device migration is not supported between other 7 series families.
## XA Spartan®-7 FPGAs

### I/O Optimization at the Lowest Cost and Highest Performance-per-Watt (1.0V)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>XA7S6</th>
<th>XA7S15</th>
<th>XA7S25</th>
<th>XA7S50</th>
<th>XA7S75</th>
<th>XA7S100</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>6,000</td>
<td>12,800</td>
<td>23,360</td>
<td>52,160</td>
<td>76,800</td>
<td>102,400</td>
</tr>
<tr>
<td>Slices</td>
<td>938</td>
<td>2,000</td>
<td>3,650</td>
<td>8,151</td>
<td>12,000</td>
<td>16,000</td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>7,500</td>
<td>16,000</td>
<td>29,200</td>
<td>65,200</td>
<td>96,000</td>
<td>128,000</td>
</tr>
<tr>
<td>Max. Distributed RAM (Kb)</td>
<td>70</td>
<td>150</td>
<td>313</td>
<td>600</td>
<td>832</td>
<td>1,100</td>
</tr>
<tr>
<td>Block RAM/FIFO w/ ECC (36Kb each)</td>
<td>5</td>
<td>10</td>
<td>45</td>
<td>75</td>
<td>90</td>
<td>120</td>
</tr>
<tr>
<td>Total Block RAM (Kb)</td>
<td>180</td>
<td>360</td>
<td>1,620</td>
<td>2,700</td>
<td>3,240</td>
<td>4,320</td>
</tr>
<tr>
<td>Clock Mgmt Tiles (1 MMCM + 1 PLL)</td>
<td>2</td>
<td>2</td>
<td>3</td>
<td>5</td>
<td>8</td>
<td>8</td>
</tr>
<tr>
<td>Max. Single-Ended I/O Pins</td>
<td>100</td>
<td>100</td>
<td>150</td>
<td>250</td>
<td>400</td>
<td>400</td>
</tr>
<tr>
<td>Max. Differential I/O Pairs</td>
<td>48</td>
<td>48</td>
<td>72</td>
<td>120</td>
<td>192</td>
<td>192</td>
</tr>
<tr>
<td>DSP Slices</td>
<td>10</td>
<td>20</td>
<td>80</td>
<td>120</td>
<td>140</td>
<td>160</td>
</tr>
<tr>
<td>Analog Mixed Signal (AMS) / XADC</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Configuration AES / HMAC Blocks</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>I-Grade</td>
<td>-1,-2</td>
<td>-1,-2</td>
<td>-1,-2</td>
<td>-1,-2</td>
<td>-1,-2</td>
<td>-1,-2</td>
</tr>
<tr>
<td>Q-Grade</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
<td>-1</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Package</th>
<th>Dimensions (mm)</th>
<th>Ball Pitch (mm)</th>
<th>Available User I/O: 3.3V SelectIO™ HR I/O</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPGA196</td>
<td>8x8</td>
<td>0.5</td>
<td>100</td>
</tr>
<tr>
<td>CSGA225</td>
<td>13x13</td>
<td>0.8</td>
<td>100</td>
</tr>
<tr>
<td>CSGA324</td>
<td>15x15</td>
<td>0.8</td>
<td>100</td>
</tr>
<tr>
<td>FGGA484</td>
<td>23x23</td>
<td>1.0</td>
<td>250</td>
</tr>
<tr>
<td>FGGA676</td>
<td>27x27</td>
<td>1.0</td>
<td>400</td>
</tr>
</tbody>
</table>
# XA Spartan®-6 FPGAs

## Transceiver Optimization at the Lowest Cost (1.2V)

<table>
<thead>
<tr>
<th>Part Number</th>
<th>XA6SLX4</th>
<th>XA6SLX9</th>
<th>XA6SLX16</th>
<th>XA6SLX25</th>
<th>XA6SLX45</th>
<th>XA6SLX75</th>
<th>XA6SLX100</th>
<th>XA6SLX25T</th>
<th>XA6SLX45T</th>
<th>XA6SLX75T</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Cells</td>
<td>3,840</td>
<td>9,152</td>
<td>14,579</td>
<td>24,051</td>
<td>43,661</td>
<td>74,637</td>
<td>101,262</td>
<td>24,051</td>
<td>43,661</td>
<td>74,637</td>
</tr>
<tr>
<td>Slices</td>
<td>600</td>
<td>1,430</td>
<td>2,278</td>
<td>3,758</td>
<td>6,822</td>
<td>11,662</td>
<td>15,822</td>
<td>3,758</td>
<td>6,822</td>
<td>11,662</td>
</tr>
<tr>
<td>CLB Flip-Flops</td>
<td>4,800</td>
<td>11,440</td>
<td>18,224</td>
<td>30,064</td>
<td>54,576</td>
<td>93,296</td>
<td>126,576</td>
<td>30,064</td>
<td>54,576</td>
<td>93,296</td>
</tr>
<tr>
<td>Memory Resources</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Distributed RAM (Kb)</td>
<td>75</td>
<td>90</td>
<td>136</td>
<td>229</td>
<td>401</td>
<td>692</td>
<td>976</td>
<td>229</td>
<td>401</td>
<td>692</td>
</tr>
<tr>
<td>Block RAM (18Kb ea.)</td>
<td>12</td>
<td>32</td>
<td>32</td>
<td>52</td>
<td>116</td>
<td>268</td>
<td>52</td>
<td>116</td>
<td>268</td>
<td></td>
</tr>
<tr>
<td>Total Block RAM (Kb)</td>
<td>216</td>
<td>576</td>
<td>576</td>
<td>936</td>
<td>2,088</td>
<td>3,096</td>
<td>4,824</td>
<td>936</td>
<td>2,088</td>
<td>3,096</td>
</tr>
<tr>
<td>Clock Resources</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMTs (2 DCM + 1 PLL)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>4</td>
<td>6</td>
<td>6</td>
<td>2</td>
<td>4</td>
<td>6</td>
</tr>
<tr>
<td>Embedded Hard IP Resources</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Memory Controller Blocks (Max)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Endpoint Blocks PCIe®</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>GTP Transceivers (3.2Gb/s Max Rate)</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Total I/O Banks</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>Max User I/O</td>
<td>132</td>
<td>200</td>
<td>232</td>
<td>266</td>
<td>320</td>
<td>328</td>
<td>326</td>
<td>250</td>
<td>296</td>
<td>268</td>
</tr>
</tbody>
</table>

## Logic Resources

### Speed Grades

<table>
<thead>
<tr>
<th>Package</th>
<th>Dimensions (mm)</th>
<th>Ball Pitch (mm)</th>
<th>Available User I/O: 3.3V SelectIO™ HR I/O (GTP Transceivers)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSG225</td>
<td>13 x 13</td>
<td>0.8</td>
<td>132 (0) 160 (0) 160 (0)</td>
</tr>
<tr>
<td>FTG256</td>
<td>17 x 17</td>
<td>1.0</td>
<td>186 (0) 186 (0) 186 (0)</td>
</tr>
<tr>
<td>CSG324</td>
<td>15 x 15</td>
<td>0.8</td>
<td>200 (0) 232 (0) 226 (0) 218 (0)</td>
</tr>
<tr>
<td>CSG484</td>
<td>19 x 19</td>
<td>0.8</td>
<td>266 (0) 316 (0) 280 (0) 326 (0)</td>
</tr>
<tr>
<td>FGG484</td>
<td>23 x 23</td>
<td>1.0</td>
<td>320 (0) 328 (0) 250 (2) 296 (4) 268 (4)</td>
</tr>
</tbody>
</table>

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## Device Ordering Information

### ZYNQ UltraSCALE+

<table>
<thead>
<tr>
<th>XA</th>
<th>ZU</th>
<th>#</th>
<th>E</th>
<th>G</th>
<th>-1</th>
<th>S</th>
<th>B</th>
<th>V</th>
<th>A</th>
<th>484</th>
<th>I</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx Automotive Generation Value Index Processor System Engine Type Speed Grade S: Flip-Chip F: Lid B: Lidless V: RoHS 6/6 Package Designator Package Pin Count Temperature Grade (I, Q)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>XA</td>
<td>7</td>
<td>Z</td>
<td>#</td>
<td>#</td>
<td>-1</td>
<td>FB</td>
<td>V</td>
<td>484</td>
<td>Q</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Xilinx Automotive Generation Family Value Index Speed Grade CL: Wire-bond (.8 mm) FB: Flip-Chip (1 mm) V: RoHS 6/6 G: RoHS 6/6 Package Pin Count Temperature Grade (I, Q)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Spartan

<table>
<thead>
<tr>
<th>XA</th>
<th>7</th>
<th>S</th>
<th>#</th>
<th>#</th>
<th>-1</th>
<th>FG</th>
<th>G</th>
<th>A</th>
<th>484</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx Automotive Generation Family Logic Cells in 1K Units Speed Grade CP: Wire-bond (.5 mm) G: RoHS 6/6 FT: Wire-bond (1 mm) CS: Wire-bond (.8 mm) FG: Wire-bond (1 mm) Package Designator Package Pin Count Temperature Grade (I, Q)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Kintex

<table>
<thead>
<tr>
<th>XA</th>
<th>7</th>
<th>K</th>
<th>160T</th>
<th>-1</th>
<th>FF</th>
<th>G</th>
<th>676</th>
<th>I</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx Automotive Generation Family Logic Cells in 1K units Speed Grade FF: Wire-bond (1 mm) G: RoHS 6/6 Package Pin Count Temperature Grade (I, Q)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Artix

<table>
<thead>
<tr>
<th>XA</th>
<th>7</th>
<th>A</th>
<th>#</th>
<th>#</th>
<th>-1</th>
<th>CP</th>
<th>G</th>
<th>236</th>
<th>I</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx Automotive Generation Family Logic Cells in 1K units Speed Grade CP: Wire-bond (.5 mm) CS: Wire-bond (.8 mm) FG: Wire-bond (1 mm) G: RoHS 6/6 Package Pin Count Temperature Grade (I, Q)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### Spartan 6

<table>
<thead>
<tr>
<th>XA</th>
<th>6</th>
<th>S</th>
<th>LX</th>
<th>LXT</th>
<th>#</th>
<th>#</th>
<th>#</th>
<th>#</th>
<th>FG</th>
<th>G</th>
<th>484</th>
<th>Q</th>
</tr>
</thead>
<tbody>
<tr>
<td>Xilinx Automotive Generation Family Sub-families LX: Logic + Transceivers Logic Cells in 1K Units Speed Grade CS: Wire-bond (.8 mm) FT: Wire-bond (1 mm) FG: Wire-bond (1 mm) G: RoHS 6/6 Package Pin Count Temperature Grade (I, Q)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

I = Tj from –40°C to +100°C; Q = Tj from –40°C to +125°C

Important: Verify all data in this document with the device data sheets found at [www.xilinx.com](http://www.xilinx.com)
# External Memory Controller Maximum Bandwidth (Mb/s)

<table>
<thead>
<tr>
<th>Core Voltage</th>
<th>XA Zynq® UltraScale+™</th>
<th>XA Zynq-7000</th>
<th>XA Spartan®-7</th>
<th>XA Kintex-7</th>
<th>XA Artix®-7</th>
<th>XA Spartan-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>-1I/Q (0.85V)</td>
<td>-1I (0.72V)</td>
<td>-1I (1.0V)</td>
<td>-1Q (1.0V)</td>
<td>-1I (1.0V)</td>
<td>-1Q (1.0V)</td>
<td>-1Q (1.0V)</td>
</tr>
<tr>
<td>PL PS PL PS</td>
<td>PL PS PL PS</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
</tr>
<tr>
<td>DDR4</td>
<td>2400 2400 2133 2400</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
</tr>
<tr>
<td>DDR3</td>
<td>2133 2133 1866 2133</td>
<td>800 1066 667 1066</td>
<td>667 667 800</td>
<td>800 800 667 800</td>
<td>800 800 667 800</td>
<td>800 800 667 800</td>
</tr>
<tr>
<td>DDR3L</td>
<td>1866 1866 1600 1866</td>
<td>667 1066 - 1066</td>
<td>667 667 800</td>
<td>800 667 N/A 800</td>
<td>800 667 N/A 800</td>
<td>800 667 N/A 800</td>
</tr>
<tr>
<td>DDR2</td>
<td>- - - -</td>
<td>- - - -</td>
<td>667 800 533 800</td>
<td>667 667 800</td>
<td>667 667 533 800</td>
<td>667 667 533 800</td>
</tr>
<tr>
<td>DDR</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- 355 - 355</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
</tr>
<tr>
<td>LPDDR4</td>
<td>- 2400 - 2400</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
</tr>
<tr>
<td>LPDDR3</td>
<td>1600 1600 1600 1600</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
</tr>
<tr>
<td>LPDDR2</td>
<td>- - - -</td>
<td>- - - -</td>
<td>533 800 400 800</td>
<td>- - - -</td>
<td>533 - - -</td>
<td>533 - - -</td>
</tr>
<tr>
<td>LPDDR</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
<td>- - - -</td>
</tr>
</tbody>
</table>

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## Internal Memory Block RAM Metrics

<table>
<thead>
<tr>
<th></th>
<th>Block RAM</th>
<th>UltraRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed grade</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>True dual-port Block RAM F_{MAX} [MHz]</strong></td>
<td>645</td>
<td>516</td>
</tr>
<tr>
<td><strong>UltraRAM F_{MAX} [MHz]</strong></td>
<td>600</td>
<td>500</td>
</tr>
</tbody>
</table>

### XA Zynq UltraScale+ FPGAs

<table>
<thead>
<tr>
<th></th>
<th>Block RAM</th>
<th>UltraRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed grade</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>-1L</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>True dual-port Block RAM F_{MAX} [MHz]</strong></td>
<td>458</td>
<td>458</td>
</tr>
</tbody>
</table>

### XA Zynq-7000 FPGAs

<table>
<thead>
<tr>
<th></th>
<th>Block RAM</th>
<th>UltraRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed grade</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>True dual-port Block RAM F_{MAX} [MHz]</strong></td>
<td>458</td>
<td>458</td>
</tr>
</tbody>
</table>

### XA Spartan-7 FPGAs

<table>
<thead>
<tr>
<th></th>
<th>Block RAM</th>
<th>UltraRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed grade</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-1</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>-2</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>True dual-port Block RAM F_{MAX} [MHz]</strong></td>
<td>388</td>
<td>461</td>
</tr>
</tbody>
</table>

### XA Spartan-6 FPGAs

<table>
<thead>
<tr>
<th></th>
<th>Block RAM</th>
<th>UltraRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Speed grade</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-2</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>-3</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>True dual-port Block RAM F_{MAX} [MHz]</strong></td>
<td>280</td>
<td>320</td>
</tr>
</tbody>
</table>
## Digital Signal Processing Metrics

<table>
<thead>
<tr>
<th>Device</th>
<th>Speed Grade</th>
<th>( F_{\text{MAX}} ) [MHz]</th>
<th>Max GMAC/s</th>
</tr>
</thead>
<tbody>
<tr>
<td>XA Zynq UltraScale+ MPSoC</td>
<td>-1, -1L</td>
<td>645, 600</td>
<td>1,362, 1,267</td>
</tr>
<tr>
<td>XA Zynq-7000 SoC</td>
<td>-1</td>
<td>547</td>
<td>438</td>
</tr>
<tr>
<td>XA Kintex-7 FPGAs</td>
<td>-1I, -1Q</td>
<td>547</td>
<td>352, 352</td>
</tr>
<tr>
<td>XA Spartan-7 FPGAs</td>
<td>-1, -2</td>
<td>464, 550</td>
<td>148, 176</td>
</tr>
<tr>
<td>XA Artix-7 FPGAs</td>
<td>-1, -2</td>
<td>464, 550</td>
<td>223, 264</td>
</tr>
<tr>
<td>XA Spartan-6 FPGAs</td>
<td>-2, -3</td>
<td>333, 390</td>
<td>120, 103 (LX75)</td>
</tr>
</tbody>
</table>

### XA Zynq UltraScale+ MPSoC
- **Speed grade**: -1, -1L
- **\( F_{\text{MAX}} \) [MHz]**: 645, 600
- **Max GMAC/s**: 1,362, 1,267

### XA Zynq-7000 SoC
- **Speed grade**: -1
- **\( F_{\text{MAX}} \) [MHz]**: 547
- **Max GMAC/s**: 438

### XA Kintex-7 FPGAs
- **Speed grade**: -1I, -1Q
- **\( F_{\text{MAX}} \) [MHz]**: 547
- **Max GMAC/s**: 352, 352

### XA Spartan-7 FPGAs
- **Speed grade**: -1, -2
- **\( F_{\text{MAX}} \) [MHz]**: 464, 550
- **Max GMAC/s**: 148, 176

### XA Artix-7 FPGAs
- **Speed grade**: -1, -2
- **\( F_{\text{MAX}} \) [MHz]**: 464, 550
- **Max GMAC/s**: 223, 264

### XA Spartan-6 FPGAs
- **Speed Grade**: -2, -3
- **\( F_{\text{MAX}} \) [MHz]**: 333, 390
- **Max GMAC/s**: 120, 103 (LX75)
References

DS894, XA Zynq UltraScale+ MPSoC Data Sheet: Overview
DS925, Zynq UltraScale+ MPSoC Data Sheet: DC and AC Switching Characteristics
DS180, 7 Series FPGAs Data Sheet: Overview
DS197, XA Artix-7 FPGAs Data Sheet: Overview
DS181, Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics
DS188, XA Zynq-7000 All Programmable SoC Data Sheet: Overview
DS187, Zynq-7000 SoC Data Sheet: DC and AC Switching Characteristics
DS175, XA Kintex-7 FPGA Data Sheet: Overview
DS189, Spartan-7 FPGAs Data Sheet: DC and AC Switching Characteristics
DS170, XA Spartan-6 Automotive FPGA Family Data Sheet: Overview
DS162, Spartan-6 FPGAs Data Sheet: DC and AC Switching Characteristics
UG1213, Zynq Migration Guide – Zynq-7000 AP SoC to Zynq UltraScale+ MPSoC Devices

For more information on Automotive products, go to https://www.xilinx.com/applications/automotive.html

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