### XA Zynq®-7000 All Programmable SoC

<table>
<thead>
<tr>
<th>Device Name</th>
<th>Z-7010</th>
<th>Z-7020</th>
<th>Z-7030</th>
</tr>
</thead>
<tbody>
<tr>
<td>Part Number</td>
<td>XA7Z010</td>
<td>XA7Z020</td>
<td>XA7Z030</td>
</tr>
</tbody>
</table>

#### Processing System
- **Processor Core**: Dual ARM® Cortex™-A9 MPCore™ with CoreSight™
- **Processor Extensions**: NEON™ & Single / Double Precision Floating Point for each processor
- **Maximum Frequency**: 667 MHz
- **L1 Cache**: 32 KB Instruction, 32 KB Data per processor
- **L2 Cache**: 512 KB
- **On-Chip Memory**: 256 KB
- **External Memory Support**: DDR3, DDR3L, DDR2, LPDDR2
- **External Static Memory Support**: 2x Quad-SPI, NAND, NOR
- **DMA Channels**: 8 (4 dedicated to Programmable Logic)
- **Peripherals**: 2x UART, 2x CAN 2.0B, 2x I2C, 2x SPI, 4x 32b GPIO
- **Peripherals w/ built-in DMA**: 2x USB 2.0 (OTG), 2x Tri-mode Gigabit Ethernet, 2x SD/SDIO
- **Security**: AES and SHA 256b Decryption and Authentication for Secure Boot

#### Programmable Logic
- **Xilinx 7 Series Programmable Logic Equivalent**
  - 28K Logic Cells (~430K) LUTs
  - 17,600
- **Flip-Flops**: 35,200
- **Extensible Block RAM (If 36 Kb Blocks)**: 240 KB (60)
- **Programmable DSP Slices (18x25 MACCs)**: 400
- **Peak DSP Performance (Symmetric FIR)**: 204 GMACs
- **Programmable Logic (Xilinx 7) User I/Os**: 32
- **Analog Mixed Signal (AMS) / XADC**: 6
- **Serial Transceivers**: 4
- **Multi-Standards and Multi-Voltage SelectIO Interfaces**: 2x 12 bit, MSPS ADCs with up to 17 Differential Inputs
- **Security**: AES and SHA 256b Decryption and Authentication for Secure Programmable Logic Configuration

#### Speed Grades
- **XA I-Grade (-40°C to 100°C)**
- **XA Q-Grade (-40°C to 125°C)**

#### Packages

<table>
<thead>
<tr>
<th>Package Type</th>
<th>CLG225(1)</th>
<th>CLG400</th>
<th>CLG400</th>
<th>CLG484</th>
<th>FBG484 / FBV484</th>
</tr>
</thead>
<tbody>
<tr>
<td>Size (mm)</td>
<td>13x13</td>
<td>17x17</td>
<td>17x17</td>
<td>19x19</td>
<td>23x23</td>
</tr>
<tr>
<td>Pitch (mm)</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>0.8</td>
<td>1.0</td>
</tr>
<tr>
<td>Processing System User I/Os (excludes DDR dedicated I/Os)(2)</td>
<td>32</td>
<td>54</td>
<td>54</td>
<td>54</td>
<td>54</td>
</tr>
<tr>
<td>Multi-Standards and Multi-Voltage SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V)</td>
<td>54</td>
<td>100</td>
<td>125</td>
<td>200</td>
<td>100</td>
</tr>
<tr>
<td>Multi-Standards and Multi-Voltage High Performance SelectIO Interfaces (1.2V, 1.35V, 1.5V, 1.8V)</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>63</td>
</tr>
<tr>
<td>Serial Transceivers</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>--</td>
<td>4</td>
</tr>
<tr>
<td>Maximum Transceiver Speed (Speed Grade Dependental)</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>NA</td>
<td>6.6 Gbps</td>
</tr>
</tbody>
</table>

Notes:
2. Security block is shared by the Processing System and the Programmable Logic.
3. Equivalent ASIC gate count is dependent on the function implemented. The assumption is 1 Logic Cell = ~15 ASIC Gates.
4. Devices in the same package are pin-to-pin compatible.
5. Static memory interface combined with the usage of many peripherals could require more than 54 I/Os. In that case, the designer can use the Programmable Logic SelectIO Interface.
6. Preliminary product information. Subject to change. Please contact your Xilinx representative for the latest information.

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