What's New in PlanAhead Software 12

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The PlanAhead™ software code includes source code for the following programs:

CenterPoint XML

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What's New in PlanAhead Software 12

This document provides an overview of the new features and functionality included in PlanAhead™ software 12.1.

This document assumes that you will upgrade to the ISE® Design Suite 12; however, if you elect to use a previous version, you will still see significant benefits in migrating to PlanAhead 12. Limited support is available for versions of ISE 10.1 and later, with specific features such as CORE Generator™ tool integration supported only in the same installation of ISE 12.

In ISE Design Suite 12, the PlanAhead software has significant enhancements to the graphical user interface, and project flows, which offer a more comprehensive design flow for Logic designer. The PlanAhead software is expanding its flow capabilities. Some PlanAhead features that are new in ISE 12.1 are optional and should not be confused with equivalent capabilities in the Project Navigator design entry and project management cockpit.

New to PlanAhead 12.1 flow are RTL development and analysis features, and CORE Generator tool integration. In future releases, Xilinx will continue to provide a comprehensive front-to-back design environment flow within PlanAhead, expanding on the key benefits it provides today. The key features include:

- I/O Pin assignment
- Design analysis and experimentation
- Floorplanning and physical constraints
- Partial reconfiguration
- Design preservation with partitions
- ChipScope Core insertion

For more information, refer to the *PlanAhead User Guide* (UG632) or contact the Xilinx® Technical Support. For contact information, visit www.xilinx.com/support.

Reference Documents

This document references the following web locations and documents:

***ISE Design Suite 12: Installation, Licensing, and Release Notes*:**

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/irn.pdf

***PlanAhead User Guide* (UG632):**

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/PlanAhead_User_Guide.pdf

***Floorplanning Methodology Guide* (UG633)**

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/Floorplanning_Methodology_Guide.pdf

***Hierarchical Design Methodology Guide* (UG748)**

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/Hierarchical_Design_Methodology_Guide.pdf

User licenses: http://www.xilinx.com/getproduct

Partial Reconfiguration User Guide: http://www.xilinx.com/tools/partial-reconfiguration

PlanAhead Tutorials:

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/planahead12-1_tutorials.htm

Device Support

PlanAhead 12 supports Virtex®-6 and Spartan®-6 device families, as well as all of the available Virtex-4, Virtex-5 and Spartan-3 FPGA devices. PlanAhead does not support any Complex Programmable Logic Devices (CPLDs).

Support for Virtex, Virtex-II, Virtex-II Pro and Spartan 2 device families was removed from the software in ISE 11.1. ISE software version 10.1 or earlier should be used to design with these devices.

As new devices are introduced they are made available in PlanAhead. It is advisable to remain current with the PlanAhead update releases using the `XilinxNotify` capabilities. Update releases are distinguished by the last digit in the release number (such as 12.2, 12.3).

PlanAhead software supports the same devices and speed files as the ISE Design Suite, with the exception of CPLDs. Refer to the *ISE Design Suite 12: Installation, Licensing, and Release Notes* for a list of supported devices.

Installation and Licensing

Xilinx software tools migrated to FlexNet-based licensing beginning with the 11.1 release. Refer to the *ISE Design Suite 12: Installation, Licensing, and Release Notes* for more information about installing the software, obtaining licenses, and configuring the license manager.

Support for Multiple ISE Installations on Windows OS

In Windows platforms, the ISE Design Suite installer was redesigned to better support the installation of multiple versions of the ISE software on Windows OS. The following subsections list the changes implemented for this effort:

Environment Variables at Install

The ISE Design Suite tools no longer set global persistent environment variables in Windows during installation. This is to allow the installation of multiple versions of the ISE software on the same machine. As a result, each application in the ISE Design Suite has implemented batch mode wrappers that set the required environment variables such as `$XILINX`, `$PATH`, and `$LD_LIBRARY_PATH`.

For PlanAhead, this is implemented in the `<installation_dir>\planAhead\bin\planAhead.bat` file. This modification requires no action on the your part; however, be aware that if you have external scripts that invoke ISE Design Suite tools and reference any of these environment variables, they will not be set by the installer. PlanAhead provides an environment variable (`XIL_PA_NO_XILINX_OVERRIDE`), which, when set to a value of 1, will not override any externally-set pointers to these variables and will revert to behavior of 11.1 and prior releases. See the *ISE Design Suite 12: Installation, Licensing, and Release Notes* for more information.

Desktop Shortcuts

The 12.1 release installer installs two desktop shortcuts:

- Project Navigator
- PlanAhead

This reduces the number of shortcuts and better supports multiple installations on the same machine.

Project File Associations

PlanAhead continues to support project file associations that are set at install time in the Windows platform. The PlanAhead file extension for project files is "`ppr`" which auto-launches PlanAhead when you double-click it from a file browser, such as Windows Explorer.

Install Image Size

The ISE Design Suite 12.1 release reduced the size of the installation image.

Updates

Incremental PlanAhead Update releases are available as full installation images using the normal ISE installation mechanisms. The `XilinxUpdate` mechanism is no longer available in the ISE Design Suite 12.

New PlanAhead Features

The PlanAhead features described in the following subsections are:

- Graphical User Interface
- Flow Navigator and View Layouts
- Project Summary
- Static Timing Analysis
- Part Selection
- RTL Projects
- CORE Generator Integration
- Hierarchical Resource Estimation
- I/O Pin Planning
- Netlist Projects
- Project Navigator Integration
- Floorplanning
- ChipScope Integration
- Hierarchical Design Features
- Tcl and Batch Scripting
- Messaging
- WebTalk
- Documentation

Graphical User Interface

In the 12 release, PlanAhead software has a redesigned Graphical User Interface (GUI) to provide a more intuitive design flow and to increase productivity. These changes include a dynamic viewing environment that comprises view layouts, which present the design and device information for the design task at hand, and distinct capabilities and viewing perspectives for design information. The redesigned GUI includes:

- Improved support for "push-button" flows
- Emphasis on an easy-to- use design environment

The improved support for pushbutton flows does not compromise control for advanced users. The GUI layouts provide a task-specific environment with views that display the device, process status, command line inputs, and access to resource utilization at each phase of the design process.

The environment layout and icons guide you to the most common tasks, and lead you through the implementation flows.

Chapters 2, "Understanding the Design Flow," and Chapter 4, "Understanding the Viewing Environment," in the *PlanAhead User Guide* (UG632) contain detailed documentation for these features.

New Project Creation Wizard

The new flows are accessible in the New Project wizard, in which you can now create four different types of projects.

These project types are:

- RTL
- Netlist
- I/O Pin Planning
- ISE Implementation Results

See Chapter 3, "Creating a Project," in the *PlanAhead User Guide* (UG632) for more information. The following subsections briefly describe the project types available in PlanAhead 12.1.

RTL

RTL projects were introduced in PlanAhead 11 with the integration of Xilinx Synthesis Technology (XST). RTL flows for PlanAhead 12.1 have improved support for management of sources and constraint files, and integration with CORE Generator. The Xilinx IP repository is now natively visible in PlanAhead, with support for creation, customization, and generation of Xilinx IP from within the PlanAhead GUI. RTL projects provide the ability to synthesize and implement projects from RTL all the way to bitstream.

Netlist

Netlist projects are the traditional and most important use of PlanAhead. These projects start with gate-level structural netlists in the form of either Electronic Design Interchange Format (EDIF) or NGC netlist files. Netlist projects provide the ability to analyze and implement a design from a post-synthesis state all the way to bitstream. Key benefits are for timing closure using floorplanning, physical constraint, and hierarchical design concepts for design preservation. Netlists generated from third party synthesis providers (such as Synopsys™ Symplify® and Mentor® Precision) should use this project type.

Pin Planning

Pin planning projects function primarily to do early assignment of I/Os for optimizing Printed Circuit Board (PCB) layout, as well as Field Programmable Gate Array (FPGA) internal design considerations. Pin planning projects typically start with no design files, comma separated value (CSV) I/O data, or Hardware Definition Language (HDL) header files. Pin assignment is of an iterative nature with flows changing through design life cycles through RTL development and design closure with post-synthesis netlists.

ISE Implementation Results

ISE implementation results projects provide a quick way to create a project and import ISE results implemented externally to the PlanAhead or the Project Navigator project framework. The project type is for heavily scripted, command-line-generated implementation results. This project type lets you import ISE results quickly, and use the design analysis and debug features of PlanAhead.

Flow Navigator and View Layouts

In PlanAhead 12.1, you can manage the design flow process from the new Flow Navigator view, located on the left side of the PlanAhead environment. The Flow Navigator includes controls to configure and launch synthesis and implementation runs, generate bitstream files, and launch programming and debug tools. It also introduces the ability to open the design at various stages of the design process to perform design analysis and constraint definition, including I/O pin planning. The Flow Navigator options are:

- Project Manager
- RTL Design (visible for RTL projects only)
- Netlist Design
- Implemented Design

Project Manager

The Project Manager environment displays by default upon opening a project, and is used to manage sources, customize IP, and view project details in the Project Summary. Project Manager does not perform design compilation, and no data is loaded into memory. A design must be open to have access to the analysis commands.

RTL Design

The RTL Design environment enables analysis of the compiled RTL design including logic exploration, resource and power estimation, Design Rule Check (DRCs), and I/O pin planning.

Netlist Design

Users familiar with PlanAhead will recognize the Netlist Design environment where pre-implementation design analysis, debug core insertion, and constraint definition is performed. You can explore various constraints sets, devices, and implementation options.

Implemented Design

The Implemented Design now loads the netlist and implementation results directly from the run directory to ensure that the viewed data represents the launched run.

In PlanAhead 12.1, you can open multiple designs simultaneously. In previous PlanAhead versions, the run results were imported using the current version of the design netlist and the constraints in-memory.

More detail and documentation of the Flow Navigator and views is available in Chapter 2, "Understanding the Design Flow," and Chapter 4, "Using the Viewing Environment," of the *PlanAhead User Guide* (UG632).

Project Summary

The Project Summary page is a summary of the current state of the design and is available when a project is opened in the Project Manager and is available in each view. The project summary contains the following information:

- Project Settings Summary: Provides the Name, Default Part, Default Family, and Top Module or Entity Name.
- Design State Summary: Such as synthesized or implemented, along with the number of errors and quick links to compilation logs reports and statements regarding the next step in the design flow.
- Compilation Settings: Includes the synthesis and implementation strategy applied to the current run. The strategy is the list of settings for each point tool that will be used for compiling the design.
- Resource Summary: Displays a summary of the design resource utilization with histograms for each instance. Tabs in the summary view are: Sources, Statistics, Pins, Children, Attributes, and Connectivity.
- Timing Summary: Displays the status of the static timing analysis results for the design.

Constraint File Handling

PlanAhead 12.1 has enhanced constraints handling in the project environment. You can reference User Constraint Files (UCFs) in other file system locations and copy those files directly into the project. You can edit the files as plain text, or modify them in-memory on physical and timing constraints.

The enhanced support for multiple constraint files uses the concept of a "Target" UC, which is the file to which PlanAhead-generated constraints are written when there are multiple files added to the project.

Users can create and manage UCF files for RTL projects and have PlanAhead pass those files to XST during synthesis. For more details on constraint file handling, see Chapter 7, "Netlist Analysis and Constraint Definition," in the *PlanAhead User Guide* (UG632).

Static Timing Analysis

The PlanAhead 12.1 started the migration toward an industry-standard constraint interface based on Synopsys Design Constraints (SDC).

PlanAhead contains a Static Timing Analysis (STA) engine that is separate from the ISE Design Suite `TRCE` engine. In prior releases, this capability was called "TimeAhead," which was replaced with the STA term, "Report Timing."

The constraints implementation and the timing reports interface are modeled after the PrimeTime STA. The STA engine is, and will continue to be, a "live" in-memory timing graph, that provides the key benefits of incremental analysis and "what-if" analysis. You can add a constraint directly in the tool, and update timing immediately, then query a custom report without re-compiling the design.

In PlanAhead 12.1, the STA engine continues to support UCF constraints while exposing the basic support for the SDC tool. The "Adoption of Synopsys Design Constraint Tcl Infrastructure" section of this document describes the SDC capabilities.

The PlanAhead software is not directly modeling routing infrastructure, The STA engine in PlanAhead 12.1 is still best suited for estimation, debug, and analysis, and cannot be considered as "sign-off." The constraint coverage for cell delays and setup and hold timing should match the trace; however, the routing delays for nets are estimate, therefore slack values will not match perfectly.

The changes for STA in the GUI are:

- Report Timing
- Slack Histogram

The *PlanAhead User Guide* (UG632) describes these features in Chapter 7, "Netlist and Constraint Definition." The following subsections briefly describe the STA engine changes.

Report Timing

A new GUI dialog box to the STA engine links to and from icons in the Flow Navigator. The dialog box replaces the previous TimeAhead interface, and allows timing reports generation for all constraints in a design, or for debugging specific paths. This dialog box models the options available in the batch-mode Tcl command for the STA engine, (the `report_timing` command).

Users can type directly into the text boxes, or further select additional helper dialog boxes to search for startpoints, endpoints, or through-points in the timing paths. These other dialog boxes provide GUI builders for the object query commands for pins, nets, cells, and clock objects, which again mirror the Tcl-equivalent SDC commands.

PlanAhead has implemented a "UCF-mode" to the dialog box, which enables a search for pin/net/port/ to report_timing to reduce unexpected UCF-style behavior from the SDC engine for those unfamiliar with SDC and the differences between UCF and PCF timing queries in TRCE and the Timing Analyzer in Project Navigator.

Slack Histogram

The PlanAhead STA engine can generate a histogram in the GUI that represents a picture of the slack of all endpoints in the design. This capability can help visualize how many endpoints in the design are failing or passing timing and by what margin, and is much more useful than an overall timing score. The STA engine calculates the slack histogram by performing timing analysis across the entire design, and calculates the slack for every endpoint. The STA engine then sorts the endpoints and put them in "buckets" that represents a range of values, and draws a graph similar to a spreadsheet that displays the distribution of endpoint slack. Each bar in the histogram is selectable, which automatically filters and displays the bar in the endpoint list, so you can perform further analysis.

Part Selection

The New Project wizard contains a new GUI element to better visualize, filter, and sort the target part for a project. The new dropdown boxes enable filtering by:

- Product
- Family
- Sub-Family
- Package
- Speed Grade
- Temperature Grade

A string-based search on the composite part name is available also.

The Part Selection dialog box provides a table of the physical resources available in each device also, allowing better visualization of the number of IO ports, block RAMs, logic cells, DSP, and high-speed transceivers available in the devices.

For more information about the part chooser, see Chapter 6, "Synthesizing the Design" in the *PlanAhead User Guide* (UG632).

RTL Projects

In PlanAhead 12.1, Xilinx continues to provide Project Navigator as the primary RTL Design entry GUI and project environment, primarily because of integration with Platform Studio and DSP tools, as well as integration with simulation engines such as ISE Simulator and Third Party simulators from Cadence, Mentor Graphics, and Synopsis.

The long-term direction for the Xilinx tool chain is the migration of the project infrastructure to the PlanAhead tool. Over time, you will see greater emphasis on PlanAhead capabilities and new features implemented in PlanAhead. RTL development capabilities for the 12 release are incremental steps along this migration path.

This release offers improved integration with floorplanning, design analysis, and I/O pin planning capabilities, as well as the ability to manage RTL and constraints more easily.

CORE Generator Integration

The CORE Generator tool is integrated into the PlanAhead 12.1 RTL development projects. The catalog of available IP from the ISE Design Suite is available in the PlanAhead environment also, and you have the ability to brows, create, customize, and generate IP directly within the environment in a manner consistent with similar capabilities in Project Navigator and the standalone CORE Generator. For more information on CORE Generator integration, see Chapter 5, "RTL and IP Design," in the *PlanAhead User Guide* (UG632).

PlanAhead can import cores configured outside PlanAhead into projects using the customization GUI from CORE Generator to configure the IP cores. There are a few key benefits to this integration besides the integration with Project Navigator and the standalone CORE Generator software.

In the PlanAhead environment, the new integration capabilities are:

- Delayed IP Core Generation of synthesized NGC to decrease design creation time
- Enhanced searching and browsing capabilities for use with the IP Catalog
- Power Estimation

The following subsections briefly describe these integration capabilities.

Delayed IP Generation

Delayed generation is available for certain IP cores, allowing the delay of the actual core synthesis by XST until the project-level synthesis runs. This enhancement addresses the limitations in standalone CORE Generator and Project Navigator, where, when a core is generated, there is no way to break up the customization and generation steps, and it can take a significant amount of time to generate cores and generate instantiation templates and wrappers, and to obtain relevant data sheets.

Enhanced Search and Browse Capabilities

The PlanAhead software environment provides an enhanced search option for the IP catalog. This includes the ability to search on any field in the catalog and to use advanced filtering. In addition, you can export the IP catalog to an Excel spreadsheet.

Power Estimation

PlanAhead provides the ability to estimate power consumption on post-elaborated RTL netlists, based upon resource estimation at the RTL level.

Hierarchical Resource Estimation

Resource estimation from the hierarchical "ROOT" down is available in PlanAhead software release 12. You can select any instance in the hierarchy tree and obtain the resource estimations.

I/O Pin Planning

PlanAhead 12 includes enhancements for the following pin planning capabilities:

- Control of UCF Mode configurations and multi-function pins
- Spartan-6 I/O Part support
- Enhanced CSV Import/Export
- Modified DRC Rules
- Show Top/Bottom view button

For more information on these capabilities, see Chapter 8, "I/O Pin Planning" in the *PlanAhead User Guide* (UG632).

The following subsections describe the enhancements to I/O pin planning.

Configuration and Multi-Function Pins

PlanAhead provides the ability to set and control the different device and configuration mode. Additionally, PlanAhead provides the ability to visualize the multi-function pins.

Spartan-6 I/O Part Compatibility

PlanAhead has added the ability to define multiple compatible parts for Spartan-6 devices. Previously, one could configure multiple parts for pin planning projects, but was prohibited from assigning unbounded I/Os.

CSV Import/Export

The CSV format for import and export of I/O assignment now aligns more with the pad CSV file exported from the ISE Design Suite tools. PlanAhead now exports all the assigned I/O standards, even those that are unchanged from device defaults.

DRC Rules

The following changes occurred in DRC and Digitally Controlled Impedance (DCI) rules:

- A new DRC check, BIIVRC, was added to check for a conflict between I/O standards in a bank and an INTERNAL_VREF constraint on the bank. Standards in a bank cannot require a VREF voltage that differs from that specified by an INTERNAL_VREF constraint for the bank. This DRC generates a message.
- A new DCI check, DCICIOSTD, was added to check that there are no conflicts related to VCCO and DCI termination of I/O. This DCI generates a message.
- The BIVRU DRC was changed from an error to a warning.
- The CRPS DRC was obsoleted because it only applied to devices that are no longer supported.

Show Top/Bottom View

In the I/O Planner, an icon is available that toggles between a top and a bottom view of the pin assignments.

Netlist Projects

Netlist Projects in PlanAhead release 12.1 contain the following changes:

- EDIF replacement of NGC
- Netlist Constraint File (NCF) Constraint support

For more information on these capabilities, see Chapter 7, "Netlist Analysis and Constraint Definition," in the *PlanAhead User Guide* (UG632). The following subsections briefly describe the Netlist changes in the 12 PlanAhead release.

EDIF Replacement of NGC

In release 12.1, PlanAhead replaces the NGC with EDIF, where previously, PlanAhead passed NGC file, unchanged, to the ISE Design Suite implementation flows. This file replacement allows PlanAhead to make modifications to the netlist to support flows such as insertion of ChipScope debugger probes on nets inside cores, and provide better support for partition and design preservation flows.

NCF Constraint Support

PlanAhead for the 12.1 release added support for NCF constraint files in the Sources tab for RTL and Netlist projects. The `ngdbuild` picks up these files automatically.

You must add the files to the project. The New Project wizard auto-discovers the NCF files and PlanAhead processes them automatically. If NCF files are not in the project, then PlanAhead does not pass the files to `ngdbuild` in the ISE flows. The tools do not silently apply them without direct user knowledge of or action.

Project Navigator Integration

Project Navigator integration continues to be the main form of interaction for design entry in the Xilinx tool chain. From Project Navigator, four processes invoke PlanAhead:

- I/O pin planning
- Pre- and post-synthesis
- Floorplanning
- Post-implementation design analysis

In release 12, these processes were updated with GUI layout changes. For more information about automatic NCF file pickup, see Chapter 15, "Using PlanAhead with Project Navigator," in the *PlanAhead User Guide* (UG632).

PlanAhead now supports passing NCF constraint files from Project Navigator to PlanAhead for block-level constraints. Project Navigator does not manage NCF files directly, but these files can contain critical timing and floorplanning constraints that were not passed to PlanAhead from Project Navigator before 12.

In the Project Navigator and ISE command-line point tool environments, NCF files are picked up automatically if they exist in the same directory as an NGC file, and the base names match exactly.

These files are added to the PlanAhead project and scoped to their respective block-level. If you do not intend for these files to be picked up automatically, they must *remove* the files from the respective project.

Floorplanning

Prior to release 12, the term "floorplan" was used to refer to a UCF file. There could be different floorplans, which allowed for experimentation with different physical constraints and different trial runs. This concept changed with the introduction of the RTL development environment. The basic capabilities are still intact, such as creation of PBlocks, AREA_GROUP constraints, and creating `LOC` and `BEL` constraints; however, the term "design" replaces "floorplan." The commonly accepted actions associated with floorplanning still apply.

A design is defined as a unique combination of the following: a synthesized netlist, a set of constraint files (a *constraint set*), and a target device. The concept of a design more accurately captures the fact that with synthesis, there can be many different synthesis trials and versions of constraints and even targeted devices as a project converges and meets design objectives.

For most users, a single constraint set is sufficient, and so in PlanAhead there a default constraint set is created and managed automatically. However, advanced users who are creating multiple runs for synthesis and implementation will notice that the Create Multiple Runs dialog box lets you launch multiple runs against a design, which is the equivalent of launching runs against different floorplans in prior releases.

The File menu has a new **Save design as** item and each of the planners have "Open design" commands which enable opening the currently active design, or creating a new one with specific synthesis results, constraint sets, and/or different target devices.

For more information about floorplanning, see Chapter 11, "Floorplanning the Design," in the *PlanAhead User Guide* (UG632).

ChipScope Integration

In 12, the changes related to ChipScope debug core insertion are:

- Port Punching in NGC Core Netlists
- CDC File integration
- BitGen Integration
- FPGA Editor Integration
- iMPACT Integration

The following subsections describe these changes. For more information on ChipScope integration, see Chapter 12, "Programming and Debugging the Design," in the *PlanAhead User Guide* (UG632).

Port Punching in NGC Core Netlists

For the 12.1 release, PlanAhead replaced binary NGC netlists with EDIF versions. You can insert debug logic and ports for ChipScope inside NGC cores.

CDC File Integration

PlanAhead provides the ability to import ChipScope Definition Core (CDC) files from the File menu. This mechanism recreates ChipScope debug insertion flows that were previously performed outside the PlanAhead environment.

Bitgen Integration

Bitgen can be accessed from Flow Navigator after implementation in the Program and Debug view.

FPGA Editor Integration

PlanAhead can launch the FPGA Editor on an implemented design run. PlanAhead invokes FPGA Editor with the routed Native Circuit Description (NCD) and PCF databases.

iMPACT Integration

PlanAhead now has the ability to launch iMPACT to perform bit file programming on devices. iMPACT can be launched on implementation runs after running BitGen, and PlanAhead passes the bit file generated from the implementation run. For more information on running iMPACT from PlanAhead, see Chapter 12, "Programming and Debugging the Design" in the *PlanAhead User Guide (UG632)*.

Hierarchical Design Features

In 12, PlanAhead provides access to two new features that are part of a Hierarchical Design methodology:

- Design preservation using partitions
- Partial reconfiguration

For more information, see Chapter 13, "Using Hierarchical Design Techniques," in the *PlanAhead User Guide* (UG632).

The following subsections briefly describe the implementation of Hierarchical Design features in PlanAhead.

Design Preservation using Partitions

In PlanAhead release 12, the Design Preservation flow is available in PlanAhead and in the ISE command-line tools, and is no longer supported in Project Navigator. The Design Preservation flow lets you implement critical portions of their design and then "preserve" them while iterating on other portions of the design, which ensures that critical logic is not disturbed by further logic development.

Partial Reconfiguration

The Partial Reconfiguration flow is licensed separately and available from PlanAhead. Partial Reconfiguration documents are located at: http://www.xilinx.com/tools/partial-reconfiguration

You can obtain a license through the Xilinx web site: http://www.xilinx.com/getproduct

Tcl and Batch Scripting

Tcl is the scripting language supported by PlanAhead and many Electronic Design Automation (EDA) tools and is an industry standard for tool flow and control.

Tcl provides the ability to query the design database dynamically, and is a powerful debug mechanism for finding design issues and for customizing tool operation. Tcl lets you automate design compilation, and the Tcl commands are coupled tightly to the constraint and flow methodologies.

The changes to Tcl and batch scripting are:

- Adoption of Synopsys Design Constraint Tcl Infrastructure
- Backward Compatibility for Tcl Scripting
- Updated Tcl Version (8.5)
- Support for SDC core commands

Chapter 14, "Tcl and Batch Scripting," of the *PlanAhead User Guide* (UG632) describes the Tcl features in PlanAhead 12.1. The following subsections describe the Tcl.

Adoption of Synopsys Design Constraint Tcl Infrastructure

In the 12 release, the Tcl infrastructure in PlanAhead changed to accommodate the long-term plans for Xilinx to migrate toward Synopsys Design Constraints (SDC) for timing constraints.

SDC is an industry standard that is based on Tcl, and the Tcl functionality in PlanAhead 12 is the first step in this migration, with significant ramifications. SDC covers timing constraints, and it is a critical query and debug tool.

Due to the tight integration of timing constraints with all portions of synthesis, place, and route flows, Xilinx changed the Tcl command infrastructure so that Tcl commands are modeled on the SDC basics.

Tcl Scripting Backward Compatibility

In release 12.1, PlanAhead implemented a deprecation layer that maps old Tcl commands to the new syntax. For most users this will be seamless and will not notice the transition, but for some custom-implemented scripts, there could be an impact.

Updated Tcl Version

In the 12.1 release, PlanAhead uses the latest available version of the Tcl interpreter, which is v8.5, from the open source community. This gives you access to the most up-to-date features available from the Tcl infrastructure.

SDC Support

The SDC support introduced in PlanAhead 12, is limited to core commands such as `get_cells`, `get_pins`, `get_nets`, and other `get_*` commands for search and query.

Messaging

PlanAhead 12.1 has improved and consolidated information, warning, and error messaging into the Console view with tabs at the bottom of the PlanAhead environment, which is active whenever messaging content is available. In prior releases, this information was not consolidated and message tabs were not present. The messaging in the Console view includes:

- Tcl Console
- Compilation Log
- Elaboration Messages
- Compilation Messages
- Reports

The following subsections briefly describe the messaging available in the Console view:

Tcl Console

Tcl Console tab contains the history of the executed Tcl commands during a session, either directly or indirectly from GUI actions. It also includes information, warning, and error messages that generated during the context of executing the command. The right of the scrollbar has color indicators the show the warning messages in yellow and error message in the history in red. You can type Tcl commands directly into text box for live execution.

Compilation Log

The Compilation Log tab contains the captured output from ISE tools: XST, ngdbuild, map, par, and trace, that appear in real-time as the tools execute in separate threads. Log file messages display in the order they were generated from the tools.

Elaboration Messages

PlanAhead invokes an Elaboration Results view upon RTL elaboration in which violations are highlighted, and where the RTL Editor invokes when you double-click on a line. You can expand, collapse, filter, and hide the messages.

Compilation Messages

The Compilation Messages tab contains ISE Design Suite tool-generated XML-based messages from CORE Generator, XST, ngdbuild, map, par, and trce. These messages are organized in a tree table by type, and are not in the exact order of occurrence. This view allows you to collapse, browse, and view messages and see the number of occurrence. The message infrastructure is the same as Project Navigator.

Reports

The Reports tab contains the standard report files generated by the ISE point tools (not the captured output of `stdout/stderr`) for XST, ngdbuild, map, par, and trce.

For more information about the PlanAhead 12.1 messaging features, see the section, "Working with the Message Viewing Area" in the *PlanAhead User Guide* (UG632).

WebTalk

PlanAhead has implemented a new "WebTalk" feature that tracks certain PlanAhead feature usage within the tool and reports back to Xilinx. Marketing can use this data to help guide the direction and priority of tool flows. This information includes usage statistics and very general information about designs without compromising any intellectual property. This information is sent to Xilinx using HTML and you can query these reports to ensure openness about the nature of information transferred. For more information, see the WebTalk section of the *ISE Design Suite 12: Installation, Licensing, and Release Notes*.

Documentation

To provide up-to-date and quality documentation, as well as to reduce the size of the install image and increase the download speed, PlanAhead documentation is longer provided in the DVD image that is shipped in the release. The install images are shipped with placeholder files that link to the documentation, and a mechanism is provided to install documentation from the Xilinx website.

The following documentation is linked in placeholder files:

- *PlanAhead User Guide* (UG632)

The following document is available on the Xilinx website:

- *Floorplanning Methodology Guide* (UG633) (previously named *PlanAhead Methodology Guide*; this document contains floorplanning-specific information.)
- *Hierarchical Design Methodology Guide* (UG748), describes the methodology for using a hierarchical design.

Tutorials

PlanAhead ships with several designs that can use as training tools to become familiar with the tool. The tutorial designs are updated to the latest Virtex®-6 based devices and the designs support the devices in the WebPack, which is applicable to all versions of the Xilinx software.

The following tutorials that use the training designs are available on the Xilinx website:

http://www.xilinx.com/support/documentation/sw_manuals/xilinx12_1/planahead12-1_tutorials.htm

- PlanAhead Tutorial: *Quick Front to Back Flow Overview* (UG673)
- PlanAhead Tutorial: *RTL Design and IP Generation with CORE Generator* (UG675)
- PlanAhead Tutorial: *I/O Pin Planning* (UG674)
- PlanAhead Tutorial: *Debugging using ChipScope* (UG677)
- PlanAhead Tutorial: *Leveraging Design Preservation for Predictable Results* (UG747)
- PlanAhead Tutorial: *Design Analysis and Floorplanning for Performance* (UG676)

Partial Reconfiguration Documentation

The following documents are available on the Xilinx web site:

http://www.xilinx.com/tools/partial-reconfiguration

- *Partial Reconfiguration User Guide* (UG702)
- *Partial Reconfiguration Flow Overview* (UG743)
- *Partial Reconfiguration with Processor Peripherals* (UG744)

You can obtain a license through Xilinx web site:

http://www.xilinx.com/getproduct

Known Issues

A list of known issues is compiled in the Answer Record (AR) link at:

http://www.xilinx.com/support/answers/34799.htm