Vivado Design Suite User Guide

Getting Started

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
07/25/12	2012.2	Initial Xilinx release.
10/16/12	2012.3	Updated graphics.

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Vivado Design Suite Overview

What is the Vivado Design Suite?

The Vivado™ Design Suite is all about improving designer productivity. This entirely new tool suite was architected to increase the overall productivity for designing, integrating, and implementing with the 28nm family of Xilinx All Programmable devices. With 28nm, Xilinx® devices are now much larger and come with a variety of new technology including Stacked Silicon Interconnect Technology, up to 28 GB high speed I/O interfaces, hardened microprocessors and peripherals, analog mixed signal, and more. With these larger and more complex devices, developers are faced with multidimensional design challenge that can prevent them from achieving faster time-to-market and increased productivity.

The Vivado Design Suite is a completely new replacement for the existing Xilinx ISE® Design Suite of tools. It replaces all of the ISE Design Suite point tools such as Project Navigator, Xilinx Synthesis Technology (XST), implementation, CORE Generator™ tool, Timing Constraints Editor, ISE Simulator (ISim), ChipScope™ Analyzer, Xilinx Power Analyzer, FPGA Editor, PlanAhead™ design tool, and SmartXplorer. All of these capabilities are now built directly into the Vivado Integrated Design Environment (IDE) leveraging a shared scalable data model.

With the Vivado Design Suite, you can accelerate design creation with High-Level Synthesis and implementation by using place and route to analytically optimize for multiple and concurrent design metrics, such as timing, congestion, total wire length, utilization and power. Built on the shared scalable data model of the Vivado Design Suite, the entire design process can be executed in memory without having to write or translate any intermediate file formats accelerating runtimes, debug and implementation while reducing memory requirements. The Vivado Design Suite provides you with up front metrics which allows for design and tool setting modifications earlier in the design processes where they have less overall schedule impact, thus reducing design iterations and accelerating productivity.

The Vivado Design Suite tools are written with a native Tcl interface. All of the commands and options available in the IDE, which is the graphical user interface, are accessible through Tcl. The Vivado Design Suite has the same tool capabilities and interface commands for both batch and IDE modes. The Vivado Design Suite also provides powerful access to the design data for reporting and configuration as well as the tool commands and options.

You can interact with Vivado Design Suite by using:

- GUI-based commands in the Vivado IDE.
- Tcl commands entered in the Tcl Console in the Vivado IDE, in the Tcl shell outside the Vivado IDE, or saved to a Tcl script file that is run either in the IDE or in the Tcl shell.
- A mix of GUI-based and Tcl commands.

A Tcl script can contain Tcl commands covering the entire design synthesis/implementation flow, including all necessary reports generated for design analysis at any point in the design flow.

Introducing the Vivado Integrated Design Environment

The Vivado Integrated Design Environment (IDE), which refers to the graphical user interface (GUI), is an evolution of the PlanAhead tool that has shipped with the ISE Design Suite beginning with version 10.1. In the current Xilinx ISE Design Suite release, there are now two executables: PlanAhead and Vivado.

- **PlanAhead Design Analysis Tool**: The PlanAhead tool is now coupled with ISE Design Suite and will include only the capabilities and features specific to designing with ISE software.
- **Vivado Design Suite**: The Vivado Design Suite executable launches the Vivado IDE which contains features specific to designing with the Vivado Design Suite and 7 series devices. The entire ISE Design Suite flow has been replaced with new Vivado Design Suite tools leveraging the PlanAhead design tool environment and framework.

The intuitive interface of the Vivado IDE is designed for new users and gives the advanced users the power they require. All of the tools and tool options are written in native Tcl; Tcl commands can be entered in the Tcl Console in the IDE or using the Tcl shell. Analysis and constraint assignment can take place throughout the design process. For example, timing or power estimations can be provided after synthesis, placement, or routing. Because the database is accessible through Tcl, changes to constraints, design configuration or tool settings can be made real time, often without forcing re-implementation.

The Vivado IDE introduces the concept of opening designs in memory. Opening a design effectively loads the design netlist at that particular stage of the design flow, assigns the constraints to the design, and applies the design to the target device. This allows you to visualize and interact with the design at each design stage, which is a new concept to many designers. The Vivado IDE enables you to open designs after register-transfer level (RTL) elaboration, synthesis, and after implementation. Changes can be made to constraints, logic or device configuration, and implementation results. Design Checkpoints can be used to save the current state of any design.

For more information about the Vivado IDE, see the *Vivado Design Suite User Guide: Using the Vivado IDE (UG893)*.

High-Level Features of the Vivado Design Suite

Industry Standards-Based Design

The Vivado Design Suite supports the following established industry design standards:

- Tcl
- AXI4, IP-XACT
- Synopsys Design Constraints (SDC)
- Verilog, VHDL, System Verilog
- System C, C, C++

The entire solution is native Tcl based, with support for SDC and Xilinx Design Constraints (XDC) formats. Broad Verilog, VHDL, and System Verilog support for synthesis enables easier FPGA adoption. Vivado High-level Synthesis (HLS) enables you to use native C, C++ or System C languages to define your logic. Using standard IP interconnect protocol, such as AXI4 and IP-XACT, enables faster and easier system-level design integration. Support for these industry standards also enables the EDA ecosystem to better support the Vivado Design Suite. Many new third-party tools are integrated with the Vivado Design Suite.

IP Design and System-Level Design Integration

The Vivado Design Suite provides an environment to configure, implement, verify, and integrate intellectual property (IP). IP can be configured and verified as a standalone module or within the context of the system-level design. IP can include logic, embedded processors, DSP modules, or C-based DSP algorithm designs. Custom IP is packaged following IP-XACT protocol and then made available through the IP Catalog. The IP Catalog provides quick access to the IP for configuration, instantiation and validation of IP. Xilinx IP utilizes the AXI4 interconnect standard to enable faster system-level integration. Existing IP can be used in the design either in RTL or netlist form. The Vivado IDE will accept ISE Design Suite IP core (`.xco` extension) files generated using a previous version of the CORE Generator™ tool.

The Vivado Design Suite is integrated with the Xilinx System Generator tool to provide a solution for implementing DSP functions. DSP modules are integrated and managed within the Vivado IDE. When you select a DSP source for edit, the System Generator launches automatically. System Generator can also be used as a standalone tool, and the resulting output files can be used as source files in the Vivado IDE.

The Vivado Design Suite is integrated with Xilinx Platform Studio (XPS) to configure and manage microprocessor cores. The cores are integrated and managed within the Vivado IDE. When you select an XPS source for edit, the XPS tool launches automatically. XPS can also be run as a standalone tool, and the resulting output files can be used as source files in the Vivado IDE.

The Vivado Design Suite is integrated with Vivado HLS to provide a solution for implementing C-based DSP functions. RTL output from the Vivado HLS is used as RTL source files in the Vivado IDE. The RTL output is packaged into IP-XACT compliant IP in the Vivado IP packager and is then available in the IP Catalog. Vivado HLS logic modules can also be used in System Generator logic to prepare DSP modules.

The IP Packager can be used to package custom Xilinx IP configurations, third-party or user IP. Packaged IP can then be displayed in the IP Catalog.

For more information, see *Vivado Design Suite User Guide: Designing with IP (UG896)*.

RTL or Netlist to Bitstream Design Flows

The Vivado Design Suite contains the following Vivado IDE features:

- Vivado synthesis
- Vivado implementation
- Vivado timing analysis
- Vivado power analysis
- Bitstream generation

These tools are designed to provide larger design capacity, increased design performance with decreased runtimes. The Vivado synthesis and implementation features are timing driven and use SDC or XDC format constraints. Various reports and analysis features are available at each stage of the design process. The design can be run though the entire flow using batch Tcl scripts, by entering Tcl commands at the Tcl shell or the IDE Tcl Console, or using the Vivado IDE. To help improve design results, you can create multiple runs to experiment with different synthesis or implementation options, timing and physical constraints, or design configuration.

The Vivado IDE leverages design projects to configure and manage the entire design process. Sources, design configuration and run results are stored and managed within the Vivado IDE project. The design status notifies you of status changes, such as, source files have been updated and run results are out-of-date. A standard set of reports, tool messages and logs are also presented within the project as well in the Tcl shell or Tcl Console for generating custom reports. Some advanced options are available for implementation, such as Vivado power optimization, Vivado physical optimizer and tool effort levels, that assist you with design closure. For more information, see the *Vivado Design Suite User Guide: Synthesis (UG901)* and the *Vivado Design Suite User Guide: Implementation (UG904)*.

Design Analysis and Verification

The Vivado IDE enables you to analyze, verify and modify the design at each stage of the design process. You can improve circuit performance by analyzing the interim results in the design process. This analysis can be run after RTL elaboration, synthesis, and implementation.

The Vivado simulator, integrated with the Vivado IDE, enables you to run behavioral and structural logic simulation at each stage of the design. The Simulator supports mixed-mode simulation, and results are displayed in an analog waveform. Third-party simulators can also be used. For more information, see *Vivado Design Suite User Guide: Logic Simulation (UG900)*.

The results can be interactively analyzed in the Vivado IDE at each stage of the design process. Some of the design and analysis features include timing analysis, power estimation and analysis, device utilization statistics, design rule checks (DRCs), I/O planning, floorplanning, and interactive placement and routing analysis, and Engineering Change Order (ECO). For more information, see the *Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)*.

After implementation, the device can be programmed and analyzed within the Vivado IDE. Debug signals can be easily identified and are processed throughout the flow. Debug cores can be configured and inserted either in RTL or in the synthesized netlist. The Vivado logic analyzer also enables hardware validation. The interface is designed to be consistent with the Vivado simulator sharing a common waveform viewer. For more information, see the *Vivado Design Suite User Guide: Programming and Debugging (UG908)*.

I/O Pin Planning and Floorplanning

The Vivado IDE provides an I/O pin planning environment that enables correct "by-construction" I/O port assignment either onto specific device package pins or onto internal die pads. You can analyze and design package and design I/O data using the views and tables available in the Vivado pin planner. For more information, see the *Vivado Design Suite User Guide: I/O and Clock Planning (UG899)*.

The Vivado IDE provides advanced floorplanning capabilities to help drive improved implementation results. These include the ability to force specified logic inside of a particular area or by interactively locking specific placement or routing for subsequent runs. For more information, see *Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)*.

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Chapter 2

Migrating Designs to the Vivado Design Suite

Overview

ISE® Design Suite is an industry-proven solution for all generations of Xilinx® devices. The Xilinx ISE Design Suite continues to bring innovations to a broad base of developers, and extends the familiar design flow for projects targeting 7 series and Zynq™-7000 devices. The current ISE Design Suite release brings innovations and contains updated device support and is available for immediate download.

The Vivado™ Design Suite supports the 7 series devices including Virtex®-7, Kintex™-7 and Artix™-7 devices, and offers enhanced tool performance, especially on large or congested designs.

Because both ISE Design Suite and Vivado Design Suite support 7 series devices, you have time to migrate tools.

RECOMMENDED: *If you start a new design for a Kintex K410 or larger device, Xilinx recommends that you contact your local Field Application Engineer to determine if Vivado Design Suite is right for your design.*

Migration considerations:

- **IP**: Existing ISE Design Suite projects and IP can be migrated to Vivado Design Suite projects and IP. The Vivado Design Suite can use ISE Design Suite IP during implementation.
- **Source files**: You can add all source files, with the exception of Schematic (SCH) and Architecture Wizard (XAW) source files, from an existing ISE Design Suite project to a new project in the Vivado Design Suite. For example, CORE Generator™ tool project files (`.xco` file extension) and netlist files (`.ngc` file extension) can be added as design sources.
- **Run results**: Run results are not migrated; however, they are generated after implementing the design in the tool.

- **Constraints**: User Constraint Format (UCF) files used for the design or IP must be converted to Xilinx Design Constraints (XDC) format for use with Vivado Design Suite. For more information about XDC, see the *Vivado Design Suite User Guide: Using Constraints (UG903)*.

CAUTION! *Do not migrate from ISE Design Suite and Vivado Design Suite in the middle of a current ISE Design Suite project because design constraints and scripts are not compatible between these environments.*

For more information about design migration, see *Vivado Design Suite Migration Methodology Guide (UG911)*.

Getting Started with the Vivado Design Suite

Installing the Vivado Design Suite

You can install the current release of both the ISE® Design Suite and the Vivado™ Design Suite at the same time from the Download Center on the Xilinx® website.

IMPORTANT: *Vivado Design Suite is available to all ISE Design Suite customers who are currently in warranty, at no additional cost.*

All current, in warranty seats of the ISE Design Suite will receive an entitlement to a copy of the current Vivado Design Suite release. If you generated your ISE Design Suite license for versions 13 or 14 *after* February 2, 2012, your current license will work for the Vivado Design Suite. If you are still in warranty but you generated a license *before* February 2, 2012, you must regenerate your license in order to use the Vivado Design Suite.

Detailed installation, licensing and release information is available in the documents listed below:

- *Xilinx Design Tools: Installation and Licensing Guide (UG798)*
- *Xilinx Design Tools: Release Notes Guide (UG631)*

Note: A WebPACK™ tool version of the Vivado Design Suite is *not* available with the current release.

Launching the Vivado Integrated Design Environment

After installing the design suite, you can launch the Vivado Integrated Design Environment (IDE), which is the graphical user interface, to create a project for your design that you run through the design flow.

Windows

To start the tool on Windows:

Select **Start > All Programs > Xilinx Design Tools > Vivado 2012.x**.

Note: You can also double-click the Vivado IDE shortcut icon on your desktop.

Figure 3-1: **Vivado Desktop Icon**

Linux

To start the tool in Linux, type the following command at the command prompt:

```
# vivado
```

Note: If you need help, type `#vivado -help`.

RECOMMENDED: *Launch the Vivado Integrated Design Environment from your working directory. This way it is easy to locate the project file, log files and journal files, which are written to the launch directory.*

For more information about the Vivado IDE, see the *Vivado Design Suite User Guide: Using the Vivado IDE (UG893)*.

Starting in the Vivado Integrated Design Environment

When you launch the Vivado Integrated Design Environment (IDE), the Getting Started page displays and provides you with options to help you begin. From this page, you can:

- Start with a Project
- Manage IP
- Review Documentation and Videos

Figure 3-2: **The Getting Started Page**

Starting with a Project

You can create or open a project, and add source files to define your design. The Getting Started Page provides links for easy access to the following start-up steps:

- Create a project
- Open example projects
- Open existing projects

If you are working with a project, you are working in *Project Mode*, which means you rely on the tool to automatically manage your design, and keep track of design file status. You can launch predefined design flow steps, and access results reports along the way.

- For more information about design entry, see the *Vivado Design Suite User Guide: System-Level Design Entry (UG895)*.
- For information about the next step in the design flow, see the *Vivado Design Suite User Guide: Design Flows Overview (UG892)*.

Managing IP

You can open the Vivado IP Catalog in which you can view and customize delivered IP. You can also open existing IP and repositories.

- For more information about design entry, see the *Vivado Design Suite User Guide: System-Level Design Entry (UG895)*.
- For information about IP, see the *Vivado Design Suite User Guide: Designing with IP (UG896)*.

Reviewing Documentation and Videos

From the Getting Started page, you can open documentation, including user guides, videos, and the release notes, in the Xilinx Documentation Navigator.

For more information about the Documentation Navigator and the Vivado Design Suite documentation, see Learning About the Vivado Design Suite.

Working with Tcl (Advanced Users)

If you prefer to work directly with Tcl, you can interact with your design using Tcl commands. Intended for the more advanced users, you can:

- Enter individual Tcl commands, in the Vivado IDE (in the Tcl Console) or in the Tcl shell outside of the IDE.
- Run Tcl scripts, either from the Vivado IDE or the Tcl shell.

For more information about using Tcl and Tcl scripting, see the *Vivado Design Suite User Guide: Using the Tcl Scripting Capabilities (UG894)*.

To use Tcl in the tool, see the *Vivado Design Suite Tutorial: Design Flows Overview (UG888)*.

Learning About the Vivado Design Suite

This appendix provides information on where to learn more about the Vivado™ Design Suite.

RECOMMENDED: *Following the Quick Take Video Tutorials and the Tool Tutorials provide a hands-on approach to learning the tool.*

Xilinx Documentation Navigator

You can view the Xilinx® tool and hardware documentation in the Xilinx Documentation Navigator or on the Xilinx website. The Documentation Navigator is integrated with the Vivado Design Suite, and it provides a catalog of Xilinx documentation and videos. To open the viewer from the Vivado Integrated Design Environment (IDE), select any documentation link on the Getting Started page or in the Help menu. Features of the Documentation Navigator include:

- **Filters**: The filters allow you to view documentation by specific document types, specific devices or other relevant categories.
- **Search**: The search feature enables you to find documentation based on the specified search terms. The search capability works for documentation both in the local repository and on the Xilinx website.
- **Quick Download**: Documentation Navigator manages downloading Xilinx documentation to your local desktop.
- **Documentation Update**: Documentation Navigator monitors and indicates when documents are updated on the Xilinx website.

RECOMMENDED: *Click **Update Catalog** to update to the latest document catalog from the Xilinx website, which ensures the latest documents and videos are available.*

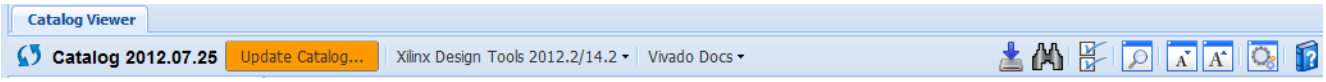

Figure 4-1: **Documentation Navigator Update Catalog Button**

Quick Take Video Tutorials

Xilinx provides a series of short training videos to help you learn to use the Vivado Integrated Design Environment (IDE). The videos focus on specific design tasks. The videos are available in the Documentation Navigator and on the Xilinx website.

Tool Tutorials

There are a variety of tutorials to help you get working in the Vivado IDE quickly. The tutorials provide step by step instructions to perform specific design tasks in the tool using small example designs. The tutorials are available in the Documentation Navigator and on the Xilinx website.

Documentation Suite

- **Vivado Design Suite User Guide**: This series of guides is categorized by design task for easy navigation to the information you need.
- **Reference Guides**: These guides provide reference information for topics, such as Tcl commands, constraints, and device libraries.
- **Methodology Guides**: These guides provide high-level guidance for performing specific design tasks, such as design migrating and large design guidance.

Installing Releases with XilinxNotify

Overview

The Vivado™ Design Suite is targeted to introduce new technology and respond to customer requests. New releases are periodically introduced. The version number reflects the release (for example: 2012.2 or 2012.3). The **Help > About Vivado** command displays the currently installed Vivado Design Suite version.

- For more information about installation, see the *Xilinx Design Tools: Installation and Licensing Guide (UG798)*.
- To download new releases and release updates, visit the Download Center on the Xilinx® website.

By default, Vivado Design Suite checks for updates upon startup, and prompts you to update to the latest version. However, if your installation is on a network location, only the machine used to install the tool automatically checks for updates from the Xilinx website, and controls tool updates.

RECOMMENDED: *Xilinx recommends that you update to the latest version of Xilinx tools.*

If your installation is not getting updates, you can either:

- Manually check for updates using XilinxNotify.
- Re-establish automatic updates using the Preferences dialog box.

Running XilinxNotify

If for any reason you are not getting update notifications, you can run XilinxNotify to check for updates. To do so:

- In the Vivado Integrated Design Environment (IDE), select **Help > Check for Updates**.
- Type `xilinxnotify` in a Linux shell

XilinxNotify performs the following activities:

- Compares the latest version of Xilinx software updates available on the Xilinx website with what you have installed, and notifies you if a newer version is available.
- Provides a **Download** button that launches a browser, allowing you to login to the Xilinx Download Center.

When you login on the Xilinx website, the product you select downloads.

IMPORTANT: *To perform a software update installation, you must have write permissions for the `$XILINX` installation directory.*

Setting Up Automatic Updates in the Preferences Dialog Box

You can set the option to check for automatic updates as follows:

1. Select **Tools > Options**.
2. In the Preferences dialog box, click **General** on the left side.
3. In the General options page, scroll down to the Miscellaneous category, and select **Automatically check xilinx.com for software updates on startup**.
4. Click **Apply**.

Now, each time you launch the tool, XilinxNotify automatically checks for updates and notifies you when one or more is found.

Appendix B

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx® Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents provide supplemental material useful with this guide:

- *Vivado™ Design Suite 2012.3 Documentation* (www.xilinx.com/support/documentation/dt_vivado_vivado2012-3.htm)
- *Xilinx Design Tools: Installation and Licensing Guide (UG798)* (www.xilinx.com/support/documentation/sw_manuals/xilinx2012_3/iil.pdf)
- *Xilinx Design Tools: Release Notes Guide (UG631)* (www.xilinx.com/support/documentation/sw_manuals/xilinx2012_3/irn.pdf)
- *Download Center on the Xilinx website* (http://www.xilinx.com/support/download/index.htm)