Vivado Design Suite User Guide

Getting Started

UG910 (v2013.1) March 20, 2013

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/20/2013	2013.1	Added information on Vivado™ IP integrator. Updated installation information to show separate installation for ISE® Design Suite and Vivado Design Suite. Removed references to the XCO file format. Added instructions for launching Vivado Design Suite using Tcl.

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Vivado Design Suite Overview

What is the Vivado Design Suite?

The Vivado™ Design Suite is designed to improve productivity. This entirely new tool suite is architected to increase the overall productivity for designing, integrating, and implementing with the 28 nanometer (nm) family of Xilinx® All Programmable devices. With 28 nm, Xilinx devices are now much larger and come with a variety of new technology, including Stacked Silicon Interconnect Technology (SSIT), up to 28 gigabyte (GB) high speed I/O interfaces, hardened microprocessors and peripherals, analog mixed signal, and more. These larger and more complex devices create multidimensional design challenges that can prevent the achievement of faster time-to-market and increased productivity.

The Vivado Design Suite replaces the existing Xilinx ISE® Design Suite of tools. It replaces all of the ISE Design Suite point tools, such as Project Navigator, Xilinx Synthesis Technology (XST), implementation, CORE Generator™ tool, Timing Constraints Editor, ISE Simulator (ISim), ChipScope™ Analyzer, Xilinx Power Analyzer, FPGA Editor, PlanAhead™ design tool, and SmartXplorer. All of these capabilities are now built directly into the Vivado Design Suite and leverage a shared scalable data model.

With the Vivado Design Suite, you can accelerate design implementation with place and route tools that analytically optimize for multiple and concurrent design metrics, such as timing, congestion, total wire length, utilization and power. Built on the shared scalable data model of the Vivado Design Suite, the entire design process can be executed in memory without having to write or translate any intermediate file formats, which accelerates runtimes, debug, and implementation while reducing memory requirements. The Vivado Design Suite provides you with design analysis capabilities at each design stage. This allows for design and tool setting modifications earlier in the design processes where they have less overall schedule impact, thus reducing design iterations and accelerating productivity.

All of the Vivado Design Suite tools are written with a native Tcl interface. All of the commands and options available in the Vivado Integrated Design Environment (IDE), which is the graphical user interface (GUI) for the Vivado Design Suite, are accessible through Tcl. The Vivado Design Suite also provides powerful access to the design data for reporting and configuration as well as the tool commands and options.

You can interact with the Vivado Design Suite using:

- GUI-based commands in the Vivado IDE
- Tcl commands entered in the Tcl Console in the Vivado IDE, in the Vivado Design Suite Tcl shell outside the Vivado IDE, or saved to a Tcl script file that is run either in the Vivado IDE or in the Vivado Design Suite Tcl shell
- A mix of GUI-based and Tcl commands

A Tcl script can contain Tcl commands covering the entire design synthesis and implementation flow, including all necessary reports generated for design analysis at any point in the design flow.

Note: This document contains information about the new Vivado IP integrator environment, which is a licensed early access feature in the 2013.1 release. Please contact your field applications engineer to obtain a license

Introducing the Vivado IDE

The Vivado IDE, which refers to the GUI, is an evolution of the PlanAhead tool that has shipped with the ISE Design Suite beginning with version 10.1.

- **PlanAhead Design Analysis Tool**: The PlanAhead tool is now coupled with ISE Design Suite and includes only the capabilities and features specific to designing with ISE software.
- **Vivado Design Suite**: The Vivado Design Suite contains features specific to designing with the Vivado Design Suite and 7 series devices. The entire ISE Design Suite flow is replaced by the new Vivado Design Suite tools and leverages the PlanAhead design tool environment and framework.

Note: The Vivado Design Suite and the ISE Design Suite, which contains the PlanAhead tool, must be installed separately. For more information, see the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)* [Ref 1] and *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)* [Ref 2].

The Vivado IDE provides new users with an intuitive interface and gives advanced users the power they require. All of the tools and tool options are written in native Tcl. Tcl commands can be entered in the Tcl Console in the Vivado IDE or using the Vivado Design Suite Tcl shell. You can run analysis and assign constraints throughout the design process. For example, the tools can provide timing or power estimations after synthesis, placement, or routing. Because the database is accessible through Tcl, you can make changes to constraints, design configuration, or tool settings in real time, often without forcing re-implementation.

The Vivado IDE introduces the concept of opening designs in memory. Opening a design effectively loads the design netlist at that particular stage of the design flow, assigns the

constraints to the design, and applies the design to the target device. This allows you to visualize and interact with the design at each design stage. The Vivado IDE enables you to open designs after register-transfer level (RTL) elaboration, synthesis, and after implementation. You can make change to constraints, logic or device configuration, and implementation results. You can also use design checkpoints to save the current state of any design.

For more information on the Vivado IDE, see the *Vivado Design Suite User Guide: Using the Vivado IDE (UG893)* [Ref 3].

High-Level Features of the Vivado Design Suite

Industry Standards-Based Design

The Vivado Design Suite supports the following established industry design standards:

- Tcl
- AXI4, IP-XACT
- Synopsys design constraints (SDC)
- Verilog, VHDL, SystemVerilog
- SystemC, C, C++

The entire solution is native Tcl based with support for SDC and Xilinx design constraints (XDC) formats. Broad Verilog, VHDL, and SystemVerilog support for synthesis enables easier FPGA adoption. Vivado High-Level Synthesis (HLS) enables you to use native C, C++ or SystemC languages to define your logic. Using standard IP interconnect protocol, such as AXI4 and IP-XACT, enables faster and easier system-level design integration. Support for these industry standards also enables the electronic design automation (EDA) ecosystem to better support the Vivado Design Suite. Many new third-party tools are integrated with the Vivado Design Suite.

IP Design and System-Level Design Integration

The Vivado Design Suite provides an environment to configure, implement, verify, and integrate intellectual property (IP). IP can be configured and verified as a standalone module or within the context of the system-level design. IP can include logic, embedded processors, digital signal processing (DSP) modules, or C-based DSP algorithm designs. Custom IP is packaged following IP-XACT protocol and then made available through the Vivado IP catalog. The IP catalog provides quick access to the IP for configuration, instantiation, and validation of IP. Xilinx IP utilizes the AXI4 interconnect standard to enable faster system-level integration. Existing IP can be used in the design either in RTL or netlist form.

The Vivado IP integrator environment enables you to stitch together various IP using the AMBA AXI4 interconnect protocol. You can interactively connect IP using a block diagram style interface and easily connect entire interfaces by drawing DRC-correct connections similar to a schematic. These IP block designs are then packaged and treated as a single design source. Block designs can be used in a design project or shared among other projects. The IP integrator is the main interface used for embedded designs using MicroBlaze™ processors or for Zynq™ devices. It is also used to integrate DSP sub-modules created with the Xilinx System Generator or HLS tools.

IMPORTANT: *The Vivado IP integrator is the replacement for Xilinx Platform Studio (XPS) for embedded processor designs, including designs targeting Zynq devices and MicroBlaze processors. XPS only supports designs targeting MicroBlaze processors, not Zynq devices. Both IP integrator and XPS are available from the Vivado IDE.*

The Vivado Design Suite is integrated with the Xilinx System Generator tool to provide a solution for implementing DSP functions. DSP modules are integrated and managed within the Vivado IDE. When you select a DSP source for edit, the System Generator launches automatically. You can also use System Generator as a standalone tool and use the resulting output files as source files in the Vivado IDE.

The Vivado Design Suite is integrated with Xilinx Platform Studio (XPS) to configure and manage MicroBlaze microprocessor cores. The cores are integrated and managed within the Vivado IDE. When you select an XPS source for edit, the XPS tool launches automatically. You can also run XPS as a standalone tool and use the resulting output files as source files in the Vivado IDE. XPS is *not* available for Zynq device designs in the Vivado IDE. Instead, use the new Vivado IP integrator environment for Zynq device designs in the Vivado IDE.

The Vivado Design Suite is integrated with Vivado HLS to provide a solution for implementing C-based DSP functions. RTL output from the Vivado HLS is used as RTL source files in the Vivado IDE. The RTL output is packaged into IP-XACT compliant IP in the Vivado IP Packager and is then available in the IP catalog. You can also use Vivado HLS logic modules in System Generator logic to prepare DSP modules. You can use the IP packager to package custom Xilinx IP configurations, third-party, or user IP. Packaged IP can then be displayed in the IP catalog.

For more information, see the *Vivado Design Suite User Guide: Designing with IP (UG896)* [Ref 4].

RTL or Netlist to Bitstream Design Flows

The Vivado Design Suite contains the following Vivado IDE features:

- Vivado synthesis
- Vivado implementation
- Vivado timing analysis
- Vivado power analysis
- Bitstream generation

These features are designed to provide larger design capacity and increased design performance with decreased runtimes. The Vivado synthesis and implementation features are timing driven and use SDC or XDC format constraints. Various reports and analysis features are available at each stage of the design process. You can run the design through the entire flow by using batch Tcl scripts, by entering Tcl commands at the Vivado Design Suite Tcl shell or the Vivado IDE Tcl Console, or by using the Vivado IDE. To help improve design results, you can create multiple runs to experiment with different synthesis or implementation options, timing and physical constraints, or design configuration.

The Vivado IDE leverages design projects to configure and manage the entire design process. Sources, design configuration, and run results are stored and managed within the Vivado IDE project. The design status notifies you of status changes, such as when source files have been updated and run results are out-of-date. The Vivado IDE generates and displays a standard set of reports, tool messages, and logs. Some advanced options are available for implementation, such as Vivado power optimization, Vivado physical optimizer, and run strategies, which assist you with design closure. For more information, see the *Vivado Design Suite User Guide: Design Flows Overview (UG892)* [Ref 5], *Vivado Design Suite User Guide: Synthesis (UG901)* [Ref 6] and the *Vivado Design Suite User Guide: Implementation (UG904)* [Ref 7].

Design Analysis and Verification

The Vivado IDE enables you to analyze, verify and modify the design at each stage of the design process. You can improve circuit performance by analyzing the interim results during the design process. This analysis can be run after RTL elaboration, synthesis, and implementation.

The Vivado simulator, integrated with the Vivado IDE, enables you to run behavioral and structural logic simulation at each stage of the design. The simulator supports Verilog, SystemVerilog, and VHDL mixed-mode simulation, and results are displayed in a waveform viewer. Third-party simulators can also be used. For more information, see the *Vivado Design Suite User Guide: Logic Simulation (UG900)* [Ref 8].

The results can be interactively analyzed in the Vivado IDE at each stage of the design process. Some of the design and analysis features include timing analysis, power estimation

and analysis, device utilization statistics, design rule checks (DRCs), I/O planning, floorplanning, and interactive placement and routing analysis. For more information, see the *Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)* [Ref 9].

After implementation, the device can be programmed and then analyzed within the Vivado lab tools environment. Debug signals can be easily identified in RTL or after synthesis and are processed throughout the flow. Debug cores can be configured and inserted either in RTL or in the synthesized netlist. The Vivado logic analyzer also enables hardware validation. The interface is designed to be consistent with the Vivado simulator, sharing a common waveform viewer. For more information, see the *Vivado Design Suite User Guide: Programming and Debugging (UG908)* [Ref 10].

I/O Pin Planning and Floorplanning

The Vivado IDE provides an I/O pin planning environment that enables I/O port assignment either onto specific device package pins or onto internal die pads. You can analyze the device and design-related I/O data using the views and tables available in the Vivado pin planner. For more information, see the *Vivado Design Suite User Guide: I/O and Clock Planning (UG899)* [Ref 11].

The Vivado IDE provides advanced floorplanning capabilities to help drive improved implementation results. These include the ability to force specified logic inside of a particular area or by interactively locking specific placement or routing for subsequent runs. For more information, see the *Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)* [Ref 9].

Migrating Designs to the Vivado Design Suite

Overview

The Xilinx® ISE® Design Suite supports projects targeting all generations of Xilinx devices, including 7 series and Zynq™-7000 devices. The Vivado™ Design Suite supports the 7 series devices, including Virtex®-7, Kintex™-7 and Artix™-7, and Zynq™-7000 devices, and offers enhanced tool performance, especially on large or congested designs.

Because both ISE Design Suite and Vivado Design Suite support 7 series devices, you have the opportunity to migrate tools. For detailed information on design migration, see the *Vivado Design Suite Migration Methodology Guide (UG911)* [Ref 12].

Migration Considerations

When migrating, consider the following:

- **IP**: You can migrate existing ISE Design Suite projects and IP to Vivado Design Suite projects and IP. The Vivado Design Suite can use ISE Design Suite IP during implementation. However, updating to the latest Vivado Design Suite native IP is highly recommended.
- **Source files**: You can add ISE Design Suite source files from an existing ISE Design Suite project to a new project in the Vivado Design Suite. For example, CORE Generator™ tool netlist files (NGC) can be added as design sources.

  Note: ISE Design Suite Schematic (SCH) and Architecture Wizard (XAW) source files are *not* supported in the Vivado Design Suite.

- **Run results**: Run results are not migrated. However, new run results are generated after implementing the design in the Vivado tools.
- **Constraints**: User constraint format (UCF) files used for the design or IP must be converted to Xilinx design constraints (XDC) format for use with Vivado Design Suite. For information on migrating UCF constraints to XDC, see the *Vivado Design Suite Migration Methodology Guide (UG911)* [Ref 12]. For more information about XDC, see the *Vivado Design Suite User Guide: Using Constraints (UG903)* [Ref 13].

CAUTION! *Do not migrate from ISE Design Suite to Vivado Design Suite while in the middle of an in-progress ISE Design Suite project, because design constraints and scripts are not compatible between these environments. Instead, start a new design using the Vivado Design Suite.*

Getting Started with the Vivado Design Suite

Installing the Vivado Design Suite

The ISE® Design Suite and the Vivado™ Design Suite are now released separately and must be installed separately. Both suites are available from the Download Center on the Xilinx® website [Ref 14].

IMPORTANT: *The Vivado Design Suite is available to all ISE Design Suite customers who are currently in warranty, at no additional cost.*

All current, in warranty seats of the ISE Design Suite will receive an entitlement to a copy of the current Vivado Design Suite release. If you generated your ISE Design Suite license for versions 13 or 14 *after* February 2, 2012, your current license will work for the Vivado Design Suite. If you are still in warranty but you generated a license *before* February 2, 2012, you must regenerate your license in order to use the Vivado Design Suite.

Detailed installation, licensing and release information is available in the following documents:

- *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)* [Ref 1]
- *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)* [Ref 2]

Launching the Vivado Design Suite

You can launch the Vivado Design Suite and run the tools using different methods depending on your preference. For example, you can choose a Tcl script-based compilation style method in which you manage sources and the design process yourself, also known as *Non-Project Mode*. Alternatively, you can use a project-based method to automatically manage your design process and design data using projects and project states, also known as *Project Mode*. Either of these methods can be run using a Tcl scripted batch mode or run interactively in the Vivado IDE. For more information on the different design flow modes, see the *Vivado Design Suite User Guide: Design Flows Overview (UG892)* [Ref 5].

Working with Tcl

If you prefer to work directly with Tcl, you can interact with your design using Tcl commands using either of the following methods:

- Enter individual Tcl commands in the Vivado Design Suite Tcl shell outside of the Vivado IDE.
- Enter individual Tcl commands in the Tcl Console at the bottom of the Vivado IDE.
- Run Tcl scripts from the Vivado Design Suite Tcl shell.
- Run Tcl scripts from the Vivado IDE.

For more information about using Tcl and Tcl scripting, see the *Vivado Design Suite User Guide: Using Tcl Scripting (UG894)* [Ref 15]. For a step-by-step tutorial that shows how to use Tcl in the Vivado tool, see the *Vivado Design Suite Tutorial: Design Flows Overview (UG888)* [Ref 16].

Launching the Vivado Design Suite Tcl Shell

Use the following command to invoke the Vivado Design Suite Tcl shell either at the Linux command prompt or within a Windows Command Prompt window:

```
vivado -mode tcl
```

Note: On Windows, you can also select **Start > All Programs > Xilinx Design Tools > Vivado 2013.x > Vivado 2013.x Tcl Shell**.

Launching the Vivado Tools Using a Batch Tcl Script

You can use the Vivado tools in batch mode by supplying a Tcl script when invoking the tool. Use the following command either at the Linux command prompt or within a Windows Command Prompt window:

```
vivado -mode batch -source <your_Tcl_script>
```

Note: When working in batch mode, the Vivado tools exit after running the specified script.

Working with the Vivado IDE

If you prefer to work in a GUI, you can launch the Vivado IDE from Windows or Linux. For more information on the Vivado IDE, see the *Vivado Design Suite User Guide: Using the Vivado IDE (UG893)* [Ref 3].

RECOMMENDED: *Launch the Vivado IDE from your working directory. This makes it easier to locate the project file, log files, and journal files, which are written to the launch directory.*

Launching the Vivado IDE on Windows

Select **Start > All Programs > Xilinx Design Tools > Vivado 2013.x > Vivado 2013.x**.

Note: You can also double-click the Vivado IDE shortcut icon on your desktop.

Figure 3-1: **Vivado IDE Desktop Icon**

Launching the Vivado IDE from the Command Line on Windows or Linux

Enter the following command at the command prompt:

```
vivado
```

Note: When you enter this command, it automatically runs `vivado -mode gui` to launch the Vivado IDE. If you need help, type `vivado -help`.

Launching the Vivado IDE from the Vivado Design Suite Tcl Shell

Enter the following command at the Tcl command prompt:

```
start_gui
```

Using the Vivado IDE

When you launch the Vivado IDE, the Getting Started page displays and provides you with options to help you begin. From this page, you can:

- Start with a project
- Manage IP
- Review documentation and videos

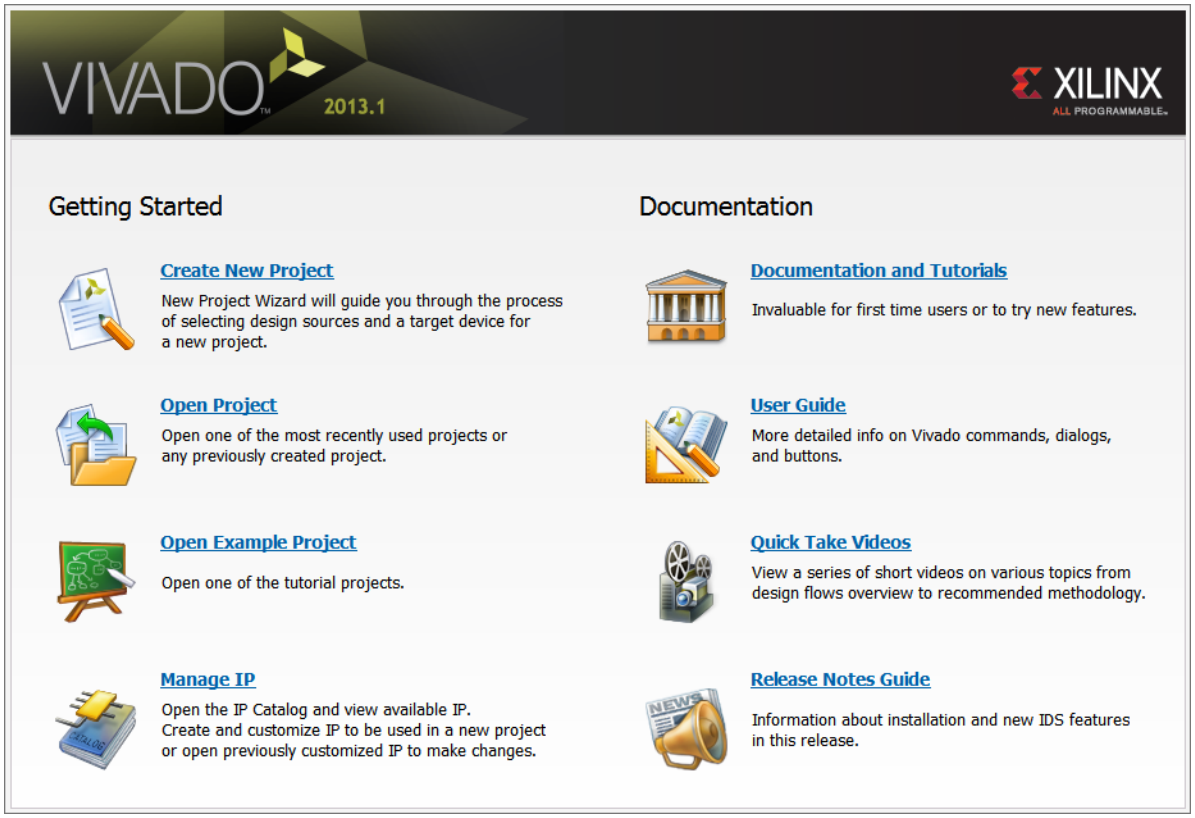

Figure 3-2: **Vivado IDE Getting Started Page**

Starting with a Project

You can create or open a project, and add source files to define your design. The Getting Started Page provides links for easy access to the following start-up steps:

- Create a project
- Open example projects
- Open existing projects

If you are working with a project, the tool automatically manages your design and keeps track of design file status. You can launch predefined design flow steps, and access results reports along the way.

For more information on design entry, see the *Vivado Design Suite User Guide: System-Level Design Entry (UG895)* [Ref 17]. For information on the next steps in the design flow, see the *Vivado Design Suite User Guide: Design Flows Overview (UG892)* [Ref 5].

Managing IP

You can open the Vivado IP catalog in which you can view and customize delivered IP. You can also open existing IP and repositories.

For more information on design entry, see the *Vivado Design Suite User Guide: System-Level Design Entry (UG895)* [Ref 17]. For information on IP, see the *Vivado Design Suite User Guide: Designing with IP (UG896)* [Ref 4].

Reviewing Documentation and Videos

From the Getting Started page, you can open documentation, including user guides, tutorials, videos, and the release notes, in the Xilinx Documentation Navigator.

For more information on the Documentation Navigator and the Vivado Design Suite documentation, see Chapter 4, Learning About the Vivado Design Suite.

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Chapter 4

Learning About the Vivado Design Suite

Overview

This chapter provides information on where to learn more about the Vivado™ Design Suite.

RECOMMENDED: *For a hands-on approach to learning the tool, follow the Quick Take Video Tutorials and the Tool Tutorials.*

Xilinx Documentation Navigator

You can view the Xilinx® tool and hardware documentation in the Xilinx Documentation Navigator or on the Xilinx website. The Documentation Navigator is integrated with the Vivado Design Suite, and it provides a catalog of Xilinx documentation and videos. To open the viewer from the Vivado IDE, select any documentation link on the Getting Started page or in the Help menu. Features of the Documentation Navigator include:

- **Filters**: The filters allow you to view documentation by specific document types, specific devices, or other relevant categories.
- **Search**: The search feature enables you to find documentation based on the specified search terms. The search capability works for documentation both in the local repository and on the Xilinx website.
- **Quick Download**: Documentation Navigator manages downloading Xilinx documentation to your local desktop.
- **Documentation Update**: Documentation Navigator monitors and indicates when documents are updated on the Xilinx website.

RECOMMENDED: *Click the **Update Catalog** button at the top of the Documentation Navigator to update to the latest document catalog from the Xilinx website. This ensures the latest documents and videos are available.*

Quick Take Video Tutorials

Xilinx provides a series of short training videos that focus on specific design tasks to help you learn to use the Vivado IDE. The videos are available in the Documentation Navigator, from the Vivado Design Suite Video Tutorials page [Ref 18] on the Xilinx website, and on YouTube.

Tool Tutorials

There are a variety of step-by-step software tool tutorials to help you get working in the Vivado IDE quickly. The tutorials provide step by step instructions to perform specific design tasks in the tool using small example designs. The tutorials are available in the Documentation Navigator and from the Vivado Design Suite Tutorials page [Ref 19] on the Xilinx website.

Documentation Suite

- **Vivado Design Suite User Guide**: These guides are categorized by design task for easy navigation to the information you need. They are available from the Vivado Design Suite User Guides page [Ref 20] on the Xilinx website.
- **Reference Guides**: These guides provide reference information for topics, such as Tcl commands, constraints, and device libraries. They are available from the Vivado Design Suite Reference Guides page [Ref 21] on the Xilinx website.
- **Methodology Guides**: These guides provide high-level guidance for performing specific design tasks, such as design migrating and large design guidance. They are available from the Vivado Design Suite Methodology Guides page [Ref 22] on the Xilinx website.

Installing Releases with XilinxNotify

Overview

The Vivado™ Design Suite is targeted to introduce new technology and respond to customer requests. New releases are periodically introduced. The version number reflects the release (for example: 2013.1). The **Help > About Vivado** command displays the currently installed Vivado Design Suite version.

By default, Vivado Design Suite checks for updates upon startup, and prompts you to update to the latest version. However, if your installation is on a network location, only the machine used to install the tool automatically checks for updates from the Xilinx website and controls tool updates.

RECOMMENDED: *Xilinx recommends that you update to the latest version of Xilinx tools.*

If your installation is not getting updates, you can either:

- Manually check for updates using XilinxNotify.
- Re-establish automatic updates using the Preferences dialog box.

For more information, see the following resources:

- For information on installation, see the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)* [Ref 1].
- To download new releases and release updates, visit the Download Center on the Xilinx® website [Ref 14].

Running XilinxNotify

If for any reason you are not getting update notifications, you can run XilinxNotify to check for updates using either of the following methods:

- In the Vivado IDE, select **Help > Check for Updates**.
- In a Linux shell, type `xilinxnotify`.

XilinxNotify performs the following activities:

- Compares the latest version of Xilinx software updates available on the Xilinx website with your installation, and notifies you if a newer version is available.
- Provides a **Download** button that launches a browser, allowing you to login to the Download Center on the Xilinx website [Ref 14].

  When you login on the Xilinx website, the product you select downloads.

IMPORTANT: *To perform a software update installation, you must have write permissions for the `$XILINX` installation directory.*

Setting Up Automatic Updates in the Preferences Dialog Box

In the Vivado IDE, you can set the option to check for automatic updates as follows:

1. Select **Tools > Options**.
2. In the Preferences dialog box, click **General** on the left side.
3. In the General options page, scroll down to the Miscellaneous category, and select **Automatically check xilinx.com for software updates on startup**.
4. Click **Apply**.

Now, each time you launch the tool, XilinxNotify automatically checks for updates and notifies you when one or more is found.

Appendix B

Additional Resources

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see the Xilinx® Support website at:

www.xilinx.com/support.

For a glossary of technical terms used in Xilinx documentation, see:

www.xilinx.com/company/terms.htm.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents provide supplemental material useful with this guide:

1. *Vivado™ Design Suite User Guide: Release Notes, Installation, and Licensing (UG973)*
2. *ISE Design Suite 14: Release Notes, Installation, and Licensing (UG631)*
3. *Vivado Design Suite User Guide: Using the Vivado IDE (UG893)*
4. *Vivado Design Suite User Guide: Designing with IP (UG896)*
5. *Vivado Design Suite User Guide: Design Flows Overview (UG892)*
6. *Vivado Design Suite User Guide: Synthesis (UG901)*
7. *Vivado Design Suite User Guide: Implementation (UG904)*
8. *Vivado Design Suite User Guide: Logic Simulation (UG900)*

9. *Vivado Design Suite User Guide: Design Analysis and Closure Techniques (UG906)*
10. *Vivado Design Suite User Guide: Programming and Debugging (UG908)*
11. *Vivado Design Suite User Guide: I/O and Clock Planning (UG899)*
12. *Vivado Design Suite Migration Methodology Guide (UG911)*
13. *Vivado Design Suite User Guide: Using Constraints (UG903)*
14. *Download Center on the Xilinx website* (http://www.xilinx.com/support/download/index.htm)
15. *Vivado Design Suite User Guide: Using Tcl Scripting (UG894)*
16. *Vivado Design Suite Tutorial: Design Flows Overview (UG888)*
17. *Vivado Design Suite User Guide: System-Level Design Entry (UG895)*
18. *Vivado Design Suite Video Tutorials* (http://www.xilinx.com/training/vivado/index.htm)
19. *Vivado Design Suite Tutorials* (http://www.xilinx.com/support/documentation/dt_vivado2013-1_tutorials.htm)
20. *Vivado Design Suite User Guides* (http://www.xilinx.com/support/documentation/dt_vivado2013-1_userguides.htm)
21. *Vivado Design Suite Reference Guides* (http://www.xilinx.com/support/documentation/dt_vivado2013-1_referenceguides.htm)
22. *Vivado Design Suite Methodology Guides* (http://www.xilinx.com/support/documentation/dt_vivado2013-1_methodologyguides.htm)
23. *Vivado Design Suite 2013.1 Documentation* (www.xilinx.com/support/documentation/dt_vivado2013-1.htm)