Vivado Design Suite User Guide

Getting Started

UG910 (v2014.1) April 2, 2014

This document applies to the following software versions: Vivado Design Suite 2014.1 and 2014.2.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/02/2014	2014.1	Added references to UltraScale™ devices throughout. Added reference to *Vivado Design Suite User Guide: Design Analysis and Closure Techniques* (UG906) in Chapter 1, Vivado Design Suite Overview. Removed reference to CORE Generator tool in Chapter 2, Migrating Designs to the Vivado Design Suite. Added information about customizing the installation and using the Xilinx Information Center in Installing the Vivado Design Suite, added reference to Vivado Design Suite QuickTake Video: Design Flows Overview in Launching the Vivado Design Suite, added tip about Start In field to Launching the Vivado IDE on Windows, updated Starting with a Project, added Opening the Hardware Manager, and added Accessing the Tcl Store in Chapter 3, Getting Started with the Vivado Design Suite. Added information about accessing Xilinx Documentation Navigator and the UltraFast Design Methodology Checklist in Xilinx Documentation Navigator in Chapter 4, Learning About the Vivado Design Suite. Removed Appendix A, Installing Releases with XilinxNotify. Updated Figure 3-2.

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Chapter 1

Vivado Design Suite Overview

What is the Vivado Design Suite?

The Vivado® Design Suite is designed to improve productivity. This entirely new tool suite is architected to increase the overall productivity for designing, integrating, and implementing with the Xilinx® 7 series, Zynq®-7000 All Programmable, and UltraScale™ devices. Xilinx devices are now much larger and come with a variety of new technology, including stacked silicon interconnect (SSI) technology, up to 28 gigabyte (GB) high speed I/O interfaces, hardened microprocessors and peripherals, analog mixed signal, and more. These larger and more complex devices create multidimensional design challenges that can prevent the achievement of faster time-to-market and increased productivity.

The Vivado Design Suite replaces the existing Xilinx ISE® Design Suite of tools. It replaces all of the ISE Design Suite point tools, such as Project Navigator, Xilinx Synthesis Technology (XST), implementation, CORE Generator™ tool, Timing Constraints Editor, ISE Simulator (ISim), ChipScope™ Analyzer, Xilinx Power Analyzer, FPGA Editor, PlanAhead™ design tool, and SmartXplorer. All of these capabilities are now built directly into the Vivado Design Suite and leverage a shared scalable data model.

With the Vivado Design Suite, you can accelerate design implementation with place and route tools that analytically optimize for multiple and concurrent design metrics, such as timing, congestion, total wire length, utilization and power. Built on the shared scalable data model of the Vivado Design Suite, the entire design process can be executed in memory without having to write or translate any intermediate file formats, which accelerates runtimes, debug, and implementation while reducing memory requirements. The Vivado Design Suite provides you with design analysis capabilities at each design stage. This allows for design and tool setting modifications earlier in the design processes where they have less overall schedule impact, thus reducing design iterations and accelerating productivity.

All of the Vivado Design Suite tools are written with a native tool command language (Tcl) interface. All of the commands and options available in the Vivado Integrated Design Environment (IDE), which is the graphical user interface (GUI) for the Vivado Design Suite, are accessible through Tcl. The Vivado Design Suite also provides powerful access to the design data for reporting and configuration as well as the tool commands and options.

You can interact with the Vivado Design Suite using:

- GUI-based commands in the Vivado IDE
- Tcl commands entered in the Tcl Console in the Vivado IDE, in the Vivado Design Suite Tcl shell outside the Vivado IDE, or saved to a Tcl script file that is run either in the Vivado IDE or in the Vivado Design Suite Tcl shell
- A mix of GUI-based and Tcl commands

A Tcl script can contain Tcl commands covering the entire design synthesis and implementation flow, including all necessary reports generated for design analysis at any point in the design flow.

Introducing the Vivado IDE

The Vivado IDE, which refers to the GUI, is an evolution of the PlanAhead tool that has shipped with the ISE Design Suite beginning with version 10.1.

- **PlanAhead Design Analysis Tool**: The PlanAhead tool is now coupled with ISE Design Suite and includes only the capabilities and features specific to designing with ISE software.
- **Vivado Design Suite**: The Vivado Design Suite contains features specific to designing with the Vivado Design Suite and 7 series, Zynq, and UltraScale devices. The entire ISE Design Suite flow is replaced by the new Vivado Design Suite tools and leverages the PlanAhead design tool environment and framework.

Note: The Vivado Design Suite and the ISE Design Suite, which contains the PlanAhead tool, must be installed separately. For more information, see the *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973) [Ref 1] and *ISE Design Suite 14: Release Notes, Installation, and Licensing* (UG631) [Ref 2].

The Vivado IDE provides new users with an intuitive interface and gives advanced users the power they require. All of the tools and tool options are written in native Tcl. Tcl commands can be entered in the Tcl Console in the Vivado IDE or using the Vivado Design Suite Tcl shell. You can run analysis and assign constraints throughout the design process. For example, the tools can provide timing or power estimations after synthesis, placement, or routing. Because the database is accessible through Tcl, you can make changes to constraints, design configuration, or tool settings in real time, often without forcing re-implementation.

The Vivado IDE introduces the concept of opening designs in memory. Opening a design effectively loads the design netlist at that particular stage of the design flow, assigns the constraints to the design, and applies the design to the target device. This allows you to visualize and interact with the design at each design stage. The Vivado IDE enables you to open designs after register-transfer level (RTL) elaboration, synthesis, and implementation. You can make change to constraints, logic or device configuration, and implementation results. You can also use design checkpoints to save the current state of any design.

For more information on the Vivado IDE, see the *Vivado Design Suite User Guide: Using the Vivado IDE* (UG893) [Ref 3]. For more information on analyzing designs, see the *Vivado Design Suite User Guide: Design Analysis and Closure Techniques* (UG906) [Ref 4].

Chapter 2

Migrating Designs to the Vivado Design Suite

Overview

The Xilinx® ISE® Design Suite supports projects targeting all generations of Xilinx devices, including 7 series and Zynq® devices. The Vivado® Design Suite supports 7 series, Zynq, and UltraScale™ devices and offers enhanced tool performance, especially on large or congested designs.

Because both ISE Design Suite and Vivado Design Suite support 7 series devices, you have the opportunity to migrate tools. For detailed information on design migration, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 5].

Migration Considerations

When migrating, consider the following:

- **IP**: You can migrate existing ISE Design Suite projects and IP to Vivado Design Suite projects and IP. The Vivado Design Suite can use ISE Design Suite IP during implementation. However, updating to the latest Vivado Design Suite native IP is highly recommended to leverage the latest IP updates and to use proper constraints.

  Note: The Vivado Design Suite is tested and validated with Vivado Design Suite IP only.

- **Source files**: You can add ISE Design Suite source files from an existing ISE Design Suite project to a new project in the Vivado Design Suite.

  Note: ISE Design Suite schematic (SCH) and Architecture Wizard (XAW) source files are *not* supported in the Vivado Design Suite.

- **Run results**: Run results are not migrated. However, new run results are generated after implementing the design in the Vivado tools.
- **Constraints**: User constraint format (UCF) files used for the design must be converted to Xilinx design constraints (XDC) format for use with Vivado Design Suite. For information on migrating UCF constraints to XDC, see the *ISE to Vivado Design Suite Migration Guide* (UG911) [Ref 5]. For more information about XDC, see the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 6].

CAUTION! *Do not migrate from ISE Design Suite to Vivado Design Suite while in the middle of an in-progress ISE Design Suite project, because design constraints and scripts are not compatible between these environments. Instead, start a new design using the Vivado Design Suite.*

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Chapter 3

Getting Started with the Vivado Design Suite

Installing the Vivado Design Suite

The ISE® Design Suite and the Vivado® Design Suite are now released separately and must be installed separately. Both suites are available from the Downloads page on the Xilinx® website [Ref 7].

IMPORTANT: *The Vivado Design Suite is available to all ISE Design Suite customers who are currently in warranty, at no additional cost.*

All current, in-warranty seats of the ISE Design Suite will receive an entitlement to the current Vivado Design Suite release. All current, in-warranty seats of the Vivado Design Suite will receive an entitlement to the equivalent ISE Design Suite edition. Generating a Vivado Design Suite license or generating an ISE Design Suite license for versions 13 or 14 will include license features for both design suites.

You can customize the Vivado Design Suite installation based on the tools and data you require. In addition, you can customize by installing only certain Xilinx device families, such as the Kintex® or Artix® device families.

RECOMMENDED: *The example designs provided with the Vivado Design Suite use specific devices from different device families. When using an example design or running a Vivado Design Suite tutorial, be sure to select a design that uses a device from one of the device families you installed.*

Detailed installation, licensing and release information is available in the following documents:

- *Vivado Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973) [Ref 1]

  Note: This document includes detailed information on the Xilinx Information Center, which periodically checks for new releases and updates from Xilinx and is the replacement for XilinxNotify.

- *ISE Design Suite 14: Release Notes, Installation, and Licensing* (UG631) [Ref 2]

Launching the Vivado Design Suite

You can launch the Vivado Design Suite and run the tools using different methods depending on your preference. For example, you can choose a Tcl script-based compilation style method in which you manage sources and the design process yourself, also known as *Non-Project Mode*. Alternatively, you can use a project-based method to automatically manage your design process and design data using projects and project states, also known as *Project Mode*. Either of these methods can be run using a Tcl scripted batch mode or run interactively in the Vivado IDE. For more information on the different design flow modes, see the *Vivado Design Suite User Guide: Design Flows Overview* (UG892) [Ref 8].

VIDEO: *For more information on design flows, see the* Vivado Design Suite QuickTake Video: Design Flows Overview.

Working with Tcl

If you prefer to work directly with Tcl, you can interact with your design using Tcl commands using either of the following methods:

- Enter individual Tcl commands in the Vivado Design Suite Tcl shell outside of the Vivado IDE.
- Enter individual Tcl commands in the Tcl Console at the bottom of the Vivado IDE.
- Run Tcl scripts from the Vivado Design Suite Tcl shell.
- Run Tcl scripts from the Vivado IDE.

For more information about using Tcl and Tcl scripting, see the *Vivado Design Suite User Guide: Using Tcl Scripting* (UG894) [Ref 9]. For a step-by-step tutorial that shows how to use Tcl in the Vivado tools, see the *Vivado Design Suite Tutorial: Design Flows Overview* (UG888) [Ref 10].

Launching the Vivado Design Suite Tcl Shell

Use the following command to invoke the Vivado Design Suite Tcl shell either at the Linux command prompt or within a Windows Command Prompt window:

```
vivado -mode tcl
```

Note: On Windows, you can also select **Start > All Programs > Xilinx Design Tools > Vivado 2014.x > Vivado 2014.x Tcl Shell**.

Launching the Vivado Tools Using a Batch Tcl Script

You can use the Vivado tools in batch mode by supplying a Tcl script when invoking the tool. Use the following command either at the Linux command prompt or within a Windows Command Prompt window:

```
vivado -mode batch -source <your_Tcl_script>
```

Note: When working in batch mode, the Vivado tools exit after running the specified script.

Working with the Vivado IDE

If you prefer to work in a GUI, you can launch the Vivado IDE from Windows or Linux. For more information on the Vivado IDE, see the *Vivado Design Suite User Guide: Using the Vivado IDE* (UG893) [Ref 3].

RECOMMENDED: *Launch the Vivado IDE from your working directory. This makes it easier to locate the project file, log files, and journal files, which are written to the launch directory.*

Launching the Vivado IDE on Windows

Select **Start > All Programs > Xilinx Design Tools > Vivado 2014.x > Vivado 2014.x**.

Note: You can also double-click the Vivado IDE shortcut icon on your desktop.

Figure 3-1: **Vivado IDE Desktop Icon**

TIP: *You can right-click the Vivado IDE shortcut icon, and select **Properties** to update the Start In field. This makes it easier to locate the project file, log files, and journal files, which are written to the launch directory.*

Launching the Vivado IDE from the Command Line on Windows or Linux

Enter the following command at the command prompt:

```
vivado
```

Note: When you enter this command, it automatically runs `vivado -mode gui` to launch the Vivado IDE. If you need help, type `vivado -help`.

Launching the Vivado IDE from the Vivado Design Suite Tcl Shell

Enter the following command at the Tcl command prompt:

```
start_gui
```

Using the Vivado IDE

When you launch the Vivado IDE, the Getting Started page (Figure 3-2) displays and provides you with different options to help you begin working with the Vivado Design Suite.

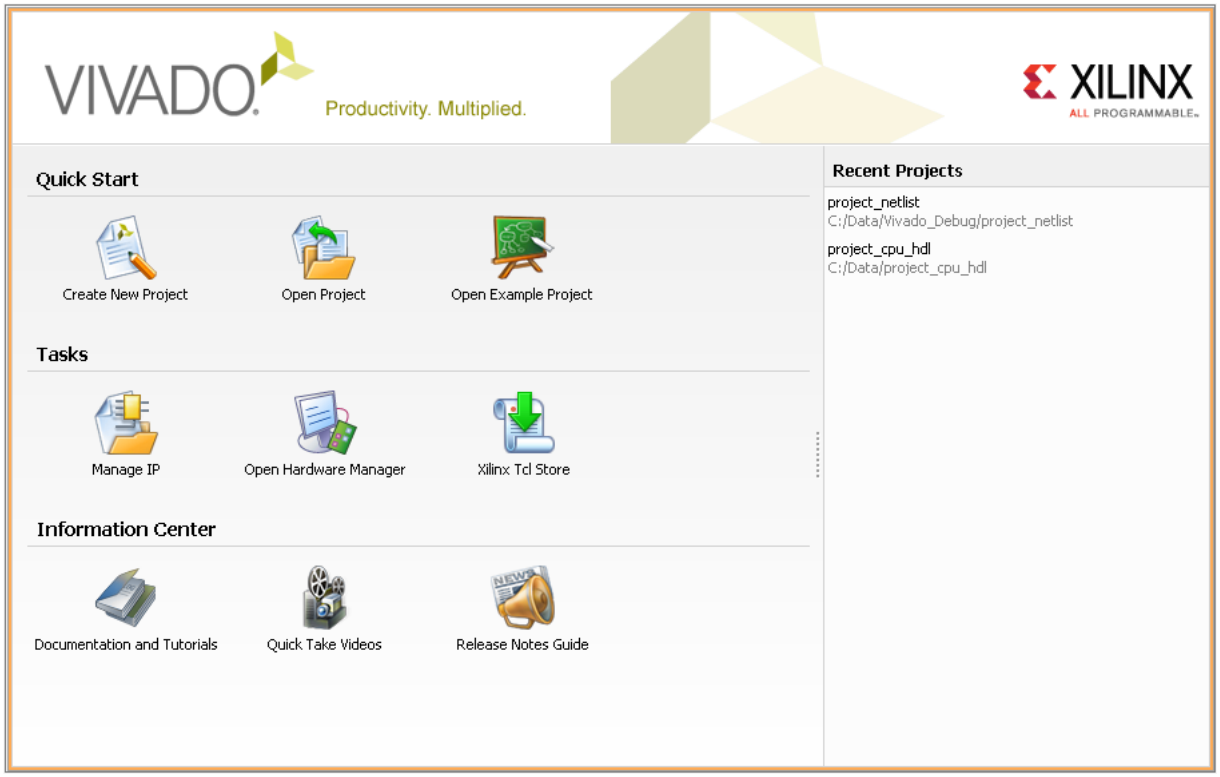

Figure 3-2: **Vivado IDE Getting Started Page**

Starting with a Project

You can create or open a project, and add source files to define your design. The Quick Start section of the Getting Started Page provides links for easy access to the following steps:

- Create a project using the New Project wizard
- Open existing projects
- Open example projects provided by Xilinx

Note: You can also open recently accessed projects from the Recent Projects list.

If you are working with a project, the tool automatically manages your design and keeps track of design file status. You can launch predefined design flow steps, and access results reports along the way.

For more information on design entry, see the *Vivado Design Suite User Guide: System-Level Design Entry* (UG895) [Ref 11]. For information on the next steps in the design flow, see the *Vivado Design Suite User Guide: Design Flows Overview* (UG892) [Ref 8].

Managing IP

You can create an IP location to configure and manage IP remotely, which allows access from different design projects and source control management systems. You can use the Vivado IP catalog to browse and customize delivered IP as well as open existing IP and repositories.

For more information on design entry, see the *Vivado Design Suite User Guide: System-Level Design Entry* (UG895) [Ref 11]. For information on IP, see the *Vivado Design Suite User Guide: Designing with IP* (UG896) [Ref 12].

Opening the Hardware Manager

You can open the Vivado Design Suite Hardware Manager to program your design into a device. The Vivado logic analyzer and Vivado serial I/O analyzer features of the tool enable you to debug your design. For example, you can add ILA, VIO, and JTAG-to-AXI cores to your design for debugging in the Vivado logic analyzer, or use the IBERT example design from the Xilinx IP catalog to test and configure the GTs in your design with the Vivado serial I/O analyzer.

For more information on these tools, see the *Vivado Design Suite User Guide: Programming and Debugging* (UG908) [Ref 13].

Accessing the Tcl Store

The Xilinx Tcl Store is an open source repository of Tcl code designed primarily for use in FPGA designs with the Vivado Design Suite. The Tcl Store provides access to multiple scripts and utilities contributed from different sources, which solve various issues and improve productivity. You can install Tcl scripts and also contribute Tcl scripts to share your expertise with others.

For more information on working with Tcl scripts and the Xilinx Tcl Store, see the *Vivado Design Suite User Guide: Using Tcl Scripting* (UG894) [Ref 9].

Reviewing Documentation and Videos

From the Getting Started page, you can open documentation, including user guides, tutorials, videos, and the release notes, in the Xilinx Documentation Navigator.

For more information on the Documentation Navigator and the Vivado Design Suite documentation, see Chapter 4, Learning About the Vivado Design Suite.

Chapter 4

Learning About the Vivado Design Suite

Overview

This chapter provides information on where to learn more about the Vivado® Design Suite.

RECOMMENDED: *For a hands-on approach to learning the tool, follow the QuickTake Video Tutorials and the Tool Tutorials.*

Xilinx Documentation Navigator

You can view the Xilinx® tool and hardware documentation in the Xilinx Documentation Navigator (DocNav) or on the Xilinx website. The Documentation Navigator is integrated with the Vivado Design Suite, and it provides a catalog of Xilinx documentation and videos. To open the Documentation Navigator:

- In the Vivado IDE, select any documentation link on the Getting Started page or in the Help menu.
- On Windows, select **Start > All Programs > Xilinx Design Tools > DocNav**.

  Note: You can also double-click the **DocNav** shortcut icon on your desktop
- At the Linux command prompt, enter: `docnav`

Features of the Documentation Navigator include:

- **Filters**: The filters allow you to view documentation by specific document types, specific devices, or other relevant categories.
- **Search**: The search feature enables you to find documentation based on the specified search terms. The search capability works for documentation both in the local repository and on the Xilinx website.
- **Design Hubs**: These pages provide quick access to documentation, training, and information for specific design tasks.

- **UltraFast™ Design Methodology Checklist**: This Design Hub feature enables you to create your own design checklist as described in UltraFast Design Methodology Checklist in Chapter 5.
- **Quick Download**: Documentation Navigator manages downloading Xilinx documentation to your local desktop.
- **Documentation Update**: Documentation Navigator monitors and indicates when documents are updated on the Xilinx website.

RECOMMENDED: *Click the **Update Catalog** button at the top of the Documentation Navigator to update to the latest document catalog from the Xilinx website. This ensures the latest documents and videos are available.*

QuickTake Video Tutorials

Xilinx provides a series of short training videos that focus on specific design tasks to help you learn to use the Vivado IDE. The videos are available in the Documentation Navigator, from the Vivado Design Suite QuickTake Video Tutorials page [Ref 14] on the Xilinx website, and on YouTube.

Tool Tutorials

There are a variety of step-by-step software tool tutorials to help you get working in the Vivado IDE quickly. The tutorials provide step by step instructions to perform specific design tasks in the tool using small example designs. Each tutorial has a series of independent labs relevant to the tutorial subject matter. The tutorials are available in the Documentation Navigator and from the Vivado Design Suite Tutorials page [Ref 15] on the Xilinx website.

Documentation Suite

- **Vivado Design Suite User Guides**: These guides are categorized by design task for easy navigation to the information you need. User guides contain detailed information about running specific commands and performing specific design tasks within the Vivado Design Suite. They are available from the Vivado Design Suite User Guides page [Ref 16] on the Xilinx website.
- **Reference Guides**: These guides provide reference information for topics, such as Tcl commands, constraints, and device libraries. They are available from the Vivado Design Suite Reference Guides page [Ref 17] on the Xilinx website.
- **Methodology Guides**: These guides provide high-level guidance for performing specific design tasks, such as design migrating and large design guidance. They are available from the Vivado Design Suite Methodology Guides page [Ref 18] on the Xilinx website.

Learning About the UltraFast Design Methodology

Overview

The Xilinx UltraFast™ design methodology provides tips and suggestions for each stage of the design process when using the Vivado® Design Suite, including:

- Design flow planning
- Printed circuit board (PCB) and field programmable gate array (FPGA) device planning
- Design creation
- Implementation
- Configuration and debug

UltraFast Design Methodology Guide for the Vivado Design Suite

The *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949) [Ref 19] describes the recommended methodology for optimizing design results and maximizing efficiency when using the Vivado tools. This guide also includes an appendix with the items from the *UltraFast Design Methodology Checklist* (XTP301) [Ref 20], and each item links to relevant information in the guide.

UltraFast Design Methodology Checklist

The *UltraFast Design Methodology Checklist* is designed to facilitate a faster design cycle with the best results. It includes a set of items to consider for each stage of the design process and provides recommended actions to take as well as links to additional information. The checklist is available in spreadsheet format at the *UltraFast Design Methodology Checklist* (XTP301) [Ref 20]. You can also access the checklist from within the

Xilinx Documentation Navigator as follows. For more information on Xilinx Documentation Navigator, see Xilinx Documentation Navigator in Chapter 4.

1. Click the **Design Hub View** tab.
2. At the top of the menu on the left side, click **Create Design Checklist**.
3. In the New Design Checklist dialog box, fill out the information and click **OK**.
4. The new checklist opens, and the tabs across the top provide navigation (Figure 5-1).

   The Title Page tab provides basic information on using the checklist, and the other tabs provide checklist items and recommendations.

Figure 5-1: **UltraFast Design Methodology Checklist Tabs in Xilinx Documentation Navigator**

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

References

These documents provide supplemental material useful with this guide:

1. *Vivado® Design Suite User Guide: Release Notes, Installation, and Licensing* (UG973)
2. *ISE® Design Suite 14: Release Notes, Installation, and Licensing* (UG631)
3. *Vivado Design Suite User Guide: Using the Vivado IDE* (UG893)
4. *Vivado Design Suite User Guide: Design Analysis and Closure Techniques* (UG906)
5. *ISE to Vivado Design Suite Migration Guide* (UG911)
6. *Vivado Design Suite User Guide: Using Constraints* (UG903)
7. Xilinx Downloads
8. *Vivado Design Suite User Guide: Design Flows Overview* (UG892)
9. *Vivado Design Suite User Guide: Using Tcl Scripting* (UG894)
10. *Vivado Design Suite Tutorial: Design Flows Overview* (UG888)
11. *Vivado Design Suite User Guide: System-Level Design Entry* (UG895)

12. *Vivado Design Suite User Guide: Designing with IP* (UG896)
13. *Vivado Design Suite User Guide: Programming and Debugging* (UG908)
14. Vivado Design Suite QuickTake Video Tutorials
15. Vivado Design Suite Tutorials
16. Vivado Design Suite User Guides
17. Vivado Design Suite Reference Guides
18. Vivado Design Suite Methodology Guides
19. *UltraFast™ Design Methodology Guide for the Vivado Design Suite* (UG949)
20. *UltraFast Design Methodology Checklist* (XTP301)
21. Vivado Design Suite QuickTake Video: Design Flows Overview
22. Vivado Design Suite Documentation

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