## Revision History

The following table shows the revision history for this document. The following table shows the revision history for this document.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>10/28/2016</td>
<td>2016.3</td>
<td>Replaced screenshots for updated GUI dialog boxes.</td>
</tr>
<tr>
<td>06/17/2016</td>
<td>2016.2</td>
<td>Added new Lab 7: Debugging Designs Using Incremental Design</td>
</tr>
<tr>
<td>05/04/2016</td>
<td>2016.1</td>
<td>Updates to reflect the 2016.1 Vivado® software changes. Added new Lab6: Using ECO flow to Replace Debug Probes Post Implementation.</td>
</tr>
</tbody>
</table>
# Table of Contents

- **Revision History** ......................................................................................................................... 2
- **Debugging in Vivado Tutorial** ..................................................................................................... 5
  - **Introduction** ................................................................................................................................. 5
  - **Objectives** .................................................................................................................................. 5
  - **Getting Started** ........................................................................................................................... 6
- **Lab 1: Using the Netlist Insertion Method for Debugging a Design** ........................................ 11
  - **Introduction** ................................................................................................................................. 11
  - **Step 1: Creating a Project with the Vivado New Project Wizard** ........................................... 11
  - **Step 2: Synthesizing the Design** ................................................................................................. 13
  - **Step 3: Probing and Adding Debug IP** ....................................................................................... 14
  - **Step 4: Implementing and Generating Bitstream** ....................................................................... 23
- **Lab 2: Using the HDL Instantiation Method for Debugging a Design in Vivado** ..................... 24
  - **Introduction** ................................................................................................................................. 24
  - **Step 1: Creating a Project with the Vivado New Project Wizard** ........................................... 24
  - **Step 2: Synthesize, Implement, and Generate Bitstream** ......................................................... 27
- **Lab 3: Using a VIO Core for Debugging a Design in Vivado** .................................................... 28
  - **Introduction** ................................................................................................................................. 28
  - **Step 1: Creating a Project with the Vivado New Project Wizard** ........................................... 28
  - **Step 2: Synthesize, Implement, and Generate Bitstream** ......................................................... 34
- **Lab 4: Using Synplify Pro Synthesis Tool and Vivado for Debugging a Design** ....................... 35
  - **Introduction** ................................................................................................................................. 35
  - **Step 1: Create a Synplify Pro Project** ........................................................................................ 36
  - **Step 2: Synthesize the Synplify Project** ..................................................................................... 43
  - **Step 3: Create EDIF Netlists for the Black Box Created in Synplify Pro** ............................... 44
  - **Step 4: Create a Post Synthesis Project in Vivado IDE** ............................................................. 44
  - **Step 5: Add (more) Debug Nets to the Project** ....................................................................... 46
  - **Step 6: Implementing the Design and Generating the Bitstream** ......................................... 47
Lab 5: Using Vivado Logic Analyzer to Debug Hardware...................................................................................... 48
  Introduction ............................................................................................................................................................. 48
  Step 1: Verifying Operation of the Sine Wave Generator...................................................................................... 48
  Step 2: Debugging the Sine Wave Sequencer State Machine (Optional).............................................................. 59
Lab 6: Using ECO Flow to Replace Debug Probes Post Implementation................................................................. 78
Lab 7: Debugging Designs Using Incremental Compile Flow .................................................................................. 93
  Introduction ............................................................................................................................................................. 93
  Procedure ................................................................................................................................................................. 93
  Step 1: Opening the Example Design and Adding a Debug Core......................................................................... 93
  Step 2: Compiling the Reference Design............................................................................................................... 97
  Step 3: Create New Runs...................................................................................................................................... 97
  Step 4: Making Incremental Debug Changes....................................................................................................... 99
  Step 5: Running Incremental Compile ................................................................................................................ 103
  Conclusion............................................................................................................................................................... 107
Lab 8: Using Vivado Serial Analyzer to Debug Serial Links.................................................................................. 108
  Introduction ............................................................................................................................................................. 108
  Design Description ............................................................................................................................................... 109
  Step 1: Creating, Customizing, and Generating an IBERT Design.......................................................................... 110
  Step 2: Adding an IBERT core to the Vivado Project........................................................................................... 111
  Step 3: Synthesize, Implement and Generate Bitstream for the IBERT design................................................. 118
  Step 4: Interact with the IBERT core using Serial I/O Analyzer........................................................................ 120
Lab 9: Using Vivado ILA core to Debug JTAG-AXI Transactions......................................................................... 135
  Introduction ............................................................................................................................................................. 135
  Design Description ............................................................................................................................................... 136
  Step 1: Opening the JTAG to AXI Master IP Example Design and Configuring the AXI Interface Debug Connections ......................................................................................................................... 136
  Step 2: Program the KC705 Board and Interact with the JTAG to AXI Master Core................................... 154
  Step 3: Using ILA Advanced Trigger Feature to Trigger on an AXI Read Transaction...................................... 162
Legal Notices.......................................................................................................................................................... 166
  Please Read: Important Legal Notices .................................................................................................................. 166
Debugging in Vivado Tutorial

Introduction

This document contains a set of tutorials designed to help you debug complex FPGA designs. The first four labs explain different kinds of debug flows that you can choose to use during the course of debug. These labs introduce the Vivado® debug methodology recommended to debug your FPGA designs. The labs describe the steps involved in taking a small RTL design and the multiple ways of inserting the Integrated Logic Analyzer (ILA) core to help debug the design. The fifth lab is for debugging high-speed serial I/O links in Vivado. The sixth lab is for debugging JTAG-AXI transactions in Vivado. The first four labs converge at the same point when connected to a target hardware board.

Example RTL designs are used to illustrate overall integration flows between Vivado logic analyzer, ILA, and Vivado Integrated Design Environment (IDE). In order to be successful using this tutorial, you should have some basic knowledge of Vivado Design Suite tool flow.

TRAINING: Xilinx provides training courses that can help you learn more about the concepts presented in this document. Use these links to explore related courses:

- Vivado Design Suite Hands-on Introductory Workshop Training Course
- Vivado Design Suite Tool Flow Training Course
- Essentials of FPGA Design Training Course
- Vivado Design Suite User Guide: Programming and Debugging, (UG908)

Objectives

These tutorials:

- Show you how to take advantage of integrated Vivado logic analyzer features in the Vivado design environment that make the debug process faster and simpler.
- Provide specifics on how to use the Vivado IDE and the Vivado logic analyzer to debug common problems in FPGA logic designs.
- Provide specifics on how to use the Vivado Serial I/O Analyzer to debug high-speed serial links.
After completing this tutorial, you will be able to:

- Validate and debug your design using the Vivado Integrated Design Environment (IDE) and the Integrated Logic Analyzer (ILA) core.
- Understand how to create an RTL project, probe your design, insert an ILA core, and implement the design in the Vivado IDE.
- Generate and customize an IP core netlist in the Vivado IDE.
- Debug the design using Vivado logic analyzer in real-time, and iterate the design using the Vivado IDE and a KC705 Evaluation Kit Base Board that incorporates a Kintex®-7 device.
- Analyze high-speed serial links using the Serial I/O Analyzer.

Getting Started

Setup Requirements

Before you start this tutorial, make sure you have and understand the hardware and software components needed to perform the labs included in this tutorial as listed below.

Software

- Vivado Design Suite 2016.3

Hardware

- Kintex-7 FPGA KC705 Evaluation Kit Base Board
- Digilent Cable
- Two SMA (Sub-miniature version A) cables
Tutorial Design Components

Labs 1 through 4 include:

- A simple control state machine
- Three sine wave generators using AXI-Streaming interface, native DDS Compiler
- Common push buttons (GPIO_BUTTON)
- DIP switches (GPIO_SWITCH)
- LED displays (GPIO_LED) VIO Core (Lab 3 only)

Push Button Switches: Serve as inputs to the de-bounce and control state machine circuits. Pushing a button generates a high-to-low transition pulse. Each generated output pulse is used as an input into the state machine.

DIP Switch: Enables or disables a de-bounce circuit.

De-bounce Circuit: In this example, when enabled, provides a clean pulse or transition from high to low. Eliminates a series of spikes or glitches when a button is pressed and released.

Sine Wave Sequencer State Machine: Captures and decodes input from the two push buttons. Provides sine wave selection and indicator circuits, sequencing among 00, 01, 10, and 11 (zero to three).

LED Displays: GPIO_LED_0 and GPIO_LED_1 display selection status from the state machine outputs, each of which represents a different sine wave frequency: high, medium, and low.
Lab5 includes:

- An IBERT core
- A top-level wrapper that instantiates the IBERT core.

**Board Support and Pinout Information**

Table 1: Pinout Information for the KC705 Board

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Pin Location</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLK_N</td>
<td>AD11</td>
<td>Clock</td>
</tr>
<tr>
<td>CLK_P</td>
<td>AD12</td>
<td>Clock</td>
</tr>
<tr>
<td>GPIO_BUTTONS[0]</td>
<td>AA12</td>
<td>Reset</td>
</tr>
<tr>
<td>GPIO_BUTTONS[1]</td>
<td>AG5</td>
<td>Sine Wave Sequencer</td>
</tr>
<tr>
<td>GPIO_SWITCH</td>
<td>Y28</td>
<td>De-bounce Circuit Selector</td>
</tr>
<tr>
<td>LEDS_n[0]</td>
<td>AB8</td>
<td>Sine Wave Selection[0]</td>
</tr>
<tr>
<td>LEDS_n[1]</td>
<td>AA8</td>
<td>Sine Wave Selection[1]</td>
</tr>
<tr>
<td>LEDS_n[2]</td>
<td>AC9</td>
<td>Reserved</td>
</tr>
<tr>
<td>LEDS_n[3]</td>
<td>AB9</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

**Design Files**

1. In your C: drive, create a folder called /Vivado_Debug.
2. Download the Reference Design Files from the Xilinx website.

   **CAUTION!** The tutorial and design files may be updated or modified between software releases. You can download the latest version of the material from the Xilinx website.

3. Unzip the tutorial source file to the /Vivado_Debug folder. There are six labs that use different methodologies for debugging your design. Select the appropriate lab and follow the steps to complete them

Lab 1: This lab walks you through the steps of marking nets for debug in HDL as well as the post-synthesis netlist (Netlist Insertion Method). Following are the required files:

- debounce.vhd
- fsm.vhd
- sinegen.vhd
- sinegen_demo.vhd
- sine_high/sine_high.xci
- sine_low/sine_low.xci
- sine_mid/sine_mid.xci
- sinegen_demo_kc705.xdc

Lab 2: This lab goes over the details of marking nets for debug in the source HDL (HDL instantiation method) as well as instantiating an ILA core in the HDL. Following are the required files:

- debounce.vhd
- fsm.vhd
- sinegen.vhd
- sinegen_demo_inst.vhd
- ila_0/ila_0.xci
- sine_high/sine_high.xci
- sine_low/sine_low.xci
- sine_mid/sine_mid.xci
- sinegen_demo_kc705.xdc

Lab 3: You can test your design even if the hardware is not physically accessible, using a VIO core. This lab walks you through the steps of instantiating and customizing a VIO core that you will hook to the I/Os of the design. Following are the required files:

- debounce.vhd
- fsm.vhd
- sinegen.vhd
- sinegen_demo_inst_vio.vhd
- sine_high/sine_high.xci
- sine_low/sine_low.xci
- sine_mid/sine_mid.xci
- ila_0/ila_0.xci
Lab 4: Nets can also be marked for debug in a third-party synthesis tool using directives for the synthesis tool. This lab walks you through the steps of marking nets for debug in the Synplify tool and then using Vivado to perform the rest of the debug. Following are the required files:

- debounce.vhd
- fsm.vhd
- sign_high.dcp
- sign_low.dcp
- sine_mid.dcp
- sine_high.xci
- sine_low.xci
- sine_mid.xci
- sinegen.edn
- sinegen_synplify.vhd
- synplify_1.sdc
- synplify_1.fdc
- sinegen_demo_kc705.xdc

Lab 5: Debug high-speed serial I/O links using the Vivado Serial I/O Analyzer. This lab uses the Vivado IP example design.

Lab 6: Using Vivado ILA core to debug JTAG-to-AXI transactions. This lab uses the Vivado IP example design.

**Connecting the Boards and Cables**

1. Connect the Digilent cable from the Digilent cable connector to a USB port on your computer.
2. Connect the two SMA cables (for lab 5 only) as follows:
   a. Connect one SMA cable from J19 (TXP) to J17 (RXP).
   b. Connect the other SMA cable from J20 (TXN) to J66 (RXN).

The relative locations of SMA cables on the board are shown in Figure 1: KC705 Board Showing Key Components.
Lab 1: Using the Netlist Insertion Method for Debugging a Design

Introduction

In this lab, you will mark signals for debug in the source HDL as well as the post synthesis netlist. Then you will create an ILA core and take the design through implementation. Finally, you will use Vivado® to connect to the KC705 target board and debug your design using Vivado Integrated Logic Analyzer.

Step 1: Creating a Project with the Vivado New Project Wizard

To create a project, use the New Project wizard to name the project, to add RTL source files and constraints, and to specify the target device.

1. Invoke the Vivado IDE.
2. In the Getting Started page, click Create New Project to start the New Project wizard. Click Next.
3. In the Project Name page, name the new project proj_netlist and provide the project location (C:/Vivado_Debug). Ensure that Create Project Subdirectory is selected and click Next.
4. In the Project Type page, specify the type of project to create as RTL Project. Click Next.
5. In the Add Sources page:
   a. Set Target Language to VHDL.
   b. Click the green “+” sign, and then click Add Files.
   c. In the Add Source Files dialog box, navigate to the /src/lab1 directory.
   d. Select all VHD source files, and click OK.
   e. Verify that the files are added, and Copy Sources into Project is selected. Click Next.
7. In the **Add Existing IP** dialog box:
   a. Click the green “+” sign, and then click **Add Files**.
   b. In the **Add Configurable IP** dialog box, navigate to the /src/lab1/sine_high directory.
   c. Select XCI source file, and click **OK**.
   d. In the **Add Configurable IP** dialog box, navigate to the /src/lab1/sine_mid directory.
   e. Select XCI source file, and click **OK**.
   f. In the **Add Configurable IP** dialog box, navigate to the /src/lab1/sine_low directory.
   g. Select XCI source file, and click **OK**.
   h. Verify that the files are added and **Copy Sources into Project** is selected. Click **Next**.

8. In the **Add Constraints** dialog box, click the green “+” sign, and then click **Add Files**.

9. Navigate to /src/lab1 directory and select sinegen_demo_kc705.xdc. Click **Next**.

10. In the **Default Part** dialog box, specify the xc7k325tffg900-2 part for the KC705 platform. You can also select **Boards** and then select **Kintex-7 KC705 Evaluation Platform**. Click **Next**.

11. Review the **New Project Summary** page. Verify that the data appears as expected, per the steps above, and click **Finish**.

    **Note:** *It could take a moment for the project to initialize.*
Step 2: Synthesizing the Design

1. In the Project Manager, click Project Settings as shown in the following figure.

   ![Figure 2: Configuring the Project Settings](image)

   **IMPORTANT:** As an optional step, in the Project Settings dialog box, select Synthesis from the left and change flatten hierarchy to none. The reason for changing this setting to none is to prevent the synthesis tool from performing any boundary optimizations for this tutorial.

2. In the Vivado Flow Navigator, expand the Synthesis drop-down list, and click Run Synthesis.

   **Note:** When synthesis runs, a progress indicator appears, showing that synthesis is occurring. This could take a few minutes.
3. In the **Synthesis Completed** dialog box, click **Cancel** as shown in the following figure. You will implement the design later.

![Synthesis Completed Dialog Box](image)

**Figure 3: Synthesis Completed Dialog Box**

---

**Step 3: Probing and Adding Debug IP**

To add a Vivado ILA core to the design, take advantage of the integrated flows between the Vivado IDE and Vivado logic analyzer.

In this step, you will accomplish the following tasks:

- Add debug nets to the project.
- Run the Set Up Debug wizard.
- Implement and open the design.
- Generate the bitstream.
Adding Debug Nets to the Project

Following are some ways to add debug nets using the Vivado IDE:

- Add MARK_DEBUG attribute to HDL files.

  **VHDL**
  
  ```vhdl
  attribute mark_debug : string;
  attribute mark_debug of sine     : signal is "true";
  attribute mark_debug of sineSel  : signal is "true";
  ```

  **Verilog**
  
  ```verilog
  (* mark_debug = "true" *) wire sine;
  (* mark_debug = "true" *) wire sineSel;
  ```

  This method lets you probe signals at the HDL design level. This can prevent optimization that might otherwise occur to that signal. It also lets you pick up the signal tagged for post synthesis, so you can insert these signals into a debug core and observe the values on this signal during FPGA operation. This method gives you the highest probability of preserving HDL signal names after synthesis.

- Right-click and select **Mark Debug** or **Unmark Debug** on a synthesized netlist.

  This method is flexible since it allows probing the synthesized netlist in the Vivado IDE and allows you to add/remove MARK_DEBUG attributes at any hierarchy in the design. In addition, this method does not require HDL source modification. However, there may be situations where synthesis may not preserve the signals due to netlist optimization involving absorption or merging of design structures.

- Use a Tcl prompt to set the MARK_DEBUG attribute on a synthesized netlist.

  ```tcl
  set_property mark_debug true [get_nets -hier [list sine[*]]]
  ```

  This applies the MARK_DEBUG on the current, open netlist.

  This method is flexible since you can turn MARK_DEBUG on and off by modifying the Tcl command. In addition, this method does not require HDL source modification. However, there may be situations where synthesis does not preserve the signals due to netlist optimization involving absorption or merging of design structures.

In the following steps, you learn how to add debug nets to HDL files and the synthesized design using Vivado IDE.

---

**TIP:** Before proceeding, make sure that the Flow Navigator on the left panel is enabled. Use **Ctrl-Q** to toggle it off and on.
Lab 1: Using the Netlist Insertion Method for Debugging a Design

1. In the **Flow Navigator** under the **Synthesis** drop-down list, click **Open Synthesized Design** as shown in the following figure.

![Open Synthesized Design](image)

**Figure 4: Open Synthesized Design**

2. In the main toolbar drop-down menu, select **Debug**. When the **Debug** window opens, click the window if it is not already selected.

3. Expand the **Unassigned Debug Nets** folder. The following figure shows those debug nets that were tagged with MARK_DEBUG attributes in `sinegen_demo.vhd`.

```vhdl
-- Add mark_debug attributes to show debug nets in the synthesized netlist
attribute mark_debug : string;
attribute mark_debug of GPIO_BUTTONS_db : signal is "true";
attribute mark_debug of GPIO_BUTTONS_dly : signal is "true";
attribute mark_debug of GPIO_BUTTONS_re : signal is "true";
attribute mark_debug of DONT_EAT : signal is "true";

component sinegen
port (clk : in std_logic;
  reset : in std_logic;
  sel : in std_logic_vector(1 downto 0);
  sine : out std_logic_vector(19 downto 0);
  );
end component;
```

![VHDL Example Using MARK_DEBUG Attributes](image)

**Figure 5: VHDL Example Using MARK_DEBUG Attributes**

![Unassigned Debug Nets Post-Synthesis](image)

**Figure 6: Unassigned Debug Nets Post-Synthesis**
4. In the **Netlist** window, elect the **Netlist** tab and expand **Nets**. Select the following nets for debugging as shown in the following figure.

- GPIO_BUTTONS_IBUF[0] and GPIO_BUTTONS_IBUF[1] - Nets folder under the top-level hierarchy
- sel(2) - Nets folder under the U_SINEGEN hierarchy
- sine(20) - Nets folder under the U_SINEGEN hierarchy

**Figure 7: Add Nets for Debug from the Synthesized Netlist**

*Note: These signals represent the significant behavior of this design and are used to verify and debug the design in subsequent steps.*
5. Right-click the selected nets and select **Mark Debug** as shown in the following figure.

![Figure 8: Adding Nets from the Netlist Tab](image)

6. Next, mark nets for debug in the Tcl console. Mark nets “\texttt{sine(20)}” under the U\_SINEGEN hierarchy for debug by executing the following Tcl command.

   ```tcl
   set_property mark_debug true [get_nets -hier [list {sine[*]}]]
   ```

   **TIP:** In the **Debug** window, you can see the unassigned nets you just selected. In the **Netlist** window, you can also see the green bug icon next to each scalar or bus, which indicates that a net has the attribute `mark_debug = true` as shown the following two figures.
Lab 1: Using the Netlist Insertion Method for Debugging a Design

Figure 9: Newly Added Nets for Debug from the Synthesized Netlist

Figure 10: Netlist View of Nets Marked for Debug
Running the Set Up Debug Wizard

7. From the Debug window tool bar or Tools drop-down menu, select Set Up Debug. The Set up Debug wizard opens.

8. When the Set up Debug wizard opens, click Next.
9. In the **Nets to Debug** page, shown in the following figure, ensure that all the nets have been added for debug and click **Next**.

![Figure 13: Specify Nets to Debug](image)

10. In the **ILA Core Options** page, go to **Trigger and Storage Settings** section and select both **Capture Control** and **Advanced Trigger**. Click **Next**.
11. In the **Setup Debug Summary** page, make sure that all the information is correct and as expected. Click **Finish**.

![Setup Debug Summary](image)

**Figure 14: Set up Debug Summary**

Upon clicking **Finish**, the relevant XDC commands that insert the ILA core(s) are generated.
Step 4: Implementing and Generating Bitstream.

1. In the Flow Navigator, under Program and Debug, click Generate Bitstream.

2. In the Save Project dialog box click Save. This applies the MARK_DEBUG attributes on the newly marked nets. You can see those constraints by inspecting the sinegen_demo_kc705.xdc file.

3. When the No Implementation Results Available dialog box pops up, click Yes.

4. When the bitstream generation completes, the Bitstream Generation Completed dialog box pops up. Click OK.

5. In the dialog box asking to close synthesized design before opening implemented design. Click Yes.

6. In the Implementation is Out-of-date dialog box, click Yes.

7. Examine the Timing Summary report to ensure that all the specified timing constraints are met.

Proceed to Lab 5: Using Vivado Logic Analyzer to Debug Hardware to complete the rest of the steps for debugging the design.
Lab 2: Using the HDL Instantiation Method for Debugging a Design in Vivado

Introduction

The HDL Instantiation method is one of the two methods supported in Vivado® Debug Probing. For this flow, you will generate an ILA IP using the Vivado IP Catalog and instantiate the core in a design manually as you would with any other IP.

Step 1: Creating a Project with the Vivado New Project Wizard

To create a project, use the New Project wizard to name the project, to add RTL source files and constraints, and to specify the target device.

1. Invoke the Vivado IDE.
2. In the Getting Started page, click Create New Project to start the New Project wizard. Click Next.
3. In the Project Name page, name the new project proj_hdl and provide the project location (C:/Vivado_Debug). Ensure that Create Project Subdirectory is selected. Click Next.
4. In the Project Type page, specify the Type of Project to create as RTL Project. Click Next.
5. In the Add Sources page:
   a. Set Target Language to VHDL.
   b. Click the green “+” sign, and then click Add Files.
   c. In the Add Source Files dialog box, navigate to the /src/lab2 directory.
   d. Select all VHD source files, and click OK.
   e. Verify that the files are added, and Copy Sources into Project is selected. Click Next.
6. In the Add Existing IP (optional) page:
   a. Click the green “+” sign, and then click Add Files.
   a. In the Add Configurable IP dialog box, navigate to the /src/lab2/sine_high directory.
   b. Select XCI source file, and click OK.
   c. In the Add Configurable IP dialog box, navigate to the /src/lab2/sine_mid directory.
Lab 2: Using the HDL Instantiation Method for Debugging a Design in Vivado

d. Select XCI source file, and click **OK**.

e. In the **Add Configurable IP** dialog box, navigate to the /src/lab2/sine_low directory.

f. Select XCI source file, and click **OK**.

g. In the **Add Configurable IP** dialog box, navigate to the /src/lab2/ila_0 directory.

h. Select XCI source file, and click **OK**.

i. Verify that the files are added, and **Copy Sources into Project** is selected. Click **Next**.

7. In the **Add Constraints** dialog box, click the green “+” sign, and then click **Add Files**.

8. Navigate to /src/lab1 directory and select *sinegen_demo_kc705.xdc*. Click **Next**.

9. In the **Default Part** page, specify the *xc7k325tffg900-2* part for the KC705 platform. You can also select **Boards** and then select **Kintex-7 KC705 Evaluation Platform**. Click **Next**.

10. Review the **New Project Summary** page. Verify that the data appears as expected, per the steps above. Click **Finish**.

11. In the **Sources** window in Vivado IDE, expand *sinegen_demo_inst* to see the source files for this lab. Note that *ila_0* core has been added to the project.

![Figure 17: ILA Instantiation in HDL](image-url)
12. Double-click the `sinegen_demo_inst.vhd` file, shown in the following figure to open it and inspect the instantiation and port mapping of the ILA core in the HDL code.

![ILA Port Mapping Code](image)

*Figure 18: Hook Signals that Require Debugging in the ILA*
Step 2: Synthesize Implement and Generate Bitstream

1. From the **Program and Debug** drop-down list, in **Flow Navigator**, click **Generate Bitstream**. This will synthesize, implement and generate a bitstream for the design.

2. The **No Implementation Results Available** dialog box appears. Click **Yes**.

3. After bitstream generation completes, the **Bitstream Generation Completed** dialog box appears. **Open Implemented Design** is selected by default. Click **OK**.

4. In the **Design Timing Summary** window, ensure that all timing constraints are met.

5. Proceed to **Lab 5: Using Vivado Logic Analyzer** to Debug Hardware chapter to complete the rest of this lab.
Lab 3: Using a VIO Core for Debugging a Design in Vivado

Introduction

The Virtual Input/Output (VIO) core is a customizable core that can both monitor and drive internal FPGA signals in real time. The number and width of the input and output ports are customizable in size to interface with the FPGA design. Because the VIO core is synchronous to the design being monitored and/or driven, all design clock constraints that are applied to your design are also applied to the components inside the VIO core. Run time interaction with this core requires the use of the Vivado® logic analyzer feature. The following figure is a block diagram of the new VIO core.

![VIO Block Diagram](image)

Figure 21: VIO Block Diagram

This lab walks you through the steps of instantiating and configuring the VIO core. It walks you through the steps of connecting the I/Os of the design to the VIO core. This way, you can debug your design when you do not have access to the hardware or the hardware is remotely located.

The following ports are created:

- One 4-bit PROBE_IN0 port. This has two bits to monitor the 2-bit Sine Wave selector outputs from the finite state machine (FSM) and other two bits to mimic the state of the other two LEDs on the board. We will configure these 4-bit signals as LEDs during run time to mimic the LEDs displayed on the KC705 board.
• One 2-bit PROBE_OUT0 port to drive the input buttons on the FSM. We will configure it so one bit can be used as a toggle switch during run time to mimic the “PUSH_BUTTON”, SW3, and second bit will be used as the “PUSH_BUTTON”, SW6.

Step 1: Creating a Project with the Vivado New Project Wizard

To create a project, use the New Project wizard to name the project, to add RTL source files and constraints, and to specify the target device.

1. Invoke Vivado IDE.
2. In the Getting Started page, click Create New Project to start the New Project wizard. Click Next.
3. In the Project Name page, name the new project proj_hdl_vio and provide the project location (C:/Vivado_Debug). Ensure that Create project subdirectory is selected. Click Next.
4. In the Project Type page, specify the Type of Project to create as RTL Project. Click Next.
5. In the Add Sources page:
   a. Set Target Language to VHDL.
   b. Click Add Files.
   c. In the Add Source Files dialog box, navigate to the /src/lab3 directory.
   d. Select all VHD source files, and click OK.
   e. Verify that the files are added, and Copy Sources into Project is selected. Click Next.
6. In the Add Existing IP page:
   a. Click the green “+” sign, and then click Add Files.
   b. In the Add Configurable IP dialog box, navigate to the /src/lab3/sine_high directory.
   c. Select all XCI source files, and click OK.
   d. In the Add Configurable IP dialog box, navigate to the /src/lab3/sine_mid directory.
   e. Select all XCI source files, and click OK.
   f. In the Add Configurable IP dialog box, navigate to the /src/lab3/sine_low directory.
   g. Select all XCI source files, and click OK.
   h. In the Add Configurable IP dialog box, navigate to the /src/lab3/ila_0 directory.
   i. Select all XCI source files, and click OK.
   j. Verify that the files are added and Copy sources into project is selected. Click Next.
7. In the Add Constraints dialog box, click the green “+” sign, and then click Add Files.
8. Navigate to /src/lab1 directory and select sinegen_demo_kc705.xdc. Click Next.

9. In the Default Part page, specify the xc7k325tffg900-2 part for the KC705 platform. You can also select Boards and then select Kintex-7 KC705 Evaluation Platform. Click Next.

10. Review the New Project Summary page. Verify that the data appears as expected, per the steps above. Click Finish.

   **Note:** It might take a moment for the project to initialize.

11. In the Sources window in Vivado IDE, expand sinegen_demo_inst_vio to see the source files for this lab. Note that ila_0 core has been added to the project. However, vio_0 (the VIO core) is missing.

![Figure 22: Missing Source for VIO Core](image)

12. In this step, you will instantiate and configure this VIO core. From the Flow Navigator, click IP Catalog, expand Debug & Verification, then expand Debug, and double-click VIO. The Customize IP dialog box opens.

13. On the General Options tab, leave the Component Name to its default value of vio_0, set Input Probe Count to 1, Output Probe Count to 1, and select the Enable Input Probe Activity Detectors check box.
14. On the **PROBE_IN Ports** tab, set **Probe Width** to 4 bits wide.

15. On the **PROBE_OUT Ports**, set **Probe Width** to 2 bits wide with an initial value of 0 in hex format.
16. Click **OK** to generate the IP. The **Generate Output Products** dialog box will appear. Click **Generate**.

**Figure 25: Configure the PROBE_OUT Ports of the VIO Core**

**Figure 26: Generate Output Products for the VIO Core**
Output product generation should take less than a minute. At this point, you have finished customizing the VIO. This core has already been instantiated in the top level design as shown in the following figure.

![VIO Instantiation in the Top Level Design](image)

**Figure 27: VIO Instantiation in the Top Level Design**

At this point, the **Sources** window should look as shown in the following figure.

![Instantiated VIO Core in the Sources Window](image)

**Figure 28: Instantiated VIO Core in the Sources Window**
17. Double-click `sinegen_demo_inst.vhd` in the Sources window, to open it and inspect the instantiation and port mapping of the ILA core in the HDL code.

![Figure 29: Hook signals that need to be debugged in the ILA](image)

**Step 2: Synthesize, Implement, and Generate Bitstream**

1. From the Program and Debug drop-down list, in Flow Navigator, click Generate Bitstream. This synthesizes, implements, and generates a bitstream for the design.

2. The No Implementation Results Available dialog box appears. Click Yes.

3. After bitstream generation completes, the Bitstream Generation Completed dialog box appears. Open Implemented Design is selected by default. Click OK.

4. Inspect the Timing Summary report and make sure that all timing constraints have been met.

![Figure 30: Report Timing Summary Dialog Box](image)

5. Proceed to Lab 5: Using Vivado Logic Analyzer to Debug Hardware chapter to complete the rest of the steps for debugging the design. Skip forward to Verifying the VIO Core Activity (Only applicable to Lab 3) section to complete the rest of this lab.
Lab 4: Using Synplify Pro Synthesis Tool and Vivado for Debugging a Design

Introduction

This simple tutorial shows how to do the following:

- Create a Synplify Pro project for the wave generator design.
- Mark nets for debug in the Synplify Pro constraints file as well as VHDL source files.
- Synthesize the Synplify Pro project to create an EDIF netlist.
- Create a Vivado® project based on the Synplify Pro netlist.
- Use the Vivado IDE to setup and debug the design from the synthesized design using Synplify Pro (Version 2016.03 SP1).
Step 1: Create a Synplify Pro Project

1. Launch Synplify Pro and select **File > New**.
2. Set **File Type** to **Project File (Project)** as highlighted in the following figure.
3. In the **New File Name** box, enter **synplify_1**.
4. Click **OK**.

![Synplify Pro New Project Dialog Box](image1.png)

**Figure 31: Synplify Pro New Project Dialog Box**

5. If you get a dialog box asking you to create a non-existing directory, click **OK**.

![Synplify Pro project Confirmation Dialog Box](image2.png)

**Figure 32: Synplify Pro project Confirmation Dialog Box**
6. In the left panel of the **Synplify Pro** window, click **Add File** as shown in the following figure.

![Figure 33: Adding Files to a Synplify Pro Project](image)

7. In the **Add Files to Project** dialog box, change the **Files of Type** to **HDL File**. Navigate to `C:\Vivado_Debug\src\lab4`, which shows all the VHDL source files needed for this lab. Select the following three files by pressing the **Ctrl** key and clicking on them.

- debounce.vhd
- fsm.vhd
- sinegen_demo.vhd

8. Click **Add**.
Figure 34: Adding VHDL Source Files to the Synplify Pro Project
10. In the same dialog box set **Files of type** to **Constraints Files**. This shows the `synplify_1.sdc` file. Select the file and click **Add** as shown in the following figure.

![Figure 35: Adding SDC Constraints File to the Synplify Pro Project](image)
11. In the same dialog box, set **Files of type** to **FPGA Constraint Files**. This shows the `synplify_1.fdc` file. Select the file and click **Add** as shown in the following figure. Click **OK**.

![Adding FPGA Constraints File to the Synplify Pro Project](image)

**Figure 36: Adding FPGA Constraints File to the Synplify Pro Project**
12. Now, you need to set the implementation options.

13. Click Implementation Options in the Synplify Pro window as shown in the following figure.

![Opening Implementation Options in Synplify Pro](image1)

**Figure 37:** Opening Implementation Options in Synplify Pro

14. This brings up the Implementation Options dialog box as shown in the following figure. In the Device tab, set Technology to Xilinx Kintex7, Part to XC7K325T, Package to FFG900 and Speed to -2. Leave all the other options at their default values. Click OK.

![Specifying Implementation Options in Synplify Pro](image2)

**Figure 38:** Specifying Implementation Options in Synplify Pro
15. You need to preserve the net names that you want to debug by putting attributes in the HDL files. These attributes are already placed in the `sinegen Demo.vhd` file of this tutorial. Open the `sinegen Demo.vhd` file and inspect the lines shown.

```
-- Attributes for Synplify Pro
attribute syn_keep : boolean;
attribute syn_keep of GPIO BUTTONS_db : signal is true;
attribute syn_keep of GPIO BUTTONS_dly : signal is true;
attribute syn_keep of GPIO BUTTONS_re : signal is true;
```

**Figure 39: Specifying Attributes to Preserve Net Names in Synplify**

16. You also can specify the `MARK_DEBUG` attributes in the source HDL files to mark the signals for debug, as shown in the code snippet from `singen Demo.vhd` file.

```
-- Add mark debug attributes to show debug nets in the synthesized netlist
attribute mark_debug : string;
attribute mark_debug of GPIO BUTTONS_db : signal is "true";
attribute mark_debug of GPIO BUTTONS_dly : signal is "true";
attribute mark_debug of GPIO BUTTONS_re : signal is "true";
```

**Figure 40: Add MARK_DEBUG Attribute in HDL File**

17. The `synplify 1.sdc` file contains various kinds of constraints such as pin location, I/O standard, and clock definition. The `synplify 1.fdc` file contains directives for the compiler. Here is where the nets of interest to us that are marked for debug are located. The attribute and the nets selected for debug are shown in the following figure.

```
declare_attribute -comment {Mark sinegen as black box} {v:work.sinegen} {syn_black_box} {1}
declare_attribute -comment {Set no prune on sinegen} {v:work.sinegen} {syn_no prune} {1}
declare_attribute -comment {Mark entire bus for debug} {i:sinegen.sin e[*]} {mark_debug} {"true"}
declare_attribute -comment {Mark entire bus for debug} {i:sinegen.sel[*]} {mark_debug} {"true"}
```

**Figure 41: Synplify Pro Constraints in FDC Files**

In the above constraints, `sinegen` has been defined as a black box by using the `syn_black_box` attribute. Second, the `syn_no_prune` attribute has been used so that the I/Os of this block are not optimized away. Finally, two nets, `sine[20:0]` and `sel[1:0]`, have been assigned the `MARK_DEBUG` attribute such that these two nets should show up in the synthesized design in Vivado IDE for further debugging. For further information on these attributes, please refer to the Synplify Pro User Manual and Synplify Pro Reference Manual.
Step 2: Synthesize the Synplify Project

1. Before implementing the project, you need to set the name for the output netlist file. By default, the name of the output netlist file is synplify_1.edf. To change the name of the output file, type the following command at the Tcl command prompt:

   %project -result_file "./rev_1/sinegen_demo.edf"

   You will use this file in Vivado IDE.

2. With all the project settings in place, click the Run button in the left panel of the Synplify Pro window to start synthesizing the design.

![Synplify Pro](image)

   Figure 42: Synthesize the Design in Synplify

3. During synthesis, status messages appear in the Tcl Script tab. Warning messages are expected, but there should not be any Error messages. To see detailed messages, click the Messages tab in the bottom left-hand corner of the Synplify Pro console.

4. When synthesis completes, the output netlist is written to the file: rev_1/sinegen_demo.edf

   [Optional] To view the netlist select View > View Result File.

5. Click File > Save All to save the project, then click File > Exit.
Step 3: Create DCPs for the Black Box Created in Synplify Pro

The black box, sinegen, created in the Synplify Pro project, contains the Direct Digital Synthesizer IP. You need to create a synthesized design for this block. To do this, create an RTL type project in Vivado IDE by following the steps outlined below.

1. Launch Vivado IDE.
2. Click Create New Project. This opens up the New Project wizard. Click Next.
3. Under Project Name, set the project name to proj_synplify_netlist. Click Next.
4. Under Project Type, select RTL Project. Click Next.
5. Under Add Sources, click Add Files, navigate to the Vivado_Debug/src/lab4 folder and select the sinegen.vhd file. Set Target Language to VHDL. Ensure that Copy sources into project box is selected. Click Next.
6. Under Add Existing IP, click Add Files, navigate to the Vivado_Debug/src/lab4 folder and select the sine_high.xci, sine_low.xci, and sine_mid.xci files. Click Next.
7. Under Default Parts, select Boards and then select the Kintex-7 KC705 Evaluation Platform and correct version for your hardware. Click Next.
8. Under New Project Summary, ensure that all the settings are correct. Click Finish.
9. Once the project has been created, in Vivado Flow Navigator, under the Project Manager folder, click Project Settings. In the dialog box, in the left panel, click Synthesis. From the pull-down menu on the right panel, set -flatten_hierarchy to none. Click OK.
10. In Vivado IDE Flow Navigator, under Synthesis Folder, click Run Synthesis.
11. When synthesis completes the Synthesis Completed dialog box appears. Select Open Synthesized Design and click OK.
12. Click File > Exit in Vivado IDE. When the OK to exit dialog box pops up, click OK.

Step 4: Create a Post Synthesis Project in Vivado IDE

1. Launch Vivado IDE.
2. Click Create New Project. This opens up the New Project wizard. Click Next.
3. Set the Project Name to proj_synplify. Click Next.
4. Under Project Type, select Post-synthesis Project. Click Next.
5. Under Add Netlist Sources, click Add Files, navigate to the Vivado_Debug/synopsys/rev_1 folder, and select sinegen_demo.edf. Click OK.
6. Add the netlist file created in the previous section. Click Add Files again, navigate to the proj_synplify_netlist/proj_synplify_netlist.runs/synth1 folder and select the following file:
   - sinegen.edn

Add the DCP files created for the sub-module IPs in the previous section. Click Add Files again, navigate to the proj_synplify_netlist/proj_synplify_netlist.srcs/sources1/ip folder and select the following files:
   - sine_high/sine_high.dcp
   - sine_mid/sine_mid.dcp
   - sine_low/sine_low.dcp

Click OK in the Add Source Files dialog box. In the Add Netlist Sources dialog box ensure that Copy Sources into Project is selected. Click Next.

7. Click Add Files, navigate to the Vivado_Debug/src folder, and select the sinegen_demo_kc705.xdc file. This file has the appropriate constraints needed for this Vivado project. Click OK in the Add Constraints File dialog box. In the Add Constraints (optional) dialog box ensure that Copy Constraints into Project is selected. Click Next.

8. Under Default Part, select Boards and then select Kintex-7 KC705 Evaluation Platform and the right version number for your hardware. Click Next.

9. Under New Project Summary, ensure that all the settings are correct and click Finish.

10. In the Sources window, ensure sinegen_demo.edf is selected as the top module.
Step 5: Add More Debug Nets to the Project

1. In Vivado IDE, in the Flow Navigator, select Open Synthesized Design from the Netlist Analysis folder.

2. Select the Netlist tab in the Netlist window to expand Nets. Select the following nets for debugging:
   - GPIO_BUTTONS_c(2)
   - sine (20)

   After selecting all the specified nets, right-click the nets and click Mark Debug, as shown in the following figure.

![Figure 43: Mark Additional Signals for Debug](image)

3. In the Confirm Debug Net(s) dialog box, click OK.

4. You should be able to see all the nets that are marked for debug, as shown in the following figure.

![Figure 44: Nets Added for Debug through the Synplify Pro Flow in Vivado IDE](image)
**Running the Set up Debug Wizard**

1. Click the **Set up Debug** icon in the **Debug** window or select the **Tools** menu, and select **Set up Debug**. The **Set up Debug** wizard opens.

2. Click through the wizard to create Vivado logic analyzer debug cores, keeping the default settings.

   **Note:** In the **Specify Nets to Debug** dialog box, ensure that all the nets marked for debug have the same clock domain.

---

**Step 6: Implementing the Design and Generating the Bitstream**

1. In the **Flow Navigator**, under the **Program and Debug** drop-down list, click **Generate Bitstream**.
2. In the **Save Project** dialog box, click **Save**.
3. When the Bitstream generation finishes, the **Bitstream Generation Completed** dialog box pops-up and **Open Implemented Design** is selected by default. Click **OK**.
4. If you get a dialog box asking to close the synthesized design before opening the implemented design, click **Yes**.
5. Proceed to **Lab 5: Using Vivado Logic Analyzer to Debug Hardware** to complete the rest of this lab.
Lab 5: Using Vivado Logic Analyzer to Debug Hardware

Introduction
The final step in debugging is to connect to the hardware and debug your design using the Integrated Logic Analyzer. Before continuing, make sure you have the KC705 hardware plugged into a machine.

In this step, you learn:

- How to debug the design using the Vivado® logic analyzer.
- How to use the currently supported Tcl commands to communicate with your target board (KC705).
- How to discover and correct a circuit problem by identifying unintended behaviors of the push button switch.
- Some useful techniques for triggering and capturing design data.

Step 1: Verifying Operation of the Sine Wave Generator
After doing some setup work, you will use Vivado logic analyzer to verify that the sine wave generator is working correctly. Your two primary objectives are to verify that:

- All sine wave selections are correct.
- The selection logic works correctly.

Target Board and Server Set Up
Connecting to the target board remotely
If you plan to connect remotely, you need to make sure that the KC705 board is plugged into a machine and you are running an hw_server application on that machine. If you plan to connect locally, skip steps 1-5 below and go directly to the Connecting to the Target Board Locally section.

1. Connect the Digilent USB JTAG cable of your KC705 board to a USB port on a Windows system.
2. Ensure that the board is plugged in and powered on.
3. Power cycle the board to clear the device.
4. Turn DIP switch positions (pin 1 on SW13, De-bounce Enable) to the OFF position.
5. Assuming you are connecting your KC705 board to a 64-bit Windows machine and you will be running the hw_server from the network instead of your local drive, open a cmd prompt and type the following:

```
<Xilinx_Install>\Vivado\2016.3\bin\hw_server
```

Leave this cmd prompt open while the hw_server is running. Note the machine name that you are using; you will use this later when opening a connection to this instance of the hw_server application.

**Connecting to the Target Board Locally**

If you plan to connect locally, ensure that the KC705 board is plugged into a Windows machine and then perform the following steps:

1. Connect the Digilent USB JTAG cable of your KC705 board to a USB port on a Windows system.
2. Ensure that the board is plugged in and powered on.
3. Power cycle the board to clear the device.
4. Turn DIP switch positions (pin 1 on SW13, De-bounce Enable) to the OFF position.

**Using the Vivado Integrated Logic Analyzer**

1. In the Flow Navigator, under Program and Debug, select Open Hardware Manager.

2. The Hardware Manager window opens. Click Open Target > Open New Target.
3. The **Open New Hardware Target** wizard opens. Click **Next**.

4. In the **Hardware Server Settings** page, type the name of the server (or select **Local server** if the target is on the local machine) in the **Connect to** field. Click **Next**.

![Figure 48: Hardware Server Settings](image)

*Note: Depending on your connection speed, this may take about 10 to 15 seconds.*
5. If there is more than one target connected, you will see multiple entries in the Select Hardware Target page. In this tutorial, there is only one target, as shown in the following figure. Click Next.

![Select Hardware Target](image)

*Figure 49: Select Hardware Target*
6. In the **Open Hardware Target Summary** page, click **Finish** as shown in the following figure.

![Figure 50: Hardware Target Summary](image)

7. Wait for the connection to the hardware to complete. The dialog in following figure appears while hardware is connecting.

![Figure 51: Open Hardware Target](image)
After the connection to the hardware target is made, the Hardware window appears as in the following figure.

**Note:** The *Hardware* tab in the *Debug* view shows the hardware target and XC7K325T device detected in the JTAG chain.

![Active Target Hardware](image)

**Figure 52: Active Target Hardware**

8. Next, program the XC7K325T device using the previously created `.bit` bitstream by right-clicking the **XC7K325T** device and selecting *Program Device* as shown in the following figure.

![Program Active Target Hardware](image)

**Figure 53: Program Active Target Hardware**
9. In the **Program Device** dialog box verify that the `.bit` file is correct for the lab that you are working on and click **Program** to program the device as shown in the following figure.

![Figure 54: Select Bitstream File to Download for Lab 1](image)

**CAUTION!** The file paths of the bitstream to be programmed will be different for different labs. Ensure that the relative paths are correct.

**Note:** Wait for the program device operation to complete. This may take few minutes.

10. Ensure that an ILA core was detected in the **Hardware** panel of the **Debug** view.

![Figure 55: ILA Core Detection](image)
11. The Integrated Logic Analyzer dashboard opens, as shown in the following figure.

![Vivado Integrated Logic Analyzer window](image)

**Figure 56: Vivado Integrated Logic Analyzer window**

**Verifying Sine Wave Activity**

12. In the Hardware window, click Run Trigger Immediate to trigger and capture data immediately as shown in the following figure.

![Run Trigger Immediate Button](image)

**Figure 57: Run Trigger Immediate Button**
13. In the **Waveform** window, verify that there is activity on the 20-bit sine signal as shown in the following figure.

![Figure 58: Output Sine Wave Displayed in Digital Format](image)

**Displaying the Sine Wave**

14. Right-click **U_SINEGEN/sine[19:0]** signals, and select **Waveform Style > Analog** as shown in the following figure.

*TIP:* The waveform does not look like a sine wave. This is because you must change the radix setting from Hex to Signed Decimal, as described in the following subsection.

![Figure 59: Output Sine Wave Displayed in Analog Format - High Frequency](image)
15. Right-click **U_SINEGEN/sine[19:0]** signals, and select **Radix > Signed Decimal**.

   You should now be able to see the high frequency sine wave as shown in the following figure instead of the square wave.

![Figure 60: Output Sine Wave Displayed in Analog Format - High Frequency](image)

**Correcting Display of the Sine Wave**

To view the mid, and low frequency output sine waves, perform the following steps:

16. Cycle the sine wave sequential circuit by pressing the GPIO_SW_E push button as shown in the following figure.

![Figure 61: Sine Wave Sequencer Push Button](image)
17. Click **Run Trigger Immediately** again to see the new sine selected sine wave. You should see the mid frequency as shown in the following figure. Notice that the `sel` signal also changed from 0 to 1 as expected.

![Figure 62: Output Sine Wave Displayed in Analog Format - Mid Frequency](image)

18. Repeat step 17 and 18 to view other sine wave outputs.

![Figure 63: Output Sine Wave Displayed in Analog Format - Low Frequency](image)

![Figure 64: Output Sine Wave Displayed in Analog Format - Mixed Frequency](image)

**Note:** As you sequence through the sine wave selections, you may notice that the LEDs do not light up in the expected order. You will debug this in the next section of this tutorial. For now, verify for
Step 2: Debugging the Sine Wave Sequencer State Machine (Optional)

As you corrected the sine wave display, the LEDs might not have lit up in sequence as you pressed the Sine Wave Sequencer button. With each push of the button, there should be a single, cycle-wide pulse on the GPIO_BUTTONS_re[1] signal. If there is more than one, the behavior of the LEDs becomes irregular. In this section of the tutorial, use Vivado logic analyzer to probe the sine wave sequencer state machine, and to view and repair the root cause of the problem.

Before starting the actual debug process, it is important to understand more about the sine wave sequencer state machine.

**Sine Wave Sequencer State Machine Overview**

The sine wave sequencer state machine selects one of the four sine waves to be driven onto the sine signal at the top-level of the design. The state machine has one input and one output. The following figure shows the schematic elements of the state machine. Refer to this diagram as you read the following description and as you perform the steps to view and repair the state machine glitch.

- The input is a scalar signal called “button”. When the button input equals “1”, the state machine advances from one state to the next.
- The output is a 2-bit signal vector called “Y”, and it indicates which of the four sine wave generators is selected.

The input signal button connects to the top-level signal GPIO_BUTTONS_re[1], which is a low-to-high transition indicator on the Sine Wave Sequencer button. The output signal Y connects to the top-level signal, sineSel, which selects the sine wave.

![Figure 65: Sine Wave Sequencer Button Schematic](image)

**Viewing the State Machine Glitch**

You cannot troubleshoot the issue identified above by connecting a debug probe to the GPIO_BUTTON [1] input signal itself. The GPIO_BUTTON [1] input signal is a PAD signal that is not directly accessible...
Lab 5: Using Vivado Logic Analyzer to Debug Hardware

from the FPGA fabric. Instead, you must trigger on low-to-high transitions (rising edges) on the GPIO_BUTTON_IBUF signal, which is connected to the output of the input buffer of the GPIO_BUTTON [1] input signal.

As described earlier, the glitch reveals itself as multiple low-to-high transitions on the GPIO_BUTTONS_1_IBUF signal, but it occurs intermittently. Because it could take several button presses to detect it, you will now set up the Vivado logic analyzer tool to Repetitive Trigger Run Mode. This setting makes it easier to repeat the button presses and look for the event in the Waveform viewer.

1. Open the Debug Probes window if not already open by selecting Window > Debug Probes from the Vivado main menu.

2. In the ILA Core Properties window scroll down to the link marked To view editable ILA Properties: Open ILA Dashboard and set the following:
   a. Trigger Mode to BASIC_ONLY
   b. Capture Mode to BASIC
   c. Window Data Depth to 1024
   d. Trigger position to 512
   e. Press the + button in the Trigger setup window and add probe GPIO_BUTTONS_IBUF_1. Change the Value field to RX by selecting the value RX in the Value field, as shown in the following figure.
Figure 66: Setting Trigger Conditions
CAUTION! For different labs the GPIO_BUTTONS_IBUF may show up differently. This may show up as two individual bits or two bits lumped together in a bus. Ensure that you are using bit 1 of this bus to set up your trigger condition. For example in case of a two-bit bus, you will set the Value field in the Compare Value dialog box to RX.

3. Enable the Auto-Retrigger mode on the ILA debug core as shown below.

![Figure 67: Enable Auto-retrigger](image)

CAUTION! The ILA properties window may look slightly different for different labs.

When you issue a Run Trigger or a Run Trigger Immediate command after setting the Auto Retrigger mode, the ILA core does the following repetitively until you disable the Auto Retrigger mode option.

- Arms the trigger.
- Waits for the trigger.
- Uploads and displays waveforms.
4. On the KC705 board, press the Sine Wave Sequencer button until you see multiple transitions on the GPIO_BUTTONS_1_IBUF signal (this could take 10 or more tries). This is a visualization of the glitch that occurs on the input. An example of the glitch is shown in the following two figures.

CAUTION! You may have to repeat the previous two steps repeatedly to see the glitch. Once you can see the glitch, you may observe that the signal glitches are not at exactly the same location as shown in the figure below.

![Figure 68: GPIO_BUTTONS_BUF1 Signal Glitch](image1)

![Figure 69: GPIO Buttons_1_re Signal Glitch magnified](image2)
Fixing the Signal Glitch and Verifying the Correct State Machine Behavior

The multiple transition glitch or “bounce” occurs because the mechanical button is making and breaking electrical contact just as you press it. To eliminate this signal bounce, a “de-bouncer” circuit is required.

1. Enable the de-bouncer circuit by setting DIP switch position on the KC705 board (labeled De-bounce Enable in Figure 1: KC705 Board Showing Key Components) to the **ON** or **UP** position.

2. Enable the **Auto-Retrigger** mode on the ILA debug core and click **RunTrigger** on the ILA core, and:
   - Ensure that you no longer see multiple transitions on the GPIO_BUTTON_re[1] signal on a single press of the Sine Wave Sequencer button.
   - Verify that the state machine is working correctly by ensuring that the sineSel signal transitions from 00 to 01 to 10 to 11 and back to 00 with each successive button press.

Verifying the VIO Core Activity (Only applicable to Lab 3)

1. From the **Program and Debug** section in **Flow Navigator**, click **Open Hardware Manager**.

   ![Open Hardware Manager](image)

   **Figure 70: Open Hardware Manager**

   The **Hardware Manager** window opens.

2. Click **Open a new hardware target**.
3. The **Open New Hardware Target** wizard opens. Click **Next**.

4. In the **Hardware Server Settings** page, type the name of the server (or select **Local server** if the target is on the local machine) in the **Connect to** field.

5. Ensure that you are connected to the right target by selecting the target from the **Hardware Targets** page. If there is only one target, that target is selected by default. Click **Next**.

6. In the **Set Hardware Target Properties** page, click **Next**.

7. In the **Open Hardware Target Summary** page, verify that all the information is correct, and click **Finish**.

8. Program the device by selecting and right-clicking the device in the **Sources** window and then selecting **Program Device**.

![Figure 71: Connect to a New Hardware Target](image)

![Figure 72: Program FPGA](image)
9. In the **Program Device** dialog box, ensure that the bit file to be programmed is correct. Click **OK**.

![Figure 73: Program Device with the sinegen_demo_inst_vio.bit File](image1)

10. After the FPGA device is programmed, you see the VIO and the ILA core in the **Hardware** window.

![Figure 74: The ILA and VIO Cores in the Hardware Window](image2)
You now have two debug dashboards, one for the ILA core and the other for the VIO core, as shown in the following figure.

![Image of ILA Core and VIO Core Dashboards]

**Figure 75: ILA Core and VIO Core Dashboards**

11. Click **Run Trigger Immediate** to capture the data immediately.

![Image of Run Trigger Immediate]

**Figure 76: Run Trigger Immediate**

12. Make sure that there is activity on the sine [19:0] signal.

13. Select the sine signal in the **Waveform** window, right-click and select **Waveform Style > Analog**.
14. Select the sine signal in the **Waveform** window again, right-click and select **Radix > Signed Decimal**. You should be able to see the sine wave in the **Waveform** window.

![Figure 77: Sine Wave after Modifying the Properties of the sine [19:0] Signal](image)

15. Instead of using the GPIO_SW push button to cycle through each different sine wave output frequency, you are going to use the virtual “push_button_vio” toggle switch from the VIO core.

16. You can now customize the ILA dashboard options to include the VIO window. This allows you to toggle the VIO output drivers and observe the impact on the ILA waveform window all in one dashboard. Slide out the **Dashboard Options** window.
Figure 78: Invoking Dashboard Options
17. Add the VIO window to the ILA dashboard by selecting `hw_vio_1`.

![Figure 79: Dashboard Options Adding VIO](image)

**Note:** The ILA dashboard now contains the VIO window as well.
18. Adjust the **Trigger Setup – hw ila 1** window and the **hw_vio 1** window so that they are side by side as shown in the following figure.

![ILA Basic Trigger Window and VIO Window Adjustment](image)

**Figure 80: ILA Basic Trigger Window and VIO Window Adjustment**

19. In the **hw_vio 1** window, select the green + button, and select all the probes under hw_vio 1.

20. Click **OK**.

   Note the initial values of all the probes.
Figure 81: VIO Add Probes Window
21. Note the values on all probes in the `hw_vio_1` window.

![Figure 82: VIO Probes Added to hw_vio_1 Window](image-url)
22. Set the push_button_reset output probe by right-clicking `push_button_reset` and select **Toggle Button**.

This will toggle the output driver from logic from ‘0’ to ‘1’ to ‘0’ as you click. It is similar to the actual push button behavior, though there is no bouncing mechanical effect as with a real push button switch.

![Figure 83: Toggle the push_button_reset Signal](image)

The **Value** field for push_button_reset is highlighted.

23. Click in the **Value** field to change its value to **1**.

![Figure 84: Toggle the Value of push_button_reset](image)
24. Follow the step above to change the push_button_vio to Toggle button as well.

25. Set these two bits of the “sineSel” input probe by right-clicking `PROBE_IN0[0]` and `PROBE_IN0[1]` and selecting **LED**.

![Figure 85: Change sineSel to LED](image_url)

26. In the **Select LED Colors** dialog box, pick the **Low Value Color** and the **High Value Color** of the LEDs as you desire and click **OK**.

![Figure 86: Pick the Low Value and High Value Color of the LEDs](image_url)
27. When finished, your **VIO Probes** window in the Hardware Manager should look similar to the following figure.

![Figure 87: Input and Output VIO Signals Displayed](image)

28. To cycle through each different sine wave output frequency using the virtual “push_button_vio” from the VIO core, perform the following simple steps:

a. Toggle the value of the “push_button_vio” output driver from 0 to 1 to 0 by clicking on the logic displayed under the **Value** column. You will notice the sineSel LEDs changed accordingly – 0, 1, 2, 3, 0, etc...

![Figure 88: Toggle push_button_reset](image)

b. Click **Run Trigger** for **hw_ila_1** to capture and display the selected sine wave signal from the previous step.
Figure 89: Run Trigger for hw_ila_1
Lab 6: Using ECO Flow to Replace Debug Probes Post Implementation

This simple tutorial shows you how to replace nets connected to an ILA core in a placed and routed design checkpoint using the Vivado® Design Suite Engineering Change Order (ECO) flow.

**TIP:** To learn more about using the ECO flow, refer to the *Debugging Designs Post Implementation Chapter* in the Vivado Design Suite User Guide: Programming and Debugging, (UG908).

1. Open the Vivado Design Suite, and select **File>Open Checkpoint…**

![Figure 90: Opening a Checkpoint in Vivado IDE](image-url)
2. Open the routed checkpoint that you created in Lab 2: Using the HDL Instantiation Method for Debugging a Design in Vivado.

![Figure 91: Open Checkpoint Dialog Box](image_url)
Change the layout in the Vivado Design Suite toolbar dropdown to **ECO**.

**Figure 92: Change Layout to ECO**

*Note:* The **Flow Navigator** window now changes to **ECO Navigator** with a different set of options.
Lab 6: Using ECO Flow to Replace Debug Probes Post Implementation

Figure 93: ECO Navigator Window
3. In the **ECO Navigator** window, click **Replace Debug Probes** to bring up the **Replace Debug Probes** dialog box. Note the Debug Hub and ILA cores in the design.

![Figure 94: Replace Debug Probes Dialog Box](image)

**IMPORTANT**: Xilinx strongly recommends that you do not replace the clock nets associated with ILA and Debug Hub cores.

4. In the **Replace Debug Probes** dialog box, highlight the probes whose nets you want to change. In this lab we will replace the **GPIO_BUTTONS_dly[0]** net that is being probed.
5. Click the **Edit Probes** button to the right of the **GPIO_BUTTONS_dly[0]** probe net to bring up the **Replace Debug Probes** dialog box.

![Figure 95: Edit Probes Button](image-url)
6. In the **Choose Nets** dialog box, choose the **U_DEBOUNCE_0/clear** net to replace the existing **GPIO_BUTTONS_dly[0]** probe net. Click **OK**.

![Figure 96: Edit Probes Button](image-url)
7. Now click **OK** in the **Replace Debug Probes** dialog.

![Figure 97: Finish Replace Debug Probes](image)

8. Next appears a dialog box that warns about the DON’T_TOUCH property on the GPIO_BUTTONS_dly[0] probe net. Select **Unset Property and Continue**.
9. Click **OK** on the confirmation dialog box to confirm the changes about to be made.

---

**IMPORTANT:** Check the Tcl Console to ensure that there are no Warnings/Errors.
10. Click **Route Design** in the ECO Navigator to bring up the **Route Design** dialog box. Select **Incremental Route** and click **OK**.

*IMPORTANT*: Check the Tcl Console to ensure that there are no Warnings/Errors.

---

![Figure 101: Route Design Dialog Box](image)

**Figure 101: Route Design Dialog Box**

---

![Figure 102: Route Design Dialog Box](image)

**Figure 102: Route Design Dialog Box**
11. Save your modifications to a new checkpoint. Use the **Save Checkpoint As** option in the ECO Navigator to bring up the **Save Checkpoint As** dialog box. Specify a file name for the `.dcp` file and click **OK**.

![Figure 103: Save Checkpoint As Dialog Box](image)

12. When the **Write Debug Probes** dialog appears, click **OK** to generate a new `.ltx` file for the debug probes.

![Figure 104: Write Debug Probes Dialog Box](image)
13. When the **Generate Bitstream** dialog appears, change the bit file name to `project_sinegen_demo_routed_debug_changes.bit` in the **Bit File** field and click **OK** to generate a new `.bit` file that reflects the debug probe changes.

![Generate Bitstream Dialog Box](image)

**Figure 105: Generate Bitstream Dialog Box**

14. Connect to the Vivado Hardware Manager by selecting **Open Hardware Manager** in the ECO Navigator.

15. Connect to the local hardware server by following the steps in the **Target Board and Server Set Up** section in Lab 5: Using Vivado Logic Analyzer to Debug Hardware.
Program the device using the `.bit` file and `.ltx` files that you created in the previous steps.

![Program Device Dialog Box](image)

**Figure 106: Generate Bitstream Dialog Box**

16. Select **Window > Debug Probes** from the Vivado Design Suite toolbar. Ensure that the probes that were replaced in step 8 and 9 above are reflected in the probes associated with `hw_ila_1`. 
Figure 107: Verifying Debug Probes
17. Run the Trigger on the ILA. Ensure the probes that were replaced in step 8 and 9 above are reflected in the Waveform window as well.

![Waveform window displaying ILA status and values]

**Figure 108: Running the Trigger on the ILA**
Lab 7: Debugging Designs Using Incremental Compile Flow

Introduction
This lab introduces the Vivado Incremental Compile Flow to add/edit/delete debug cores to an earlier implementation of the design.

Procedure
This lab consists of five generalized steps followed by general instructions and supplementary detailed steps that allow you to make choices based on your skill level as you progress through the lab.

If you need help completing a general instruction, go to the detailed steps below it, or if you are ready, simply skip the step-by-step directions and move on to the next general instruction.

The lab has five primary steps as follows:
Step 1: Opening the Example Design and Adding a Debug Core
Step 2: Compiling the Reference Design
Step 3: Create New Runs Step
Step 4: Making Incremental Debug Changes
Step 5: Running Incremental Compile

Step 1: Opening the Example Design and Adding a Debug Core
1. Start Vivado IDE
   Load Vivado IDE by doing one of the following:
   - Double-click the Vivado IDE icon on the Windows desktop
   - Type `vivado` in a command terminal.
   From the Getting Started page, click Open Example Project.
2. In the Open Example Project dialog box, click Next.
3. Select the CPU (Synthesized) design template, and click Next.
4. In the Project Name dialog box, specify the following:
Lab 7: Debugging Designs Using Incremental Compile Flow

- Project name: project_cpu_incremental
- Project location: <Project_Dir>

Click **Next**.

5. In the **Default Part** screen, select **xc7k70tfbg484-2** and click **Next**.

6. The **New Project Summary** screen appears, displaying project details. Reviewed these and click **Finish**.

7. When Vivado IDE opens with the default view, open the Synthesized design.

8. In the **Netlist** window, select the set of signals specified below in the **cpuEngine** hierarchy and apply the MARK_DEBUG property by right-clicking and selecting **Mark Debug** from the dialog.

   - cpuEngine/dcqmem_dat_qmem[*],
   - cpuEngine/dcpu_dat_qmem[*],
   - cpuEngine/dcqmem_adr_qmem[*],
   - cpuEngine/du_dsr[*],
   - cpuEngine/dvr0__0[*],
   - cpuEngine/du_dsr[*],
   - cpuEngine/dcqmem_sel_qmem[*]

   ![Figure 109: Set MARK_DEBUG Property](Image)

Alternatively, use the Tcl command below to set the MARK_DEBUG property on the signals specified:

---

Programming and Debugging  
UG936 (v2016.3) October 28, 2016  
www.xilinx.com
set_property mark_debug true [get_nets [list {cpuEngine/dcqmem_dat_qmem[*]} (cpuEngine/dcpu_dat_qmem[*]) (cpuEngine/dcqmem_adr_qmem[*]) {cpuEngine/du_dsr[*]} {cpuEngine/dvr0__0[*]} {cpuEngine/du_dsr[*]} {cpuEngine/dcqmem_sel_qmem[*]}]]

9. In the Flow Navigator, click Set Up Debug to invoke the Set Up Debug wizard.

10. When the Set Up Debug Wizard appears, click Next.
11. When ILA Core Options screen appears, click **Next** again.

12. When **Set Up Debug Summary** screen appears, ensure that **1 debug core** is created and click **Finish**.

13. Check the Debug widow to ensure that **u_ila_0** core has been inserted into the design.
14. Save the new debug XDC commands by selecting File > Save Constraints or clicking the Save Constraints button.

---

### Step 2: Compiling the Reference Design

The following are the steps to run implementation on the reference design.

1. From the Flow Navigator, select Run Implementation.
2. After implementation finishes, the Implementation Complete dialog box opens. Click Cancel.
3. In a project-based design, the Vivado Design Suite saves intermediate implementation results as design checkpoints in the implementation runs directory. You will use one of the saved design checkpoints from the implementation in the incremental compile flow.

   **TIP:** When you re-run implementation, the previous results will be deleted. Save the intermediate implementation results to a new directory or create a new implementation run for your incremental compile to preserve the reference implementation run directory.

4. In the Design Runs window, right click impl_1 and select Open Run Directory from the popup menu. This opens the run directory in a file browser as seen in the figure below. The run directory contains the routed checkpoint (top_routed.dcp) to be used later for the incremental compile flow. The location of the implementation run directory is a property of the run.

5. Get the location of the current run directory in the Tcl Console by typing:

   ```tcl
   get_property DIRECTORY [current_run]
   ```

   This returns the path to the current run directory that contains the design checkpoint. You can use this Tcl command, and the DIRECTORY property, to locate the DCP files needed for the incremental compile flow.

---

### Step 3: Create New Runs

In this step, you define new synthesis and implementation runs to preserve the results of the current runs. Then you make debug related changes to the design and rerun synthesis and implementation. If you do not create new runs, Vivado overwrites the current results.

1. From the Vivado tool bar, select Flow > Create Runs to invoke the Create New Runs wizard.
2. In the Create New Runs screen, click Next.
3. The Configure Implementation Runs screen opens, as shown in the figure below. Select the Make Active check box, and click Next.
4. From the Launch Options window, select Do not launch now and click Next.
5. In the **Create New Runs Summary** screen, click **Finish** to create the new runs.

   The Design Runs window displays the new active runs in bold.

---

**Step 4: Making Incremental Debug Changes**

In this step, in order to add/delete/edit debug cores, you need to reopen the synthesized netlist. Make debug related changes to the design using the Set Up Debug wizard.
1. If you have closed the synthesized netlist, go back to the synthesized design using the Flow Navigator.

2. For this tutorial, assume that you now need to debug some other nets in addition to the ones already being debugged. However, you want to reuse the previous place and route results. So let’s debug the nets fftEngine/fifo_out[*].

3. Apply the MARK_DEBUG property to this bus in the netlist window.

4. Click Set Up Debug to invoke the Set Up Debug wizard in the Flow Navigator.

5. In the Existing Debug Nets tab, select Continue debugging 143 nets connected to existing debug cores.
6. Click **Next** to debug the new unassigned debug nets.
7. Click **Next** and ensure the new nets are in the list of **Nets to Debug**.

![Set Up Debug Additional Debug Nets](image-url)
8. Click **Next** and ensure that two debug cores are created and click **Finish**.

9. Save the new debug XDC commands by clicking the **Save Constraints** button or selecting **File>Save Constraints** from the main Vivado toolbar.

---

**Step 5: Running Incremental Compile**

In the previous steps, you have updated the design with debug changes. You could run implementation on the new netlist, to place and route the design and work to meet the timing requirements. However, with only minor changes between this iteration and the last, the incremental compile flow lets you reuse the bulk of your prior debug, placement and routing efforts. This can greatly reduce the time it takes to meet timing on design iterations. For more information, refer to *Vivado Design Suite User Guide: Implementation*, (UG904).

1. Start by defining the design checkpoint (DCP) file to use as the reference design for the incremental compile flow. This is the design from which the Vivado Design Suite draws placement and routing data.
2. In the Design Runs window, right-click the impl_2 run and select Set Incremental Compile from the popup menu. The Set Incremental Compile dialog box opens.

3. Click the Browse button in the Set Incremental Compile dialog box, and browse to the ./project_cpu_incremental.runs/impl_1 directory.

4. Select top_routed.dcp as the incremental compile checkpoint.

5. Click OK. This information is stored in the INCREMENTAL_CHECKPOINT property of the selected run. Setting this property tells the Vivado Design Suite to run the incremental compile flow during implementation.

6. You can check this property on the current run using the following Tcl command:
   ```tcl
   get_property INCREMENTAL_CHECKPOINT [current_run]
   ```
   This returns the full path to the top_routed.dcp checkpoint.

   **TIP:** To disable Incremental Compile for the current run, clear the INCREMENTAL_CHECKPOINT property. This can be done using the Set Incremental Compile dialog box, or by editing the property directly through the Properties window of the design run, or through the reset_property command.

7. From the Flow Navigator, select Run Implementation.
   This runs implementation on the current run, using the top_routed.dcp file as the reference design for the incremental compile flow. When the run is finished, the Implementation Completed dialog box opens.

8. Select Open Implemented Design and click OK. As shown in the following figure, the Design Runs window shows the elapsed time for implementation run impl_2 versus impl_1.
Note: This is an extremely small design. The advantages of the incremental compile flow are greater and significant with larger, more complex designs.

9. Select the **Reports** tab in the **Results** window area and under **Place Design**, double-click **Incremental Reuse Report** as shown in the following figure.

![Opening Incremental Reuse Report](image)

**Figure 122: Opening Incremental Reuse Report**

The Incremental Reuse Report opens in the Vivado IDE text editor. This report shows the percentage of reused Cells, Ports, and Nets. A higher percentage indicates more effective reuse of placement and routing from the incremental checkpoint.
In the report, fully reused nets indicate that the entire routing of the nets is reused from the reference design. Partially reused nets indicate that some of the routing of the nets reuses routing from the reference design. Some segments re-route due to changed cells, changed cell placements, or both. Non-reused nets indicate that the net in the current design was not matched in the reference design.

Figure 123: Incremental Reuse Report Sample

<table>
<thead>
<tr>
<th>Type</th>
<th>Count</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Matched Cells</td>
<td>44202</td>
<td>45869</td>
<td>96.36%</td>
</tr>
<tr>
<td>Matched Ports</td>
<td>135</td>
<td>135</td>
<td>100.00%</td>
</tr>
<tr>
<td>Matched Nets</td>
<td>51358</td>
<td>53240</td>
<td>96.46%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>Count</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reused Cells</td>
<td>59506</td>
<td>45869</td>
<td>84.81%</td>
</tr>
<tr>
<td>Reused Ports</td>
<td>135</td>
<td>135</td>
<td>100.00%</td>
</tr>
<tr>
<td>Fixed Ports</td>
<td>135</td>
<td>135</td>
<td>100.00%</td>
</tr>
<tr>
<td>Reused Nets</td>
<td>50742</td>
<td>53240</td>
<td>91.61%</td>
</tr>
<tr>
<td>Non-Reused Cells</td>
<td>6563</td>
<td>45869</td>
<td>15.18%</td>
</tr>
<tr>
<td>Discarded illegal placement due to netlist changes</td>
<td>1970</td>
<td>45869</td>
<td>4.29%</td>
</tr>
<tr>
<td>Discarded to improve timing</td>
<td>3225</td>
<td>45869</td>
<td>7.25%</td>
</tr>
<tr>
<td>Fully Reused nets</td>
<td>27567</td>
<td>33665</td>
<td>81.90%</td>
</tr>
<tr>
<td>Partially reused nets</td>
<td>3168</td>
<td>33665</td>
<td>9.41%</td>
</tr>
<tr>
<td>Discarded due to timing</td>
<td>2923</td>
<td>33665</td>
<td>8.68%</td>
</tr>
<tr>
<td>Non-Reused Ports</td>
<td>0</td>
<td>135</td>
<td>0.00%</td>
</tr>
</tbody>
</table>
Conclusion

This concludes the lab. You can close the current project and exit the Vivado IDE.

In this lab, you learned how to run the Incremental Compile Debug flow, using a checkpoint from a previously implemented design. You inserted a new debug core using the Set Up Debug wizard on the synthesized netlist. You examined the similarity between a reference design checkpoint and the current design by examining the Incremental Reuse Report.
Lab 8: Using Vivado Serial Analyzer to Debug Serial Links

Introduction

The Serial I/O analyzer is used to interact with IBERT debug IP cores contained in a design. It is used to debug and verify issues in high speed serial I/O links.

The Serial I/O Analyzer has several benefits as listed below:

- Tight integration with Vivado® IDE.
- Ability to script during netlist customization/generation and serial hardware debug.
- Common interface with the Vivado Integrated Logic Analyzer.

The customizable LogiCORE™ IP Integrated Bit Error Ratio Tester (IBERT) core for 7 series FPGA GTX transceivers is designed for evaluating and monitoring the GTX transceivers. This core includes pattern generators and checkers that are implemented in FPGA logic, and provides access to ports and the dynamic reconfiguration port attributes of the GTX transceivers. Communication logic is also included to allow the design to be run time accessible through JTAG.

In the course of this tutorial, you:

- Create, customize, and generate an Integrated Bit Error Ratio Tester (IBERT) core design in the Vivado Integrated Design Suite.
- Interact with the design using Serial I/O Analyzer. This includes connecting to the target KC705 board, configuring the device, and interacting with the IBERT/Transceiver IP cores.
- Perform a sweep test to optimize your transceiver channel and to plot data using the IBERT sweep plot GUI feature.
Design Description

You can customize the IBERT core and use it to evaluate and monitor the functionality of transceivers for a variety of Xilinx devices. The focus for this tutorial is on Kintex®-7 GTX transceivers. Accordingly, the KC705 target board is used for this tutorial.

The following figure shows a block diagram of the interface between the IBERT Kintex-7 GTX core interfaces with Kintex-7 transceivers.

- **DRP Interface and GTX Port Registers**: IBERT provides you with the flexibility to change GTX transceiver ports and attributes. Dynamic reconfiguration port (DRP) logic is included, which allows the runtime software to monitor and change any attribute in any of the GTX transceivers included in the IBERT core. When applicable, readable and writable registers are also included. These are connected to the ports of the GTX transceiver. All are accessible at run time using the Vivado logic analyzer.

- **Pattern Generator**: Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern generator sends data out through the transmitter.

- **Error Detector**: Each GTX transceiver enabled in the IBERT design has both a pattern generator and a pattern checker. The pattern checker takes the data coming in through the receiver and checks it against an internally generated pattern.

![Figure 124: IBERT Design Flow](Image)
Step 1: Creating, Customizing, and Generating an IBERT Design

To create a project, use the New Project wizard to name the project, to add RTL source files and constraints, and to specify the target device.

1. Invoke the Vivado IDE.
2. In the Getting Started screen, click Create New Project to start the New Project wizard, and click Next.
3. In the Project Name page, name the new project ibert_tutorial and provide the project location (C:/ibert_tutorial). Ensure that Create Project Subdirectory is selected. Click Next.
4. In the Project Type page, specify the Type of Project to create as RTL Project. Click Next.
5. In the Add Sources page, click Next.
6. In the Add Existing IP page, click Next.
7. In the Add Constraints page, click Next.
8. In the Default Part page, select Boards and then select Kintex-7 KC705 Evaluation Platform. Click Next.
9. Review the New Project Summary page. Verify that the data appears as expected, per the steps above. Click Finish.

Note: It might take a moment for the project to initialize.
Step 2: Adding an IBERT core to the Vivado Project

1. In the Flow Navigator click IP Catalog.
   The IP Catalog opens.

   ![Opening the Vivado IP Catalog](image)

   **Figure 125: Opening the Vivado IP Catalog**

2. In the search field of the IP Catalog type **IBERT**, to display the IBERT 7 Series GTX IP.

   ![Instantiating the IBERT IP from the Vivado IP Catalog](image)

   **Figure 126: Instantiating the IBERT IP from the Vivado IP Catalog**

3. Double-click **IBERT 7 Series GTX IP**. This brings up the customization GUI for the IBERT.
4. In the **Customize IP** dialog box, choose the following options in the **Protocol Definition** tab:
   a. Type the name of the component in the **Component Name** field. In this case, leave the name as the default name, `ibert_7series_gtx_0`.
   b. Ensure that the **Silicon Version** is selected as **General ES/Production**.
   c. Ensure that the **Number of Protocols** option is set to 1.
   d. Change the **LineRate (Gbps)** to 8.
   e. Change **DataWidth** to 40.
   f. Change **Refclk (MHz)** to 125.
   g. Ensure that the **Quad Count** is set to 2.
   h. Ensure **Quad PLL** box is selected.

   ![Customize IP dialog box](image)

   **Figure 127: Setting the Protocol Definition on the IBERT Core**

5. Under the **Protocol Selection** tab, update the following selections:
   a. For GTX Location QUAD_117, in the **Protocol Selected** column, click the pull-down menu and select **Custom 1 / 8 Gbps**. This should automatically populate **Refclk Selection** to **MGTREFCLK0 117** and **TXUSRCLK Source** to **Channel 0**.
b. For GTX Location QUAD_118, do the following:
   i. In the **Protocol Selected** column, click the pull-down menu and select **Custom 1 / 8 Gbps**.
   ii. In the **Refclk Selection** column, change the value to **MGTREFCLK0 117**.
   iii. In the **TXUSRCLK Source** column, change the value to **Channel 0**.

![Image](image_url)

**Figure 128: Setting the Protocol Selection on the IBERT Core**

6. Click the **Clock Settings** tab and make the following changes for both QUAD_117 and QUAD_118:
   a. Leave the **Source** column at its default value of **External**.
   b. Change the **I/O Standard** column to **DIFF SSTL15**.
   c. Change the **P Package Pin** to **AD12**.
   d. Change the **N Package Pin** to **AD11**.
   e. Leave the **Frequency(MHz)** at its default value of **200.00**.
7. Click the **Summary** tab and ensure that the content matches the following figure, then click **OK**.

![Figure 129: Specifying clock settings for the IBERT Core](image)

**Figure 129: Specifying clock settings for the IBERT Core**

![Figure 130: IBERT Core Summary Page](image)

**Figure 130: IBERT Core Summary Page**
8. When the **Generate Output Products** dialog box opens, click **Generate**.

![Generate Output Products dialog box](image_url)

**Figure 131: Generate Output Products**
9. In the **Sources** window, right-click the IP, and select **Open IP Example Design**.

![Open Example IP Design Menu Item](image)

**Figure 132: Open Example IP Design Menu Item**
10. In the **Open IP Example Design** dialog box, and specify the location of your project directory. Ensure that the **Overwrite existing example project** is selected and click **OK**.

**Note:** This opens a new instance of Vivado IDE with the new example design opened.
Step 3: Synthesize, Implement and Generate Bitstream for the IBERT design

1. In the newly opened instance of Vivado IDE, click Generate Bitstream in the Flow Navigator. When the No Implementation Results Available dialog box appears, click Yes.

![Figure 134: No Implementation Results Available Dialog Box](image)

When the bitstream generation is complete, the Bitstream Generation Completed dialog box opens.

2. Select Open Hardware Manager, and click OK.

![Figure 135: Bitstream Generation Completed Dialog Box](image)
3. The **Hardware Manager** window appears as shown in the following figure.

![Hardware Manager Window](image)

**Figure 136: Hardware Manager Window**
Step 4: Interact with the IBERT core using Serial I/O Analyzer

In this tutorial step, you connect to the KC705 target board, program the bitstream created in the previous step, and then use the Serial I/O Analyzer to interact with the IBERT design that you created in Step 1. You perform some analysis using various input patterns and loopback modes, while observing the bit error count.

1. Click **Open a new hardware target**. When the **Open New Hardware Target** wizard opens, click **Next**.
2. In the **Connect to** field, choose **Local server**. Click **Next**.
Lab 8: Using Vivado Serial Analyzer to Debug Serial Links

Figure 139: Vivado CSE Server Name Page
3. In the **Select Hardware Target** page, and click **Next**.

There is only one target board in this case to connect to, so that the default is selected.

![Select Hardware Target Page](image_url)

**Figure 140: Select Hardware Target Page**
4. In the **Open Hardware Target Summary** page, review the options that you selected. Click **Finish**.

![Figure 141: Open Hardware Target Summary Dialog Box](image1.png)

5. The **Hardware** window in Vivado IDE should show the status of the target FPGA device on the KC705 board.

![Figure 142: Hardware Window Showing the XC7K325T Device on the KC705 Board](image2.png)
6. Select **XC7K325T_0(0)** in the **Hardware** window, right-click and select **Program Device**.

![Program Target Device](image1.png)

**Figure 143: Program Target Device**

7. The **Program Device** dialog box opens. Make sure that the correct `.bit` file is selected, and click **OK**.

![Program Device Dialog Box](image2.png)

**Figure 144: Program Device Dialog Box**
8. Click **No** in response to “Do you want to auto-detect serial I/O links for IBERT cores?”

![Auto-Detect Serial I/O links](image1.png)

**Figure 145: Auto-Detect Serial I/O links**

9. The **Hardware** window now shows the IBERT IP that you customized and implemented from the previous steps. It contains two QUADS each of which has four GTX transceivers. These components of the IBERT were detected while scanning the device after downloading the bitstream. If you do not see the QUADS then select the **XC7K325** device, right-click and select **Refresh Device**.

![The Hardware Window Showing the QUADS after Device Programming](image2.png)

**Figure 146: The Hardware Window Showing the QUADS after Device Programming**
10. Next, create links for all eight transceivers. Vivado Serial I/O analyzer is a link-based analyzer, which allows users to link between any transmitter and receiver GTs within the IBERT design. For this tutorial, simply link the TX and RX of the same channel. To create a link, right-click the **IBERT Core** in the **Hardware** window and click **Create Links**.

![Figure 147: Create Links](image)

The **Create Links** dialog box opens.

11. Ensure the first transceiver pairs (MGT_X0Y8/TX and MGT_X0Y8/RX) are selected.

![Figure 148: Selecting the Transceiver Pairs for Creating New Links](image)
12. Click the green + button to add a new link. In the **Link group description** field, type **Link Group SMA**. Select the **Internal Loopback** check box.

![Create Links Dialog Box](image)

**Figure 149: Create Links Dialog Box**

For the first link group, call this Link Group SMA as this is the only transceiver channel that is linked through the SMA cables. The new link shows up in the **Links** window.

![Create Link Groups for Other Transceiver Pairs](image)

**Figure 150: Create Link Groups for Other Transceiver Pairs**
13. Click **Create Link** again to create link groups for the rest of the transceiver pairs. To do this ensure that the transceiver pairs are selected, and click the + sign icon (add new link) repeatedly, until all the links have been added to the new link group called **Link Group Internal Loopback**. Click **OK**.

![Create Link Dialog Box to Create the Second Link Group](image)

**Figure 151: Create Link Dialog Box to Create the Second Link Group**

14. After the links have been created, they are added to the **Links** window as shown.

![Links Window after Link Groups are Created](image)

**Figure 152: Links Window after Link Groups are Created**

The status of the links indicate an **8.0 Gbps** line rate.
For more information about the different columns of the Links windows, see the Vivado Design Suite User Guide: Programming and Debugging, (UG908).

15. Change the GT properties of the rest of the transceivers as described above.

16. Next, create a 2D scan. Click Create Scan in the Links window.

![Figure 153: Creating a 2D Scan for Link 1](image)

The Create Scan dialog box opens. In this dialog box, you can change the various scan properties. In this case, leave everything to its default value and click OK. For more information on the scan properties, see Vivado Design Suite User Guide: Programming and Debugging, (UG908).

![Figure 154: The Create Scan Dialog Box](image)
The **Scan Plot** window opens as shown in the following figure.

![Figure 155: 2D Scan Plot](image)

The 2D Scan Plot is a heat map of the BER value.

You can also perform a Sweep test on the links that you created earlier.

17. In the **Links** window, highlight **Link 0** under the Link called **Link Group SMA**, right-click and select **Create Sweep**.

![Figure 156: Create a Sweep Test](image)
18. The **Create Sweep** dialog box opens, as shown below. Various properties for the Sweep test can be changed in this dialog box. Leave all the values to its default state and click **OK**.

![Create Sweep Dialog Box](image_url)

*Figure 157: Create Sweep Dialog Box*
Because here are four different Sweep Properties and each of these properties has three different values (as seen in the **Values to Sweep** column), a total number of 81 sweep tests are carried out. The **Scans** window shows the results of all the scans that have been done for the selected link.

**CAUTION!** Since there are 81 scans to be done, it could be a few minutes before all the scans are complete.

---

**Figure 158: Sweep Test Results in the Scans Window**

To see the results of any of the scans that have been performed, highlight the scan, right-click, and select **Display Scan Plots**.

**Figure 159: Displaying Scan Plots**
The **Scan Plots** window opens showing the details of the scan performed.

![Figure 160: Analyzing the Results of Individual Scans](image)

**Figure 160: Analyzing the Results of Individual Scans**
Lab 9: Using Vivado ILA Core to Debug JTAG-AXI Transactions

Introduction

The purpose of this tutorial is to provide a very quick and easy to reproduce introduction to inserting an ILA core into the JTAG to AXI Master IP core example design, and using the ILA’s advanced trigger and capture capabilities.

What is the JTAG to AXI Master IP core?

The LogiCORE™ IP JTAG-AXI core is a customizable core that can generate AXI transactions and drive AXI signals internal to FPGA at run-time. This supports all memory-mapped AXI interfaces (except AXI4-Stream) and Lite protocol and can be selected using a parameter. The width of AXI data bus is customizable. This IP can drive any AXI4-Lite or Memory Mapped Slave directly. This can also be connected as master to the interconnect. Run-time interaction with this core requires the use of the Vivado® logic analyzer feature.

Key Features

- AXI4 master interface
- Option to select AXI4-Memory Mapped and AXI4-Lite interfaces
- User controllable AXI read and write enable
- User Selectable AXI datawidth : 32 and 64
- User Selectable AXI ID width up to four bits
- Vivado logic analyzer Tcl Console interface to interact with hardware

Additional Documentation

LogiCORE IP JTAG AXI Master v1.0 Product Guide (AXI), (PG174) contains more information the JTAG to AXI Master IP core.
Design Description

This section has three steps as follows:

1. Opening the JTAG to AXI Master IP Example Design project and adding MARK_DEBUG to the AXI interface connection. Inserting an ILA core into the design and configuring it for advanced trigger is also included in this step.

2. Programming the KC705 board and interacting with the JTAG to AXI Master IP core.

3. Using the ILA Advanced Trigger Feature to Trigger on an AXI Read Transaction.

Step 1: Opening the JTAG to AXI Master IP Example Design and Configuring the AXI Interface Debug Connections

To create a project, use the New Project wizard to name the project, add RTL source files and constraints, and specify the target device.

1. Invoke the Vivado IDE.

2. In the Getting Started screen, click Create New Project to start the New Project wizard. Click Next.

3. In the Project Name page, name the new project jtag_2_axi_tutorial and provide the project location (C:/jtag_2_axi_tutorial). Ensure that Create Project Subdirectory is selected. Click Next.

4. In the Project Type page, specify the Type of Project to create as RTL Project. Click Next.

5. In the Add Sources page, click Next.

6. In the Add Existing IP page, click Next.

7. In the Add Constraints page, click Next.
8. In the **Default Part** page, shown in the following figure, choose **Boards** and choose the **Kintex-7 KC705 Evaluation Platform**. Click **Next**.

![Figure 161: Choosing the Kintex-7 KC705 Evaluation Platform board](image)
9. In the **New Project Summary** page, shown in the following figure, click **Finish**.

![New Project Summary](image)

*Figure 162: New Project Summary*
10. In the leftmost panel of the **Flow Navigator** under **Project Manager**, click **IP Catalog**.
11. In the **Search** field on the upper left of the **IP Catalog** tab, type in **JTAG to AXI**.

*Note: The JTAG to AXI Master core shows up under the **Debug & Verification > Debug** category.*

![IP Catalog JTAG to AXI Master](image)

**Figure 164: JTAG to AXI Master IP Core**

12. Double-click **JTAG to AXI Master** core. The **Customization** dialog of the core appears. Accept the default core settings by clicking **OK**.
13. In the **Generate Output Products** dialog box, click **Generate**.
14. The `jtag_axi_0 IP` core is inserted into the design.

15. Right-click `jtag_axi_0` and select **Open IP Example Design**.
Lab 9: Using Vivado ILA Core to Debug JTAG-AXI Transactions

Figure 168: Open IP Example Design Menu Item
16. In the **Open IP Example Design** dialog, ensure that **Overwrite existing example project** is selected. Click **OK**.

![Open IP Example Design Dialog Box](image)

**Figure 169: Open IP Example Design Dialog Box**

17. Open the `example_jtag_axi_0.v` file and notice that the `jtag_axi_0` module is connected to an `axi_bram_ctrl_0` (AXI-BRAM block memory) module.

18. In the `example_jtag_axi_0.v` file, add the following string to the beginning of the wire declaration for each `axi_*` signal from lines 72-108:

```
(* mark_debug *)
```

**Note**: Do not put `mark_debug` on the `axi_aclk` signal since this might result in Vivado Synthesis adding a LUT1 to the clock path, which could possibly cause you to not meet timing.
Lines 72-108 should look like this:

(* mark_debug *) wire [31:0]axi_araddr;
(* mark_debug *) wire [1:0]axi_arburst;
(* mark_debug *) wire [3:0]axi_arcache;
(* mark_debug *) wire [0 :0]axi_arid;
(* mark_debug *) wire [7:0]axi_arlen;
(* mark_debug *) wire axi_arlock;
(* mark_debug *) wire [2:0]axi_arprot;
(* mark_debug *) wire [3:0]axi_arqos;
(* mark_debug *) wire axi_arready;
(* mark_debug *) wire [2:0]axi_arsize;
(* mark_debug *) wire axi_arvalid;
(* mark_debug *) wire [31:0]axi_awaddr;
(* mark_debug *) wire [1:0]axi_awburst;
(* mark_debug *) wire [3:0]axi_awcache;
(* mark_debug *) wire [0 :0]axi_awid;
(* mark_debug *) wire [7:0]axi_awlen;
(* mark_debug *) wire [7:0]axi_awlen;
(* mark_debug *) wire axi_awlock;
(* mark_debug *) wire [2:0]axi_awprot;
(* mark_debug *) wire [3:0]axi_awqos;
(* mark_debug *) wire axi_awready;
(* mark_debug *) wire [2:0]axi_awsize;
(* mark_debug *) wire axi_awvalid;
(* mark_debug *) wire [0 :0]axi_bid;
(* mark_debug *) wire axi_bready;
(* mark_debug *) wire [1:0]axi_bresp;
(* mark_debug *) wire axi_bvalid;
(* mark_debug *) wire [31 :0]axi_rdata;
(* mark_debug *) wire [0 :0]axi_rid;
(* mark_debug *) wire axi_rlast;
(* mark_debug *) wire axi_rready;
(* mark_debug *) wire [1:0]axi_rresp;
(* mark_debug *) wire axi_rvalid;
(* mark_debug *) wire [31 :0]axi_wdata;
(* mark_debug *) wire axi_wlast;
(* mark_debug *) wire axi_wready;
(* mark_debug *) wire [3 :0]axi_wstrb;
(* mark_debug *) wire axi_wvalid;

19. Save changes to example_jtag_axi_o.v file.

20. In the Flow Navigator on the left side of the Vivado window, click Run Synthesis.
21. Open the synthesized design by selecting **Open Synthesized Design** and clicking **OK**.

![Figure 170: Open Synthesized Design](image)

22. After the synthesized design opens, do the following:
   
a. Select the **Debug** layout in the main toolbar Layout drop-down of the Vivado IDE.

![Figure 171: Debug Layout in the Vivado IDE Toolbar](image)
b. Select the **Debug** window near the bottom of the Vivado IDE.

![Debug Window in the Vivado IDE](image)

*Figure 172: Debug Window in the Vivado IDE*
c. Click the **Set up Debug** toolbar button to launch the **Set up Debug** wizard.

![Set Up Debug Wizard](image)

**Figure 173: Set Up Debug Wizard**

23. The **Set up Debug** wizard opens, click **Next**.
24. In the next page of the **Setup Debug** wizard, note that some of the nets that you would like to debug have no detectable clock domains selected. Click the **more info** link in the message banner.

25. In the resulting pop-up, click **Assign All Clock Domains**.
26. In the **Select Clock Domain** dialog box, select the **aclk** clock net, then click **OK**.

![Select Clock Domain Dialog Box](image)

**Figure 175: Select Clock Domain Dialog Box**

27. Observe that all of the nets now have an assigned clock domain. Click **Next**.

28. In the **Trigger and Storage Settings** area of the **ILA General Options** page, ensure that **Advanced Trigger** and **Capture Control** are selected. Click **Next**.
29. When **Set up Debug Summary** page appears, ensure that summary is correct and click **Finish**.

*Note:* See that the ILA core was inserted and attached to the `dbg_hub` core.
30. Save the constraints by clicking **Save**.
31. The insertion of debug cores and changing of properties on those debug cores adds constraints to your target XDC constraint file. This modification of your target constraints file currently sets your synthesis out of date. You can force the design up to date by selecting Run in the Design Runs tab, right-clicking, and selecting **Force Up-to-Date**.

![Figure 178: Forcing Synthesis Up-To-Date](image)

32. In the Flow Navigator on the left side of the Vivado IDE, click **Generate Bitstream**.

33. Click **Yes** to implement the design.

34. Wait until the Vivado status shows **write_bitstream complete**.

35. In the Bitstream Generation Completed dialog box, select **Open Hardware Manager** and click **OK**.

![Figure 179: Open Hardware Manager](image)
Step 2: Program the KC705 Board and Interact with the JTAG to AXI Master Core

1. Connect your KC705 board's USB-JTAG interface to a machine that has Vivado IDE and cable drivers installed on it and power up the board.

2. The Hardware Manager window opens. Click Open New Target. The Open New Hardware Target dialog box opens.

3. In the Connect to field choose Local server, and click Next.
4. If there is more than one target connected to the hardware server, you will see multiple entries in the Select Hardware Target page. In this tutorial, there is only one target as shown in the following figure. Leave these settings at their default values and click Next.
5. Leave these settings at their default values as shown. Click **Next**.
6. In the **Open Hardware Target Summary** page, click **Finish** as shown in the following figure.

![Open Hardware Summary](image1)

**Figure 183: Open Hardware Summary**

7. Wait for the connection to the hardware to complete. The dialog in the following figure appears while hardware is connecting.

![Open Hardware Target](image2)

**Figure 184: Open Hardware Target**
After the connection to the hardware target is made, the dialog shown in the following figure opens.

**Note:** The Hardware tab in the Debug view shows the hardware target and XC7K325T device that was detected in the JTAG chain.

8. Next, program the previously created XC7K325T device using the `.bit` bitstream file by right-clicking the XC7K325T device and selecting Program Device as shown in the following figure.
9. In the **Program Device** dialog box verify that the `.bit` file is correct for the lab that you are working on. Click **Program** to program the device.

![Program Device](image)

**Figure 187: Select Bitstream File to Download**

*Note: Wait for the program device operation to complete. This may take few minutes.*

10. Verify that the JTAG to AXI Master and ILA cores are detected by locating the `hw_axi_1` and `hw ila_1` instances in the **Hardware Manager** window.

![Hardware Manager](image)

**Figure 188: ILA Core Instances in the Hardware Window**
11. You can communicate with the JTAG to AXI Master core with Tcl commands only. You can issue AXI read and write transactions using the `run_hw_axi` command. However, before issuing these transactions, it is important to reset the JTAG to AXI Master core. Because the `aresetn` input port of the `jtag_axi_0` core instance is not connected to anything, you need to use the following Tcl commands to reset the core:

   ```tcl
   reset_hw_axi [get_hw_axis hw_axi_1]
   ```

   ![Figure 189: Reset JTAG to AXI core](image)

12. The next step is to create a 4-word AXI burst transaction to write to the first four locations of the BRAM:

   ```tcl
   set wt [create_hw_axi_txn write_txn [get_hw_axis hw_axi_1] -type WRITE -address 00000000 -len 128 -data {44444444_33333333_22222222_11111111}]
   ```

   where:
   - `write_txn` is the name of the transaction
   - `[get_hw_axis hw_axi_1]` returns the `hw_axi_1` object
   - `-address 00000000` is the start address
   - `-len 128` sets the AXI burst length to 128 words
   - `-data {44444444_33333333_22222222_11111111}` is the data to be written.

   **Note:** The data direction is MSB to the left (i.e., address 3) and LSB to the right (i.e., address 0). Also note that the data will be repeated from the LSB to the MSB to fill up the entire burst.

13. The next step is to set up a 128-word AXI burst transaction to read the contents of the first four locations of the AXI-BRAM core:

   ```tcl
   set rt [create_hw_axi_txn read_txn [get_hw_axis hw_axi_1] -type READ -address 00000000 -len 128]
   ```

   where:
   - `read_txn` is the name of the transaction
   - `[get_hw_axis hw_axi_1]` returns the `hw_axi_1` object
   - `-address 00000000` is the start address
   - `-len 128` sets the AXI burst length to 4 words
14. After creating the transaction, you can run it as a write transaction using the `run_hw_axi` command:

```
run_hw_axi $wt
```

This command should return the following:
```
INFO: [Labtools 27-147] : WRITE DATA is : 4444444333333332222222211111111...
```

15. After creating the transaction, you can run it as a read transaction using the `run_hw_axi` command:

```
run_hw_axi $rt
```

This command should return the following:
```
INFO: [Labtools 27-147] : READ DATA is : 4444444333333332222222211111111...
```
Step 3: Using ILA Advanced Trigger Feature to Trigger on an AXI Read Transaction

1. In the ILA – hw ila_1 dashboard, locate the Trigger Mode Settings area and set Trigger mode to ADVANCED_ONLY.
2. In the Capture Mode Settings area set the Trigger position to 512.
3. In the Trigger State Machine area click the Create new trigger state machine link.

Figure 190: Setting Trigger Mode to ADVANCED and Trigger Position to 512 in the ILA Dashboard
4. In the New Trigger State Machine File dialog box set the name of the state machine script to txns.tsm.

![New Trigger State Machine File dialog box](image)

**Figure 191: Creating a New Trigger State Machine Script**

5. A basic template of the trigger state machine script is displayed in the Trigger State Machine gadget. Expand the trigger state machine gadget in the ILA dashboard. Copy the script below after line 17 of the state machine script and save the file.

```plaintext
# The "wait_for_arvalid" state is used to detect the start
# of the read address phase of the AXI transaction which
# is indicated by the axi_arvalid signal equal to '1'
state wait_for_arvalid:
  if (axi_arvalid == 1'b1) then
    goto wait_for_rready;
  else
    goto wait_for_arvalid;
  endif

# The "wait_for_rready" state is used to detect the start
# of the read data phase of the AXI transaction which
# is indicated by the axi_rready signal equal to '1'
state wait_for_rready:
  if (axi_rready == 1'b1) then
    goto wait_for_rlast;
  else
    goto wait_for_rready;
  endif
```

# The "wait_for_rlast" state is used to detect the end
# of the read data phase of the AXI transaction which
# is indicated by the axi_rlast signal equal to '1'.
# Once the end of the data phase is detected, the ILA core
# will trigger.
#
state wait_for_rlast:
  if (axi_rlast == 1'b1) then
    trigger;
  else
    goto wait_for_rlast;
endif

Note: The state machine is used to detect the various phases of an AXI read transaction:

- Beginning of the read address phase.
- Beginning of the read data phase.
- End of the read data phase.

6. Arm the trigger of the ILA by right-clicking the hw ila 1 core in the Hardware Manager window and selecting Run Trigger.

![Figure 192: Run Trigger](image)

7. In the Trigger Capture Status window, note that the ILA core is waiting for the trigger to occur, and that the trigger state machine is in the wait_for_a_valid state. Note that the pre-trigger capture of 512 samples has completed successfully:
8. In the Tcl console, run the read transaction that you set up in the previous section of this tutorial.
   
   ```tcl
   run_hw_axi $rt
   ```

   **Note:** The ILA core has triggered and the trigger mark is on the sample where the `axi_rlast` signal is equal to ‘1’, just as the trigger state machine program intended.
Legal Notices

Please Read: Important Legal Notices

The information disclosed to you hereunder (the “Materials”) is provided solely for the selection and use of Xilinx products. To the maximum extent permitted by applicable law: (1) Materials are made available “AS IS” and with all faults, Xilinx hereby DISCLAIMS ALL WARRANTIES AND CONDITIONS, EXPRESS, IMPLIED, OR STATUTORY, INCLUDING BUT NOT LIMITED TO WARRANTIES OF MERCHANTABILITY, NON-INFRINGEMENT, OR FITNESS FOR ANY PARTICULAR PURPOSE; and (2) Xilinx shall not be liable (whether in contract or tort, including negligence, or under any other theory of liability) for any loss or damage of any kind or nature related to, arising under, or in connection with, the Materials (including your use of the Materials), including for any direct, indirect, special, incidental, or consequential loss or damage (including loss of data, profits, goodwill, or any type of loss or damage suffered as a result of any action brought by a third party) even if such damage or loss was reasonably foreseeable or Xilinx had been advised of the possibility of the same. Xilinx assumes no obligation to correct any errors contained in the Materials or to notify you of updates to the Materials or to product specifications. You may not reproduce, modify, distribute, or publicly display the Materials without prior written consent. Certain products are subject to the terms and conditions of Xilinx’s limited warranty, please refer to Xilinx’s Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos; IP cores may be subject to warranty and support terms contained in a license issued to you by Xilinx. Xilinx products are not designed or intended to be fail-safe or for use in any application requiring fail-safe performance; you assume sole risk and liability for use of Xilinx products in such critical applications, please refer to Xilinx’s Terms of Sale which can be viewed at http://www.xilinx.com/legal.htm#tos.

AUTOMOTIVE DISCLAIMER

AUTOMOTIVE PRODUCTS (IDENTIFIED AS “XA” IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE (“SAFETY APPLICATION”) UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD (“SAFETY DESIGN”). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

© Copyright 2012-2016 Xilinx, Inc. Xilinx, the Xilinx logo, Artix, ISE, Kintex, Spartan, Virtex, Zynq, and other designated brands included herein are trademarks of Xilinx in the United States and other countries. All other trademarks are the property of their respective owners.