### Revision History

The following table shows the revision history for this document.

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</table>
Table of Contents

Chapter 1: Logic Analysis Within the IDE

Design Analysis Within the IDE ................................................................. 6
Logic Analysis Features ........................................................................ 6
Using the Netlist Window ................................................................. 7
Using the Hierarchy Window ........................................................... 9
Using the Utilization Report ............................................................ 10
Using the Schematic Window .......................................................... 11
Searching for Objects Using the Find Dialog Box ..................... 15
Analyzing Device Utilization Statistics ........................................ 18
Using Report DRC ............................................................................. 19
Validating Design Methodology DRCs .......................................... 20

Chapter 2: Timing Analysis Features

Report Timing Summary ................................................................. 22
Report Clock Networks ................................................................. 39
Report Clock Interaction ............................................................... 41
Report Pulse Width .................................................................... 48
Report Timing ................................................................................ 49
Report Datasheet ............................................................................ 55
Report Exceptions ........................................................................... 61
Report Clock Domain Crossings ................................................ 69
Report Bus Skew .............................................................................. 90

Chapter 3: Implementation Results Analysis Features

Using the Design Runs Window .......................................................... 94
Placement Analysis .......................................................................... 96
Routing Analysis .............................................................................. 103
Report Design Analysis .................................................................. 109
Report QoR Suggestions ................................................................. 133

Chapter 4: Viewing Reports and Messages

Introduction to Reports and Messages ............................................. 137
Viewing and Managing Messages in the IDE ............................... 138
Vivado Generated Reports and Messages ............................................................... 141
Creating Design Related Reports ................................................................. 142

Chapter 5: Performing Timing Analysis
Introduction to Timing Analysis ................................................................. 161
Understanding the Basics of Timing Analysis ........................................... 165
Reading a Timing Path Report ................................................................. 175
Verifying Timing Signoff ........................................................................ 185

Chapter 6: Synthesis Analysis and Closure Techniques
Using the Elaborated View to Optimize the RTL ............................................. 186
Decomposing Deep Memory Configurations for Balanced Power and Performance .................................................................. 189
Optimizing RAMB Utilization when Memory Depth is not a Power of 2 ................................................................. 192
Optimizing RAMB Input Logic to Allow Output Register Inference .......... 195
Improving Critical Logic on RAMB Outputs ............................................. 199

Chapter 7: Implementation Analysis and Closure Techniques
Using the report_design_analysis Command ............................................. 203
Identifying the Longest Logic Delay Paths in the Design ......................... 207
Identifying High Fanout Net Drivers ....................................................... 208
Determining if Hold-Fixing is Negatively Impacting the Design ............... 210
Quickly Analyzing All Failing Paths ........................................................... 212
Floorplanning ......................................................................................... 213

Appendix A: Timing Methodology Checks
TIMING-1: Invalid Clock Waveform on Clock Modifying Block .................. 228
TIMING-2: Invalid Primary Clock on Internal Pin ........................................ 230
TIMING-3: Invalid Primary Clock on Clock Modifying Block ..................... 231
TIMING-4: Invalid Primary Clock Redefinition on a Clock Tree ................. 233
TIMING-5: Invalid Waveform Redefinition on a Clock Tree ....................... 234
TIMING-6: No Common Primary Clock Between Related Clocks ............... 235
TIMING-7: No Common Node Between Related Clocks ............................ 236
TIMING-8: No Common Period Between Related Clocks ............................ 237
TIMING-9: Unknown CDC Logic ............................................................. 238
TIMING-10: Missing Property on Synchronizer .......................................... 239
TIMING-11: Inappropriate Max Delay with Datapath Only Option ............. 240
TIMING-12: Clock Reconvergence Pessimism Removal Disabled ............... 241
TIMING-13: Timing Paths Ignored Due to Path Segmentation .................... 241
TIMING-14: LUT on the Clock Tree ............................................................ 242
TIMING-15: Large Hold Violation on Inter-Clock Path ............................... 243
TIMING-16: Large Setup Violation ................................................................. 244
TIMING-17: Non-Clocked Sequential Cell .................................................. 245
TIMING-18: Missing Input or Output Delay ................................................. 245
TIMING-19: Inverted Generated Clock Waveform on ODDR ........................ 246
TIMING-20: Non-Clocked Latch ................................................................. 246
TIMING-21: Invalid COMPENSATION Property on MMCM ....................... 247
TIMING-22: Missing External Delay on MMCM .......................................... 248
TIMING-23: Combinatorial Loop Found ..................................................... 249
TIMING-24: Overridden Max Delay Datapath Only .................................... 249
TIMING-25: Invalid Clock Waveform on Gigabit Transceiver (GT) ................. 250
TIMING-26: Missing Clock on Gigabit Transceiver (GT) .............................. 251
TIMING-27: Invalid Primary Clock on Hierarchical Pin ............................... 251
TIMING-28: Auto-Derived Clock Referenced by a Timing Constraint ............... 252
TIMING-29: Inconsistent Pair of Multicycle Paths ...................................... 253
TIMING-30: Sub-Optimal Master Source Pin Selection for Generated Clock .... 254

Appendix B: Additional Resources and Legal Notices

Xilinx Resources ......................................................................................... 255
Solution Centers ......................................................................................... 255
Documentation Navigator and Design Hubs ................................................. 255
References ............................................................................................... 256
Training Resources ..................................................................................... 256
Please Read: Important Legal Notices ...................................................... 257
Logic Analysis Within the IDE

Design Analysis Within the IDE

The following chapters provide an introduction to design analysis in the Xilinx® Vivado® Design Suite Integrated Design Environment (IDE):

- Logic Analysis Within the IDE (this chapter)
- Chapter 2, Timing Analysis Features
- Chapter 3, Implementation Results Analysis Features

Logic Analysis Features

This chapter discusses Logic Analysis Features, and includes:

- Using the Netlist Window
- Using the Hierarchy Window
- Using the Schematic Window
- Searching for Objects Using the Find Dialog Box
- Analyzing Device Utilization Statistics
- Using Report DRC
- Validating Design Methodology DRCs
Using the Netlist Window

The Netlist Window shows the design hierarchy as it is in the netlist, processed by the synthesis tools.

Depending on synthesis settings, the netlist hierarchy may be a one hundred percent match for the original RTL, or there may be no hierarchy. Generally, the synthesis tools default to preserving most of the user hierarchy while optimizing the logic. This results in a smaller, faster netlist.

With the synthesis tool defaults, the netlist hierarchy is recognizable, but the interfaces to the hierarchies may be modified. Some pins and levels of hierarchy may be missing.

Each level of hierarchy shows its hierarchy tree. At each level, the tool shows:

- A nets folder for any nets at that level
- A Leaf Cells folder if there are hardware primitive instances at that level
- Any hierarchies instantiated at that level

Traversing the tree shows the whole branch. The icons next to the cells display information about the state of the design.

For more information, see this link in the Vivado Design Suite User Guide: Using the Vivado IDE (UG893) [Ref 1].
The Properties Window for each level of hierarchy shows utilization statistics including:

- Primitive usage for the whole hierarchical branch, grouped in higher level buckets
- The number of nets crossing the hierarchy boundary
- Clocks used in the hierarchy

![Instance Properties Window](image)

*Figure 1-2: Instance Properties Window*

If you floorplan the design, similar properties are displayed for the Pblock.
Using the Hierarchy Window

Explore the hierarchy to understand resource usage. To open the Hierarchy Window, select Tools > Show Hierarchy, or from the Netlist window, click F6.

As shown in the following figure, the Hierarchy Window displays the hierarchy map for the netlist. Each level of the hierarchy is sized relative to the flat number of instances at that level compared to the total number of instances in the design.

![Hierarchy Window](image)

*Figure 1-3: Hierarchy Window*

*Figure 1-3* shows that cpuEngine, usbEngine0, and usbEngine1 have most of the logic in the design, and all use about the same number of resources.
Using the Utilization Report

The Utilization Report breaks apart the design based on resource type. It displays each resource type independently with consumption per level of hierarchy.

To view the Utilization Report, select Tools > Report > Report Utilization. Figure 1-4 shows the Utilization Report.

In this design, the two `usbEngine` blocks are the two biggest consumers of the RAMB36 and FIFO36 blocks. Click the + (plus) icon to view the consumption at sub-hierarchies.
Using the Schematic Window

The schematic is a graphical representation of the netlist. View the schematic to:

- View a graphical representation for the netlist.
- Review the gates, hierarchies, and connectivity.
- Trace and expand cones of logic.
- Analyze the design.
- Better understand what is happening inside the design.

At the RTL level in Elaborated Design, you see how the tool has interpreted your code. In Synthesize Design and Implemented Design, you see the gates generated by the synthesis tool. To open the schematic, select **Tools > Schematic**. If nothing is selected, the gates, hierarchy, and connectivity appear at the top level of the design, as shown in Figure 1-5.

---

**TIP:** The schematic is simpler if you use a single level of hierarchy only. The schematic populates with the selected element emphasized (blue). The ports for the single hierarchy display.

---

*Figure 1-5: Top Level Schematic*
Chapter 1: Logic Analysis Within the IDE

You can trace the schematic in multiple ways:

- Click the + (plus) icon in the upper left to display the gates in the hierarchy.
- Double-click a port or element to expand it.
- Use the schematic popup.
- Click the < - > arrows to switch between the previous and next schematic views.
- Select **Expand All** to display more logic and connectivity.
- Select **Collapse All** to simplify the schematic.

For more information about schematics, see this link in the Vivado Design Suite User Guide: Using the Vivado IDE (UG893) [Ref 1].

After implementation, the schematic is the easiest way to visualize the gates in a timing path. Select the path, then open the schematic with the gates and nets from that path.
Chapter 1: Logic Analysis Within the IDE

To identify the relevant levels of hierarchy in the schematic, choose **Select Leaf Cell Parents** from the popup menu.

**Figure 1-7:** Schematic with Timing Path

**Figure 1-8:** Timing Path with Select Primitive Parents
As you review the schematic, select the **Highlight** and **Mark** commands to track gates of interest. Color coding primitives (using either a mark or a highlight) makes it easier to track which logic was in the original path, and which logic was added.

![Schematic with Timing Path Marked](image)

*Figure 1-9:  Schematic with Timing Path Marked*
Searching for Objects Using the Find Dialog Box

The Vivado IDE includes powerful find and search capabilities. To open the Find dialog box, select **Edit > Find**. (See the following figure.)

*Note:* You can also open the Find window by pressing **Ctrl+F**.

![Find Dialog Box](image)

*Figure 1-10: Find Dialog Box*

**Find Criteria**

The Find dialog box allows you to search the netlist for a wide range of criteria and properties, as shown in the following figures.
Figure 1-11: Find Dialog Box Displaying Search Criteria

Figure 1-12: Find Dialog Box Showing Properties Options
Find Examples

Select Edit > Find to find, for example:

- All unplaced I/Os
- Only the tool-placed Global Clocks
- All nets with a fanout over 10,000
- All DSPs using the PREG embedded register

Complex Finds

To run a complex find:

1. Set the first search criterion.
2. Click + (plus) next to the Properties drop-down options.
3. Add additional criteria.
4. Join the additional criteria with logical operators (AND, OR).

Tcl Finds

From the script or Tcl console, use the equivalent Tcl get_* command (such as get_cells) to query Vivado objects.

TIP: The Tcl Console at the bottom of the Vivado IDE shows the Vivado Design Suite Tcl commands run for each action executed in the GUI. From the Tcl Console, you can also enter Vivado Design Suite Tcl commands.

For more information on Tcl scripting, see the Vivado Design Suite User Guide: Using Tcl Scripting (UG894) [Ref 2].

For more information on Tcl commands, see the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3], or type <command> -help.
Analyzing Device Utilization Statistics

A common cause of implementation issues comes from not considering the logic and device layout implied by the pinout. Slice logic is uniform in most devices. However, specialized resources such as the following impact logic placement:

- I/O
- High Performance Banks
- High Range Banks
- MGT
- DSP48
- Block RAM
- MMCM
- BUFG
- BUFR

Blocks that are large consumers of a certain specialized resource may have to spread around the device. Take this into account when designing the interface with the rest of the design. Use a combination of the following to find block resources:

- report_utilization
- netlist properties
- Pblock properties
Using Report DRC

Design Rule Checks (DRCs) check the design and report on common issues. Since the 2016.1 release, DRCs are split into two different commands. The methodology DRCs have been moved to the `report_methodology` command, while all other DRCs are in the `report_drc` command. Run non-methodology DRCs using the `report_drc` command. During implementation, the tools also run DRCs. The DRCs become more complete and comprehensive with placement and routing.

RECOMMENDED: Review the DRC messages, Critical Warnings, and Warnings early in the flow to prevent issues later.

At Synthesized Design, the optional Report DRC step reports a Critical Warning for the unconstrained I/Os. The routed design DRC report reports the Critical Warnings. You must review the report. At `write_bitstream`, the DRC has been elevated to an Error. Review the DRC reports early to identify areas of the design that need modification.
Validating Design Methodology DRCs

Due to the importance of methodology, the Vivado tools provide the `report_methodology` command, which specifically checks for compliance with methodology DRCs. There are different types of DRCs depending on the stage of the design process. RTL lint-style checks are run on the elaborated RTL design; netlist-based logic and constraint checks are run on the synthesized design; and implementation and timing checks are run on the implemented design.

To run these checks at the Tcl prompt, open the design to be validated and enter following Tcl command:

```
report_methodology
```

To run these checks from the IDE, open the design to be validated and run the Report Methodology command. The dialog box appears, as shown in Figure 1-14.

![Report Methodology Dialog Box](image)

*Figure 1-14: Report Methodology Dialog Box*

Violations (if there are any) are listed in the Methodology window, as shown in the following figure.
Figure 1-15: DRC Violations

For more information on running design methodology DRCs, refer to this link in the Vivado Design Suite User Guide: System-Level Design Entry (UG895) [Ref 4].
Chapter 2

Timing Analysis Features

Report Timing Summary

Timing analysis is available anywhere in the flow after synthesis. You can review the Timing Summary report files automatically created by the Synthesis and Implementation runs.

If your synthesized or implemented design is loaded in memory, you can also generate an interactive Timing Summary report from:

- Flow Navigator > Synthesis
- Flow Navigator > Implementation
- Tools > Timing > Report Timing Summary

Equivalent Tcl command: report_timing_summary

For more information on the report_timing_summary options, see this link in the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3].

In a synthesized design, the Vivado® IDE timing engine estimates the net delays based on connectivity and fanout. The accuracy of the delays is greater for nets between cells that are already placed by the user. There can be larger clock skew on paths where some of the cells have been pre-placed, such as I/Os and GTs.

In an Implemented Design, the net delays are based on the actual routing information. You must use the Timing Summary report for timing signoff if the design is completely routed. To verify that the design is completely routed, view the Route Status report.

Report Timing Summary Dialog Box

In the Vivado IDE, the Report Timing Summary dialog box includes the following tabs:

- Options Tab
- Advanced Tab
- Timer Settings Tab
The Results name field at the top of the Report Timing Summary dialog box specifies the name of the graphical report that opens in the Results window. The graphical version of the report includes hyperlinks that allow you to cross-reference nets and cells from the report to Device and Schematic windows, and design source files.

If this field is left empty, the report is returned to the Tcl Console, and a graphical version of the report is not opened in the Results window.

Equivalent Tcl option: `-name`

**Options Tab**

The Options tab in the Report Timing Summary dialog box is shown in the figure below.

![Figure 2-1: Report Timing Summary Dialog Box: Options Tab](image)

**Report Section**

The Report section of the Options tab of the Report Timing Summary dialog box includes:

- **Path delay type**

  Sets the type of analysis to be run. For synthesized designs, only max delay analysis (setup/recovery) is performed by default. For implemented design, both min and max...
delay analysis (setup/hold, recover/removal) are performed by default. To run min delay analysis only (hold and removal), select delay type min.

Equivalent Tcl option: -delay_type

• Report unconstrained paths

Generates information on paths that do not have timing requirements. This option is checked by default in the Vivado IDE, but is not turned on by default in the equivalent Tcl command report_timing_summary.

Equivalent Tcl option: -report_unconstrained

• Report datasheet

Generates the design datasheet as defined in Report Datasheet, in this chapter.

Equivalent Tcl option: -datasheet

Path Limits Section

The Path Limits section of the Options tab of the Report Timing Summary dialog box includes:

• Maximum number of paths per clock or path group: Controls the maximum number of paths reported per clock pair or path group.

Equivalent Tcl option: -max_paths

• Maximum number of worst paths per endpoint: Controls the maximum number of paths potentially reported per path endpoint. This limit is bounded by the maximum number of paths per clock pair or path group. Therefore, the total number of reported paths is still limited by the number of -max_paths.

Equivalent Tcl option: -nworst

Path Display Section

The Path Display section of the Options tab of the Report Timing Summary dialog box includes:

• Display paths with slack less than: Filters the reported paths based on their slack value. This option does not affect the content of the summary tables.

Equivalent Tcl option: -slack_less_than

• Significant digits: Controls the accuracy of the numbers displayed in the report.

Equivalent Tcl option: -significant_digits
Common Section

The following controls common to all three tabs are located at the bottom of the Report Timing Summary dialog box:

- Command: Displays the Tcl command line equivalent of the various options specified in the Report Timing Summary dialog box.
- Open in a New Tab: Opens the results in a new tab, or to replace the last tab opened by the Results window.
- Open in Timing Analysis Layout: Resets the current view layout to the Timing Analysis view layout.

For more information on view layouts, see this link in the Vivado Design Suite User Guide: Using the Vivado IDE (UG893) [Ref 1].

Advanced Tab

The Advanced tab in the Report Timing Summary dialog box is shown in the figure below.

![Report Timing Summary Dialog Box: Advanced Tab](image-url)

Figure 2-2: Report Timing Summary Dialog Box: Advanced Tab
Chapter 2: Timing Analysis Features

Report Section

- Report from cell: Enable to limit the timing reporting on the particular cell of the design. Only paths that start, end, or are fully contained inside the cell will be reported.

  Equivalent Tcl option: -cell

- Show input pins in path: Displays which input pin of the cell is used for the path.

  Equivalent Tcl option: -input_pins

**RECOMMENDED:** Keep this option selected to provide more information about all pins used in the path.

- Report unique Pins: show only one timing path for each unique set of pins.

  Equivalent Tcl option: -unique_pins

File Output Section

- Write results to file: Writes the result to the specified file name. By default the report is written to the Timing window in the Vivado IDE.

  Equivalent Tcl option: -file

- Overwrite/Append: When the report is written to a file, determines whether (1) the specified file is overwritten, or (2) new information is appended to an existing report.

  Equivalent Tcl option: -append

Miscellaneous Section

- Ignore command errors: Executes the command quietly, ignoring any command line errors and returning no messages. The command also returns TCL_OK regardless of any errors encountered during execution.

  Equivalent Tcl option: -quiet

- Suspend message limits during command execution: Temporarily overrides any message limits and return all messages.

  Equivalent Tcl option: -verbose

Timer Settings Tab

To set the timer settings, use either: (1) one of the Vivado IDE timing analysis dialog boxes; or, (2) one of the Tcl commands listed in this section. These settings affect other timing-related commands run in the same Vivado IDE session, except the synthesis and implementation commands.
The timer settings are not saved as a tool preference. The default values are restored for each new session. Do not change the default values. Keeping the default values provides maximum timing analysis coverage with the most accurate delay values.

The Timer Settings tab in the Report Timing Summary dialog box is shown in the figure below.

![Report Timing Summary Dialog Box: Timer Settings Tab](image)

**Interconnect Setting**

Controls whether net delays are calculated based on the estimated route distance between leaf cell pins, by the actual routed net, or excludes net delay from timing analysis. This option is automatically set to Estimated for post-synthesis designs, and to Actual for post-implementation designs.

- Estimated: For unplaced cells, the net delay value corresponds to the delay of the best possible placement, based on the nature of the driver and loads as well as the fanout. A net between unplaced leaf cell pins is labeled unplaced in the timing path report.
For placed cells, the net delay depends on the distance between the driver and the load as well as the fanout. This net is labeled estimated in the timing path report.

• Actual: For routed nets, the net delay corresponds to the actual hardware delay of the routed interconnect. This net is labeled routed in the timing path report.
• None: Interconnect delays are not considered in the timing report and net delays are forced to zero.

Equivalent Tcl command: set_delay_model

**Speed Grade Setting**

Sets the device speed grade. By default, this option is set based on the part selected when creating a project or opening a design checkpoint. You can change this option to report timing on the same design database against another speed grade without rerunning the complete implementation flow.

Equivalent Tcl command: set_speed_grade

**Multi-Corner Configuration Setting**

Specifies the type of path delays to be analyzed for the specified timing corner. Valid values are none, max, min, and min_max. Select none to disable timing analysis for the specified corner.

*RECOMMENDED: Keep both setup (max) and hold (min) analysis selected for both corners.*

Equivalent Tcl command: config_timing_corners

**Disable Flight Delays**

Do not add package delays to I/O delay calculations.

Equivalent Tcl command: config_timing_analysis
Details of the Timing Summary Report

The Timing Summary Report contains the following sections:

- General Information Section
- Timer Settings Section
- Design Timing Summary Section
- Clock Summary Section
- Check Timing Section
- Intra-Clock Paths Section
- Inter-Clock Paths Section
- Path Groups Section
- User-Ignored Paths Section
- Unconstrained Paths Section

The comprehensive information contained in the Timing Summary Report is similar to the information provided by several reports available from the Vivado IDE (Report Clock Interaction, Report Pulse Width, Report Timing, Check Timing) and to some of the reports available in Tcl only (report_clocks). However, the Report Timing Summary also includes information that is unique to this report, such as Unconstrained Paths.

**General Information Section**

The General Information section of the Timing Summary Report provides information about the following:

- Design name
- Selected device, package, and speed grade (with the speed file version)
- Vivado Design Suite release
- Current date
- Equivalent Tcl commands executed to generate the report

**Timer Settings Section**

The Timer Settings section of the Timing Summary Report contains details on the Vivado IDE timing analysis engine settings used to generate the timing information in the report.
Figure 2-4 shows the default options in an example of the Timer Settings section, which includes:

- **Enable Multi-Corner Analysis:** This analysis is enabled for each corner (Multi-Corner Configuration).
- **Enable Pessimism Removal (and Pessimism Removal Resolution):** Ensures that the source and destination clocks of each path are reported with no skew at their common node.
  
  **Note:** This setting must always be enabled.
- **Enable Input Delay Default Clock:** Creates a default null input delay constraint on input ports with no user constraint. It is disabled by default.
- **Enable Preset / Clear Arcs:** Enables timing path propagation through asynchronous pins. It does not affect recovery/removal checks and is disabled by default.
- **Disable Flight Delays:** Disables package delays for I/O delay calculations.

For additional information on default timer settings and how to change them, see config_timing_analysis, available from this link in the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3].

### Design Timing Summary Section

The Design Timing Summary section of the Timing Summary Report (shown in Figure 2-5) provides a summary of the timing for the design, and combines the results of all other sections in one view.

**RECOMMENDED:** Review the Design Timing Summary section to verify that all timing constraints are met after route, or to understand the status of the design at any point in the flow.
Chapter 2: Timing Analysis Features

The Design Timing Summary section includes the following:

- **Setup Area (Max Delay Analysis)**
- **Hold Area (Min Delay Analysis)**
- **Pulse Width Area (Pin Switching Limits)**

**Setup Area (Max Delay Analysis)**

The Setup area of the Design Timing Summary section displays all checks related to max delay analysis: setup, recovery, and data check.

- Worst Negative Slack (WNS): This value corresponds to the worst slack of all the timing paths for max delay analysis. It can be positive or negative.
- Total Negative Slack (TNS): The sum of all WNS violations, when considering only the worst violation of each timing path endpoint. Its value is:
  - 0 ns when all timing constraints are met for max delay analysis.
  - Negative when there are some violations.
- Number of Failing Endpoints: The total number of endpoints with a violation (WNS<0 ns).
- Total Number of Endpoints: The total number of endpoints analyzed.

**Hold Area (Min Delay Analysis)**

The Hold area of the Design Timing Summary section displays all checks related to min delay analysis: hold, removal, and data check.

- Worst Hold Slack (WHS): Corresponds to the worst slack of all the timing paths for min delay analysis. It can be positive or negative.
- Total Hold Slack (THS): The sum of all WHS violations, when considering only the worst violation of each timing path endpoint. Its value is:
  - 0 ns when all timing constraints are met for min delay analysis.
  - Negative when there are some violations.
- Number of Failing Endpoints: The total number of endpoints with a violation (WHS<0 ns).
- Total Number of Endpoints: The total number of endpoints analyzed.

**Pulse Width Area (Pin Switching Limits)**

The Pulse Width area of the Design Timing Summary section displays all checks related to pin switching limits:

- Min low pulse width
- Min high pulse width
- Min period
- Max period
- Max skew (between two clock pins of a same leaf cell, such as for PCIE or GT [UltraScale™ devices only]).

The reported values are:

- Worst Pulse Width Slack (WPWS): Corresponds to the worst slack of all the timing checks listed above when using both min and max delays.
- Total Pulse Width Slack (TPWS): The sum of all WPWS violations, when considering only the worst violation of each pin in the design. Its value is:
  - 0 ns when all related constraints are met.
  - Negative when there are some violations.
- Number of Failing Endpoints: The total number of pins with a violation (WPWS< 0 ns).
- Total Number of Endpoints: The total number of endpoints analyzed.

**Clock Summary Section**

The Clock Summary section of the Timing Summary Report includes information similar to that produced by `report_clocks`:

- All the clocks in the design (whether created by `create_clock`, `create_generated_clock`, or automatically by the tool).
- The properties for each clock, such as name, period, waveform, and target frequency.

**TIP:** The indentation of names reflects the relationship between master and generated clocks.
Check Timing Section

The Check Timing section of the Timing Summary Report contains information about missing timing constraints or paths with constraints issues that need to be reviewed. For complete timing signoff, all path endpoints must be constrained.

For more information on constraints definition, see the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5].

To generate Check Timing as a standalone report, do one of the following:

- Run the **Tools > Timing > Check Timing** menu command.
- Run the Tcl `check_timing` command.
Chapter 2: Timing Analysis Features

The list of checks reported by default, as shown in Figure 2-7, is:

- **pulse_width_clock**: Reports clock pins that have only a pulse width check associated with the pin, and no setup or hold check, no recovery, removal, or \( \text{clk} > Q \) check.
- **no_input_delay**: Number of non-clock input ports without any input delay constraints.
- **no_clock**: Number of clock pins not reached by a defined timing clock. Constant clock pins are also reported.
- **constant_clock**: Checks for clock signals connected to a constant signal (\( \text{gnd/vss/data} \)).
- **unconstrained_internal_endpoints**: Number of path endpoints (excluding output ports) without a timing requirement. This number is directly related to missing clock definitions, which is also reported by the **no_clock** check.
- **no_output_delay**: Number of non-clock output ports without at least one output delay constraint.
- **multiple_clock**: Number of clock pins reached by more than one timing clock. This can happen if there is a clock multiplexer in one of the clock trees. The clocks that share the same clock tree are timed together by default, which does not represent a realistic timing situation. Only one clock can be present on a clock tree at any given time. If you do not believe that the clock tree is supposed to have a MUX, review the clock tree to understand how and why multiple clocks are reaching the specific clock pins.
- **generated_clocks**: Number of generated clocks that refer to a master clock source which is not part of the same clock tree. This situation can occur when a timing arc is disabled on the logical path between the master clock and the generated clock source points. This check also applies to individual edges of the generated clocks when specified with the \(-\text{edges}\) option: the logical path unateness (inverting/non-inverting) must match the edge associations between the master and generated clocks.
- **loops**: Number of combinational loops found in the design. The loops are automatically broken by the Vivado IDE timing engine to report timing.
- **partial_input_delay**: Number of non-clock input ports with only a min input delay or max input delay constraint. These ports are not reported by both setup and hold analysis.
- **partial_output_delay**: Number of non-clock output ports with only a min output delay or max output delay constraint. These ports are not reported by both setup and hold analysis.
- **latch_loops**: Checks for and warns of loops passing through latches in the design. These loops will not be reported as part of combinational loops, and will affect latch time borrowing computation on the same paths.
Chapter 2: Timing Analysis Features

Intra-Clock Paths Section

The Intra-Clock Paths section of the Timing Summary Report (shown in the following figure) summarizes the worst slack and total violations of the timing paths with the same source and destination clock.

![Intra-Clock Paths](image)

Figure 2-8: Timing Summary Report: Intra-Clock Paths Section

To view detailed information, click the names under Intra-Clock Paths in the left index pane. For example, you can view the slack and violations summary for each clock and details about the N-worst paths for SETUP/HOLD/Pulse Width checks. The N-worst is defined using the `-max_paths` on the command line or the maximum number of paths per clock or path group (GUI).

The worst slack value and the number of reported paths are displayed next to the label for each analysis type. See the following figure.

![Intra-Clock Paths Details](image)

Figure 2-9: Timing Summary Report: Intra-Clock Paths Details

Inter-Clock Paths Section

Similar to the Intra-Clock Paths section, the Inter-Clock Paths section of the Timing Summary Report (shown in the following figure) summarizes the worst slack and total violations of the timing paths between different source and destination clocks.
Chapter 2: Timing Analysis Features

To view detailed information, click the names under Inter-Clock Paths in the left index pane. For example, you can view the slack and violations summary for each clock and details about the N-worst paths for SETUP/HOLD/Pulse Width checks. The N-worst is defined using the -max_paths on the command line or the **maximum number of paths per clock or path group** (GUI).

**Path Groups Section**

The Path Groups section of the Timing Summary Report displays default path groups and user-defined path groups. The following figure shows an example of the Path Groups summary table. To access this table, select **Path Groups** in the left pane.

**User-Ignored Paths Section**

The User-Ignored Paths Section of the Timing Summary Report (shown in the following figure) displays the paths that are ignored during timing analysis due to the **set_clock_groups and set_false_path** constraints. The reported slack is infinite.

---

**Warning:** **async_default** is a path group automatically created by the Vivado IDE timing engine. It includes all paths ending with an asynchronous timing check, such as recovery and removal. These two checks are respectively reported under SETUP and HOLD categories, which corresponds to max delay analysis and min delay analysis. Any groups you create using **group_path** appear in this section as well. Any combination of source and destination clocks can be present in a path group.
Unconstrained Paths Section

The Unconstrained Paths section of the Timing Summary Report displays the logical paths that are not timed due to missing timing constraints. These paths are grouped by source and destination clock pairs. The clock name information displays as empty (or NONE) when no clock can be associated with the path startpoint or endpoint.

Reviewing Timing Path Details

You can expand most of the sections to show paths organized by clock pairs. For each SETUP, HOLD and Pulse Width sub-section, you can view the N-worst reported paths. Select any of these paths to view more details in the Path Properties window (Report tab).

To view the same details in a new window, double click the path.

For more information on timing path details, see Chapter 5, Performing Timing Analysis.
To access more analysis views for each path:

1. Right click the path in the right pane.
2. Select one of the following options from the popup menu:
   - **Schematic**: Open a Schematic of the path.
   - **Report Timing on Source to Destination**: Rerun timing analysis on this same path.
   - **Highlight**: Highlight the path in the Device and Schematic windows.

### Filtering Paths With Violations

The report displays the slack value of failing paths in red. To focus on these violations, click the **Show only failing paths** button.

The following figure shows the Timing Summary window with only failing paths displayed.

![Figure 2-14: Timing Summary Report: Violating Paths Filter](image-url)
Report Clock Networks

The Report Clock Network command can be run from:

- The Flow Navigator in the Vivado IDE, or
- The Tcl command:

  ```
  report_clock_networks -name {network_1}
  ```

Report Clock Networks provides a tree view of the clock trees in the design. See Figure 2-15. Each clock tree shows the clock network from source to endpoint with the endpoints sorted by type.

![Figure 2-15: Clock Networks](image-url)
The clock trees:

- Show clocks defined by the user or generated automatically by the tool.
- Report clocks from I/O port to load.

*Note:* The full clock tree is only detailed in the GUI form of the report. The text version of this report shows only the name of the clock roots.

- Can be used to find BUFGs driving other BUFGs.
- Shows clocks driving non-clock loads.

There is a folder containing each primary clock and any generated clocks defined in the design. A separate folder displays each unconstrained clock root.

Use the filter Ports, Nets, Instances, and related buttons to reduce the amount of data displayed in the clock tree. The filter options can be viewed by clicking on the gear icon.

To view a schematic of the clock path:

1. Select an object in the tree.
2. Run the **Trace to Source** popup command.
Report Clock Interaction

To view the Clock Interaction Report, select one of the following:

- **Main Menu > Tools > Timing > Report Clock Interaction**
- **Flow Navigator > Synthesis > Report Clock Interaction**
- **Flow Navigator > Implementation > Report Clock Interaction**

Equivalent Tcl command: `report_clock_interaction -name clocks_1`

**Report Clock Interaction Dialog Box**

In the Vivado IDE, the Report Clock Interaction dialog box includes the following:

- **Results Name Field**
- **Command Field**
- **Open in a New Tab Check Box**
- **Options Tab**
- **Timer Settings Tab**

**Results Name Field**

The Results name field at the top of the Report Clock Interaction dialog box specifies the name of the graphical report that opens.

Equivalent Tcl option: `-name`

**Command Field**

Use the Command field to display the Tcl command line equivalent of the various options specified in the Report Datasheet dialog box.

**Open in a New Tab Check Box**

Use the Open in a New Tab check box to either: (1) open the results in a new tab; or (2) replace the last tab opened by the Results window.
Options Tab

The Options tab of the Report Clock Interaction dialog box contains the following:

- **Delay Type Field**
- **Significant Digits Field**
- **File Output Section**

**Delay Type Field**

Use the Delay Type field to set the type of analysis to be run.

- For synthesized designs, only max delay analysis (setup/recovery) is performed by default.
- For implemented designs, both min delay and max delay analysis (setup/hold, recover/removal) are performed by default.

To run min delay analysis only (hold and removal), select delay type `min`.

Equivalent Tcl option: `-delay_type`
**Significant Digits Field**

Use the Significant Digits field to specify the number of significant digits in the reported values. The default is three.

Equivalent Tcl option: `-significant_digits`

**File Output Section**

The File Output section includes:

- **Write Results to File**: Use the Write Results to File field to write the result to a specified file. In the Vivado IDE, the report is displayed in the Clock Interaction window.

  Equivalent Tcl option: `-file`

- **Overwrite/Append**: Select the Overwrite/Append option buttons to determine whether, when the report is written to a file: (1) the specified file is overwritten, or (2) new information is appended to an existing report.

  Equivalent Tcl option: `-append`

**Timer Settings Tab**

For details on this tab, see Timer Settings Tab, page 26.

**Details of the Clock Interaction Report**

The Clock Interaction report analyzes timing paths that cross from one clock domain (the source clock) into another clock domain (the destination clock). The Clock Interaction report helps to identify cases in which there may be data loss or metastability issues.

After you run the Report Clock Interaction command, the results open in the Clock Interaction window. As shown in the following figure, the Clock Interaction Report displays as a matrix of clock domains with the source clocks in the vertical axis and the destination clocks in the horizontal axis.
Matrix Color Coding

The tiles of the matrix are color coded. The colors of the matrix are determined by the background color of the Graphical Editors as defined under **Tools > Settings**. For more information, see this link in the *Vivado Design Suite User Guide: Using the Vivado IDE* (UG893) [Ref 1]. To hide the legend, click the ? button on the toolbar on the left of the matrix.

- **No Path - Black**: There are no timing paths that cross from the source clock to the destination clock. In this case, there is no clock interaction and nothing to report.
- **Timed - Green**: The source clock and destination clock have a synchronous relationship, and are safely timed together. This state is determined by the timing engine when the two clocks have a common primary clock and a simple period ratio.
- **User Ignored Paths - Dark Blue**: User-defined false path or clock group constraints cover all paths crossing from the source clock to the destination clock.
- **Partial False Path - Light Blue**: User-defined false path constraints cover some of the timing paths crossing from the source clock to the destination clock where the source clock and destination clock have a synchronous relationship.
- **Timed (Unsafe) - Red**: The source clock and destination clock have an asynchronous relationship. In this case, there is no common primary clock or no expandable period.
Partial False Path (Unsafe) - Orange: This category is identical to Timed (Unsafe), except that at least one path from the source clock to the destination clock is ignored due to a false path exception.

Max Delay Datapath Only - Gray: A set_max_delay -datapath_only constraint covers all paths crossing from the source clock to the destination clock.

**IMPORTANT:** The color of a cell in the matrix reflects the state of the constraints between clock domains, not the state of the timing paths worst slack between the domains. A green cell does not indicate that the timing is met, only that all timing paths that cross clock domains are properly timed, and that their clocks have a known phase relationship.

### Clock Pair Classification

The **Clock Pair Classification** column provides information about the missing common primary clock, missing common node, and missing common period between two clocks, as well as the presence of a virtual clock.

The possible values, from the highest to the lowest priority, are listed below. As soon as a condition is detected, the report command does not perform the remaining checks.

- **Ignored**: When the clock pair is entirely covered by a Clock Group, a False Path, or a Max Delay Datapath Only, the analysis is ignored.
- **Virtual Clock**: At least one of the clocks is virtual, and common primary clock or common node checks do not apply.
- **No Common Clock**: The two clocks do not have a common primary clock.
- **No Common Period**: The periods of the two clocks are not expandable.
- **Partial Common Node**: The two clocks appear synchronous, but a subset of the crossing paths do not have a common node and cannot be safely timed.
- **No Common Node**: The two clocks appear synchronous, but the crossing paths do not have a common node.
- **Clean**: None of the above conditions applies.

### Filtering the Clocks

To filter the clocks displayed in the Clock Interaction report:

1. Click on the settings button to display the **Clock Visibility**.
2. Select the clocks to display.
The **Clock Visibility** filter reduces the matrix complexity by limiting the number of clocks, but does not reduce the number of clock interactions reported in the table below the matrix. You can also show and hide the clocks that do not directly time a logical path in the design by clicking the **Hide Unused Clocks** button in the toolbar. Because these clocks do not contribute to WNS/TNS/WHS/THS computation, they are hidden by default.

The table below the matrix provides a comprehensive overview of the timing slack for setup/recovery and/or for hold/removal for source/destination clock pair. It also shows useful information about path requirement of the worst paths, common primary clock and constraints status. See **Figure 2-18**. This provides details not displayed in the matrix above.

**Clock Pairs Slack Table**

The table below the matrix provides a comprehensive overview of the timing slack for setup/recovery and/or for hold/removal for source/destination clock pair. It also shows useful information about path requirement of the worst paths, common primary clock and constraints status. See **Figure 2-18**. This provides details not displayed in the matrix above.

**Sorting the Data**

To sort the data in the table in increasing or decreasing values, single click multiple times on a column header.

**Selecting Cells and Rows**

Selecting a cell in the matrix cross-selects a specific row of the table below.

Selecting a row from the table highlights a cell in the matrix above.

**Table Columns**

The table columns are:

- **ID**: A numeric ID for the source/destination clock pair being displayed.
- **Source Clock**: The clock domain from which the path originates.
Chapter 2: Timing Analysis Features

- **Destination Clock**: The clock domain within which the path terminates.
- **Edges (WNS)**: The clock edges used to calculate the worst negative slack for max delay analysis (setup/recovery).
- **WNS (Worst Negative Slack)**: The worst slack calculated for various paths crossing the specified clock domains. A negative slack indicates a problem in which the path violates a required setup (or recovery) time.
- **TNS (Total Negative Slack)**: The sum of the worst slack violation for all the endpoints that belong to paths crossing the specified clock domains.
- **Failing Endpoints (TNS)**: The number of endpoints in the crossing paths that fail to meet timing. The sum of the violations corresponds to TNS.
- **Total Endpoints (TNS)**: The total number of endpoints in the crossing paths.
- **Path Req (WNS)**: The timing path requirement corresponding to the path reported in the WNS column. There can be several path requirements between any clock pairs if both rising and falling edges are active for at least one of the two clocks, or some timing exceptions have been applied on paths between the two clocks. The value reported in this column is not always the most challenging requirement.

For more information, see **Path Requirement, page 169**.

- **Clock Pair Classification**: Provide information about the common node and common period between the clock pair. From highest to lowest precedence: Ignored, Virtual Clock, No Common Clock, No Common Period, Partial Common Node, No Common Node, and Clean. See **Clock Pair Classification, page 45**.

- **Inter-Clock Constraints**: Shows the constraints summary for all paths between the source clock and destination clock. The possible values are listed in the **Matrix Color Coding, page 44**. Following are example definitions of these constraints:

  ```
  set_clock_groups -async -group wbClk -group usbClk
  set_false_path -from [get_clocks wbClk] -to [get_clocks cpuClk]
  ```

When the min delay analysis is also selected (hold/removal), the following columns also appear in the table:

- **Edges (WHS)**: The clock edges used to calculate the worst hold slack.
- **WHS (Worst Hold Slack)**: The worst slack calculated for various paths crossing the specified clock domains. A negative slack indicates a problem in which the path violates a required hold (or removal) time.
- **THS (Total negative Hold Slack)**: The sum of the worst slack violation for all the endpoints that belong to paths crossing the specified clock domains for min delay analysis (hold/removal).
- **Failing Endpoints (THS)**: The number of endpoints in the crossing paths that fail to meet timing. The sum of the violations corresponds to THS.
Chapter 2: Timing Analysis Features

- Total Endpoints (THS): The total number of endpoints in the crossing paths for min delay analysis (hold/removal).
- Path Req (WHS): The timing path requirement corresponding to the path reported in the WHS column. Like with WNS, there can be several possible path requirements for min delay analysis between two clocks, and the value reported in this column does not always correspond to the most challenging ones.

For more information, see Chapter 5, Performing Timing Analysis.

One or multiple clock pairs can be selected from the table. Report Timing between a selected source/destination clock pair can be run from the popup menu.

Exporting the Table

Run the Export to Spreadsheet command to export the table to an XLS file for use in a spreadsheet.

Report Pulse Width

The Pulse Width Report (shown in the figure below) checks that the design meets min period, max period, high pulse time, and low pulse time requirements for each instance clock pin. It also checks that the maximum skew requirement is met between two clock pins of the same instance in the implemented design (for example, PCIe® clocks). The pulse width slack equations do not include jitter or clock uncertainty.

Equivalent Tcl command: report_pulse_width

Note: Xilinx® Integrated Software Environment (ISE®) Design Suite implementation calls this check Component Switching Limits.

Figure 2-20: Report Pulse Width
Report Timing

Read Report Timing to view specific timing paths at any point of the flow after synthesis when: (1) you need to further investigate timing problems reported by Report Timing Summary; or (2) you want to report the validity and the coverage of particular timing constraints. Report Timing does not cover Pulse Width reports.

Running Report Timing

If a design is already loaded in memory, you can run Report Timing from the menu, the Clock Interaction Report, or the Report Timing Summary paths list.

Running Report Timing from the Menu


Running Report Timing from the Clock Interaction Report

To run Report Timing from the Clock Interaction Report:

1. Select a from/to clock pair.
2. Right-click and select Report Timing to run a report from or to the selected clocks.

Running Report Timing from a Paths List

To run Report Timing from a Paths List:

1. Select a path.
2. Right-click and select Report Timing to run a report between the selected path startpoint endpoint.

Equivalent Tcl command: report_timing

When setting specific Report Timing options, you can view the equivalent report_timing command syntax in:

- The Command field at the bottom of the dialog box, and
- The Tcl Console after execution

The report_timing options are listed along with the dialog box description in the following section.

Overall, the Report Timing options are identical to the Report Timing Summary options, plus a few additional filtering options.
Report Timing provides several filtering options that you must use in order to report a particular path or group of paths. The filters are based on the structure of a timing path.

- **Startpoints (From):** List of startpoints, such as sequential cell clock pins, sequential cells, input ports, bidirectional ports or source clock.

  If you combine several startpoints in a list, the reported paths will start from any of these netlist objects.

  The Rise/Fall filter selects a particular source clock edge.

  Equivalent Tcl option: `-from`, `-rise_from`, `-fall_from`

- **Through Points (Through):** List of pins, ports, combinational cells or nets.

  You can combine several netlist objects in one list if you want to filter on paths that traverse any of them.
You can also specify several Through options to refine your filters and report paths that traverse all groups of through points in the same order as they are listed in the command options.

The Rise/Fall filter applies to the data edge.

**RECOMMENDED: Use the default value (Rise/Fall).**

Equivalent Tcl option: `-through`, `-rise_through`, `-fall_through`

- Endpoints (To): List of endpoints, such as input data pins of sequential cells, sequential cells, output ports, bidirectional ports or destination clock.

If you combine several endpoints in a list, the reported paths will end with any of these netlist objects.

In general, the Rise/Fall option selects a particular data edge. But if you specified a destination clock, it selects a particular clock edge.

Equivalent Tcl option: `-to`, `-rise_to`, `-fall_to`

The Targets tab in the Report Timing dialog box (Figure 2-21) defines the paths from the rising clock edge of `usbClk_3`, through any of the `cpuEngine/or1200_cpu/sprs_dataout[*]` nets, to either edge of `cpuClk_5` or `sysClk`.

**Options Tab**

The Options tab contains the following options:

- **Reports**
- **Path Limits**
- **Path Display**

**Reports**

- Path delay type: See Path delay type, page 23.
- Do not report unconstrained paths: By default, Report Timing reports paths that are not constrained if no path that matches the filters (from/through/to), is constrained. Check this box if you do not want to display unconstrained paths in your report.

Equivalent Tcl option: `-no_report_unconstrained`
Chapter 2: Timing Analysis Features

Path Limits

- Number of paths per group: See Report Timing Summary, page 22.
- Number of paths per endpoint: See Report Timing Summary, page 22.
- Limit paths to group: Filters on one or more timing path groups. Each clock is associated to a group. The Vivado IDE timing engine also creates default groups such as **async_default** which groups all the paths ending with a recovery or removal timing check.

Equivalent Tcl option: -group

Path Display

- Display paths with slack greater than: Displays the reported paths based on their slack value.

Equivalent Tcl option: -slack_greater_than

- Display paths with slack less than: See Report Timing Summary, page 22.
- Number of significant digits: See Report Timing Summary, page 22.
- Sort paths by: Displays the reported paths by group (default) or by slack. When sorted by group, the N worst paths for each group and for each type of analysis (-delay_type min/max/min_max) are reported.

The groups are sorted based on their individual worst path. The group with the worst violation appears at the top of the list.

When sorted by slack, the N worst paths per type of analysis are reported (all groups combined) and are sorted by increasing slack.

Equivalent Tcl option: -sort_by

Advanced Tab

The Advanced tab has the same options as Report Timing Summary, page 22.

Timer Settings Tab

The Timer Settings tab has the same options as Report Timing Summary, page 22.
Reviewing Timing Path Details

After you click **OK** to run the report command, a new window opens. You can now review its content. You can view the N-worst paths reported for each type of selected analysis (min/max/min_max).

The following figure shows the Report Timing window in which both min and max analysis (SETUP and HOLD) were selected, and N=4.

![Report Timing Paths List](image)

*Figure 2-22: Report Timing Paths List*

Select any of these paths to view more details in the Path Properties window (Report tab).
To view the same details in a new window, double click the path.

For more information on timing path details, see Chapter 5, Performing Timing Analysis.

To access more analysis views for each path, right-click the path in the right pane and select one of the following actions:

- View the timing path Schematic.
- Rerun timing analysis on the same startpoint and endpoint of the selected path.
- Highlight the path in the Device and Schematic windows.

**Filtering Paths with Violation**

The report displays the slack value of failing paths in red. To focus on these violations, click **Show only failing checks mode**.
Report Datasheet

The Report Datasheet command reports the operating parameters of the FPGA device for use in system-level integration.

Report Datasheet Dialog Box

In the Vivado IDE, select Tools > Timing > Report Datasheet to open the Report Datasheet dialog box. See Figure 2-24.

Report Datasheet Dialog Box: Options Tab

![Report Datasheet Dialog Box: Options Tab](image)

*Figure 2-24: Report Datasheet Dialog Box: Options Tab*
Chapter 2: Timing Analysis Features

The Report Datasheet Dialog Box Options tab includes the following:

- **Results name**: Specifies the name for the returned results of the Report Datasheet command. The report opens in the Timing window of the Vivado IDE with the specified name.
  
  Equivalent Tcl option: `-name`

- **Sort by**: Sorts the results by port name or by clock name.
  
  Equivalent Tcl option: `-sort_by`

- **Report all process corners separately**: Reports the data for all defined process corners in the current design.
  
  Equivalent Tcl option: `-show_all_corners`

- **Significant digits**: Specifies the number of significant digits in the reported values. The default is three.
  
  Equivalent Tcl option: `-significant_digits`

- **Write results to file**: Write the result to the specified file name. By default the report is written to the Timing window in the Vivado IDE.
  
  Equivalent Tcl option: `-file`

- **Overwrite / Append**: When the report is written to a file, determines whether the specified file is overwritten, or new information is appended to an existing report.
  
  Equivalent Tcl option: `-append`

- **Ignore command errors**: Executes the command quietly, ignoring any command line errors and returning no messages. Returns `TCL_OK` regardless of any errors encountered during execution.
  
  Equivalent Tcl option: `-quiet`

- **Suspend message limits**: Temporarily overrides any message limits. Returns all messages from this command.
  
  Equivalent Tcl option: `-verbose`

- **Command**: Displays the Tcl command line equivalent of the various options specified in the Report Datasheet dialog box.

  - Open in a new tab: Opens the results in a new tab, or replaces the last tab opened by the Results window.
  
  - Open in Timing Analysis layout: Resets the current view layout to the Timing Analysis view layout.
Report Datasheet Dialog Box: Groups Tab

The Report Datasheet dialog box Groups tab allows you to define your own custom group of ports for analysis by specifying the reference port and additional ports to report. When Groups are not specified, the timer automatically finds the group of output ports based on the launching clock, and reports skew based on that clock.

The Report Datasheet dialog box Groups tab includes:

- **Reference**: Specifies the reference port for skew calculation. In most cases, this will be a clock port of a source synchronous output interface.

  Equivalent Tcl option: `-group`

- **Ports**: Defines additional ports to report.
  - Notice the + and - (plus and minus) buttons to the right of the Ports field.
    - The + (plus) button specifies multiple groups, each with its own reference clock port allowing you to define a new group of ports, including a new reference port.
    - The - (minus) button removes additional groups of ports as needed.

Report Datasheet Dialog Box: Timer Settings Tab

For details on this tab, see Timer Settings Tab, page 26.
Details of the Datasheet Report

General Information

This section provides details of the design and Xilinx® device, and the tool environment at the time of the report.

- Design Name: The name of the design
- Part: The target Xilinx part and speed file information
- Version: The version of the Vivado tools used when the report was generated
- Date: The date and timestamp of the report
- Command: The command line used to generate the report

Input Ports Setup/Hold

The report displays worst-case setup and hold requirements for every input port with regard to the reference clock. The internal clock used to capture the input data is also reported.

Max/Min Delays for Output Ports

Shows worst-case maximum and minimum delays for every output port with regard to the reference clock. The internal clock used to launch the output data for is also reported.

Setup Between Clocks

For every clock pair, the worst-case setup requirements are reported for all clock edge combinations.

Setup/Hold for Input Buses

Input buses are automatically inferred and their worst-case setup and hold requirements are displayed. Worst case data window for the entire bus is the sum of the largest setup and hold values. If the input ports are constrained, the slack is also reported.

An optimal tap point is reported for input clocks with IDELAY defined. The optimal tap point can be used to configure IDELAY for balanced setup and hold slack.

The source offset is the delta between two windows. The first window is defined by the setup and hold time of the input port with regard to the clock. The second window is derived from the input delay and the clock period. If the input clock is offset with this value, then it will be in the center of the window.
The following figure reports a design in which a DDR input bus, vsf_data[0:9], has a worst case data window of 1.663 ns. The ideal clock offset is 1.063 ns.

![Setup and Hold Delays for Input Buses](image)

**Figure 2-26: Setup and Hold Delays for Input Buses**

**Note:** The optimal tap point can be specified by using the Tcl command:

```
set_property IDELAY_VALUE 13 [get_cells idelay_clk]
```

### Max/Min Delays for Output Buses

Output buses are automatically inferred and their worst case maximum and minimum delays are displayed. The bus skew is also reported. For bus skew calculation, one bit is considered as the reference and the offset of every other bit is calculated with respect to this reference bit. The worst offset is the skew for the entire bus.

### Max/Min Delays for Groups

For Source Synchronous Output Interfaces, the output skew is desired with regard to the forwarded clock. A custom group report can be generated by specifying the reference port as the forwarded clock port. This table looks similar to “max/min delays for output buses” except the reference port is used as the reference bit for calculating source offset and bus skew.

**Note:** This section might be hidden if empty.

As an example, for a DDR output skew calculation, if multiple bits (for example, rldiii_a[0-19], rldiii_ba[0-3], rldiii_ref_n, rldiii_we_n) should be
grouped together with regard to the forwarded clock port \((rldiii\_ck\_n[0])\), the following command can be used:

```plaintext
report_datasheet -group [get_ports {rldiii\_ck\_n[0] rldiii\_a[*] rldiii\_ba[*] rldiii\_ref\_n rldiii\_we\_n}] -name timing_1
```

The first port in the group list is considered the reference pin.

For all these sections, the worst case data is calculated from multi-corner analysis. If \(-\text{show\_all\_corners}\) is used, the worst case data is reported for each corner separately.

The following figure shows the report data sheet for this example.

---

**Figure 2-27:** Report Data Sheet Max/Min Delay Example
Chapter 2: Timing Analysis Features

Report Exceptions

You can use the Report Exceptions command anywhere in the flow after the synthesis. The Report Exception command reports the following information:

- All the timing exceptions that have been set in the design and that are affecting timing analysis
- All the timing exceptions that have been set in the design but that are being ignored as they are overridden by other timing exception

The timing exceptions analyzed by the Report Exception command are (in the order of precedence):

- clock groups
- false paths
- max/min delays
- multicycle paths

The Report Exception is a powerful command to help debugging issues related to timing exceptions. Some designs have timing constraints with complex timing exceptions. Because the timing exceptions have different priorities, it can quickly become difficult to understand which timing exceptions might be partially or fully ignored by other exception(s). The Report Exception reports timing exceptions that are partially overridden, as well as those that are totally overridden. It also provides a hint to the overriding constraint(s).

The Report Exception command is only available through the Tcl command line, using Tcl command `report_exceptions`.

For more information about the `report_exceptions` command line options, refer to this link in the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3]. For more information about the timing exception priority order, refer to this link in the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5].

The `report_exception` command has several modes of operation:

- Reporting the timing exceptions affecting the timing analysis
- Reporting the timing exceptions being ignored
- Reporting the timing exceptions coverage
- Reporting the invalid objects specified for the `-from/-through/-to` command line options
- Writing out the timing exceptions with only the valid objects
- Writing out the timing exceptions merged by the timing engine
Example: Reporting the Timing Exceptions Affecting the Timing Analysis

This example describes how to take the design, shown in the following figure, through some timing exceptions. The design is fully constrained (clk and input/output delays defined relative to clk).

Figure 2-28: Fully Constrained Design for Timing Exception Example

The first mode of operation of the Report Exception command is report_exception.

2. In the Timing Constraints window, add the following timing exceptions to the design:

   set_multicycle_path 3 -from [get_cell int10_reg] -to [get_cell int20_reg]
   set_multicycle_path 4 -to [get_cell int20_reg]
   set_false_path -from [get_ports in6] -to [get_cell int20_reg]
   set_false_path -to [get_ports out5]
   set_false_path -to [get_cell int21_reg]
   set_max_delay 5 -to [get_ports out6]
   set_min_delay 3 -from [get_cells int10_reg] -to [get_cell int20_reg]

The Timing Constraints window displays the timing constraints applied to the design, as shown in the following figure.
The actual Exception Report (report_exception) is shown in the following figure.

![Constraints Window Displaying Timing Constraint Changes](image)

**Figure 2-29:** Constraints Window Displaying Timing Constraint Changes

The Exceptions Report contains the following information:

- The Position column indicates the constraint position number. This is the same position number reported by the Timing Constraint Window, shown in Figure 2-29.

- The From/Through/To columns indicate the patterns or objects specified with -f from/-t through/-t to command line options (including all the rise/fall versions of those options). An asterisk is displayed when the associated option was not specified.

- The Setup/Hold columns indicate whether the constraint applies to setup check, hold check, or both. The naming conventions for the Setup/Hold columns are shown in the following table:
Chapter 2: Timing Analysis Features

Table 2-1: Setup/Hold Column Naming Conventions

<table>
<thead>
<tr>
<th>Short Name</th>
<th>Timing Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>cycles=</td>
<td>set_multicycle_path</td>
</tr>
<tr>
<td>false</td>
<td>set_false_path</td>
</tr>
<tr>
<td>max=</td>
<td>set_max_delay</td>
</tr>
<tr>
<td>max_dpo=</td>
<td>set_max_delay -datapath_only</td>
</tr>
<tr>
<td>min=</td>
<td>set_min_delay</td>
</tr>
<tr>
<td>clock_group=</td>
<td>set_clock_group</td>
</tr>
</tbody>
</table>

• The Status column reports a message when a constraint is partially overridden by another timing exception. The naming conventions for the Status column are shown in the following table:

Table 2-2: Status Column Naming Conventions

<table>
<thead>
<tr>
<th>Short</th>
<th>Timing Exception</th>
</tr>
</thead>
<tbody>
<tr>
<td>MCP</td>
<td>multicycle path</td>
</tr>
<tr>
<td>FP</td>
<td>false path</td>
</tr>
<tr>
<td>MXD</td>
<td>max delay</td>
</tr>
<tr>
<td>MND</td>
<td>min delay</td>
</tr>
<tr>
<td>CG</td>
<td>clock group</td>
</tr>
</tbody>
</table>

Note: The clock group is only reported in the Status column of the report_timing -ignored command when a clock group constraint overrides another timing exception.

In this example, there are two messages regarding partially overridden constraints:

• The timing constraint position 5 (set_multicycle_path 4 -to [get_cell int20_reg] based on the Timing Constraints Window) is partially overridden by the multicycle constraint position 4 (set_multicycle_path 3 -from [get_cell int10_reg] -to [get_cell int20_reg]) and by the false path constraint position 6 (set_false_path -from [get_ports in6] -to [get_cell int20_reg]).

• The timing constraint position 10 (set_max_delay 5 -to [get_ports out6]) is partially overridden by the false path position 9 (set_false_path -from [get_ports in6] -to [get_ports out6]).
**Reporting the Timing Exceptions Being Ignored**

The second mode of operation of the Report Exception command is `report_exception -ignored`.

To illustrate, add the following timing exceptions on the top of the previous ones:

```plaintext
set_max_delay 5 -to [get_ports out5]
set_multicycle_path 1 -hold -to [get_cell int21_reg]
set_multicycle_path 2 -setup -to [get_ports out6]
set_false_path -from [get_cell int11_reg] -to [get_cell int20_reg]
```

All those exceptions are either already covered by a timing exception from the previous section (reporting the timing exceptions affecting the timing analysis) or target a non-existing path (there is no physical connection between the registers `int11_reg` and `int20_reg`).

After adding these four constraints, the Timing Constraints Window looks like Figure 2-31.

![Timing Constraints Window](image)

*Figure 2-31: Timing Constraints Window*

The Exceptions Report (`report_exception -ignored`) is as shown in the following figure:
Chapter 2: Timing Analysis Features

Note: The Status column provides some explanations why the timing exceptions are being ignored.

Reporting the Timing Exceptions Coverage

The Vivado tools can generate a detailed coverage of each valid timing exception applied to the design. All the timing exceptions are reported, including those that are fully overridden or that do not have a path between startpoints and endpoints.

The exceptions coverage report is generated using the -coverage command line option:

    report_exceptions -coverage

The report includes, for each valid timing exception, the following information:

- Constraint position number.
- Number of objects selected by the -from/-through/-to command line options.
- The coverage, expressed as a percentage, between the number of pins reached by the timing exception compared to the number of pins specified by the -from/-through/-to command line options.

Note: When cells objects are specified, Vivado tools expand the cells into valid pins objects. This cell-to-pin conversion tends to bring the coverage down because typically the timing exception only reaches a subset of pins.

Figure 2-33 shows the exceptions coverage report.
When a timing exception does not have a path between the startpoints and endpoints, the coverage report shows 0.0. In the above example, timing exception position 15 does not have a timing path. This matches the result from `report_exceptions -ignore` where constraint position 15 is reported as Non-Existent Path.

A coverage report can assist in writing effective timing exceptions. Figure 2-34 shows another example of a coverage report for the following `set_multicycle_path` constraint:

```
set_multicycle_path -setup 2 -from [all_registers] -to [get_cells cpuEngine/or1200_cpu/or1200_ctrl/ex_insn_reg[*]]
```

<table>
<thead>
<tr>
<th>Position</th>
<th>Type</th>
<th>Setup</th>
<th>Hold</th>
<th>From</th>
<th>Through</th>
<th>To</th>
<th>Endpoints</th>
<th>From (%)</th>
<th>Through (%)</th>
<th>To (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>54</td>
<td>Multicycle Path</td>
<td>cycles-2</td>
<td></td>
<td>15901 cells</td>
<td>71 cells</td>
<td>63</td>
<td>0.95</td>
<td>100.00</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Figure 2-34: Multicycle Path Coverage**

In the example shown in Figure 2-34, the coverage for the `-from` option is only 0.95% for 15901 cells objects returned by all_registers. The efficiency of the constraint can be improved by refining the list of objects specified for the `-from` option to only those objects that have a path to the cells cpuEngine/or1200_cpu/or1200_ctrl/ex_insn_reg[*].

**Reporting the Ignored Objects**

The Report Exception command can generate a list of invalid startpoints and endpoints for each of the timing exception constraints. Invalid startpoints and endpoints are ignored by the Vivado tool because timing paths can neither originate from those startpoints nor end on those endpoints. The ignored pins are reported by `report_exceptions -ignore_objects`.

**Note:** Invalid startpoints and endpoints with a Max Delay or Min Delay constraint are not ignored but result in path segmentation.

**Note:** Startpoint or endpoint pins tied to POWER or GROUND are reported in the list of ignored objects.

To illustrate, set the following timing constraints on the small example design:

```
create_clock -period 10.000 -name clk [get_ports clk]
set_false_path -from [get_cells int10_reg] -to [get_cells int20_reg]
set_false_path -from [get_pins int11_reg/*] -to [get_pins int21_reg/*]

**Note:** When the second False Path constraint is entered, the Vivado tool generates Warning Constraints 18-402 because some startpoints and endpoints are invalid.

**WARNING:** [Constraints 18-402] set_false_path: 'int11_reg/CE' is not a valid startpoint.
Resolution: A valid start point is a main or generated clock pin or port, a clock pin of a sequential cell, or a primary input or inout port. Please validate that all the objects returned by your query belong to this list.

- The first `set_false_path` constraint uses the `get_cells` command. The Vivado tool converts the cell(s) from `get_cells` into pins using only valid startpoint or endpoint pins. This ensures that the constraint refers only to valid objects.
- The second `set_false_path` constraint uses the `get_pins` command and forces all the register pins for `-from` and `-to`. This results in several invalid pins for both `-from` and `-to`.

Figure 2-35 shows the report from `report_exceptions -ignored_objects`.

```
Exceptions Report

<table>
<thead>
<tr>
<th>Position</th>
<th>Exception</th>
<th>Ignored Startpoints</th>
<th>Ignored Endpoints</th>
</tr>
</thead>
<tbody>
<tr>
<td>3</td>
<td>False Path \int1_reg/0</td>
<td>\int21_reg/0</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>False Path \int1_reg/CE</td>
<td>\int21_reg/CE</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>False Path \int1_reg/CLR</td>
<td>\int21_reg/CE</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>False Path \int1_reg/D</td>
<td>\int21_reg/0</td>
<td></td>
</tr>
</tbody>
</table>
```

Figure 2-35: Ignored Objects

Exporting the Valid Exceptions

The Report Exception command can export the list of timing exceptions. Only the constraints that cover at least one path are exported. Only valid startpoints and endpoints pins are exported while the patterns used to specify the timing exceptions are expanded inside the Vivado Design Suite Timer memory. This report can be used in conjunction with the coverage report to help refine the patterns and collections of objects used to define the timing exceptions.

Note: Timing constraints `set_clock_group` and `set_bus_skew` are not exported.

Figure 2-36 illustrates `report_exceptions -write_valid_exceptions` on the two False Path constraints explained in the section Reporting the Ignored Objects.

```
# position: 3
set_false_path \n  -from [get_pins {int10_reg/O}] \n  -to [get_pins {int30_reg/O}]

# position: 3
set_false_path \n  -from [get_pins {int11_reg/O}] \n  -to [get_pins {int21_reg/O}]
```

Figure 2-36: Valid Exceptions
Exporting the Merged Exceptions

The Report Exception command can export the list of timing exceptions as seen by the STA engine. The Vivado timing engine internally merges the timing exceptions to reduce memory and runtime. If the number of merged timing exceptions is different from the number of timing exceptions specified for the design, then this could mean that the timing exceptions are not optimally defined. The merged timing exceptions are reported with report_exceptions -write_merged_exceptions.

Note: Timing constraints set_clock_group and set_bus_skew are not exported.

Note: Invalid startpoints and endpoints are not filtered out when the merged timing exceptions are exported.

Figure 2-37 illustrates the report_exceptions -write_merged_exceptions on the two False Path constraints explained in the section Reporting the Ignored Objects. The second False Path includes all the registers pins because the pattern for -from/-to for the get_pins command is int21_reg/*. 

```
set_false_path \
    -from [get_pins {int10_reg/C}] \ 
    -to [list [get_pins {int20_reg/CE}] \ 
             [get_pins {int20_reg/C(R)}] \ 
             [get_pins {int20_reg/O}]]

set_false_path \
    -from [list [get_pins {int11_reg/C}] \ 
             [get_pins {int11_reg/CE}] \ 
             [get_pins {int11_reg/C(R)}] \ 
             [get_pins {int11_reg/O}]] \ 
    -to [list [get_pins {int21_reg/C}] \ 
             [get_pins {int21_reg/CE}] \ 
             [get_pins {int21_reg/C(R)}] \ 
             [get_pins {int21_reg/O}]]
```

Figure 2-37: Merged Exceptions

Report Clock Domain Crossings

The Clock Domain Crossings (CDC) report performs a structural analysis of the clock domain crossings in your design. You can use this information to identify potentially unsafe CDCs, which will lead to metastability or data coherency issues. While the CDC report is similar to the Clock Interaction Report, the CDC report focuses on structures and their timing constraints, but does not provide information related to timing slack.
Overview

Before generating the CDC report, you must ensure that the design has been properly constrained and there are no missing clock definitions. Report CDC only analyzes and reports paths where both source and destination clocks have been defined. Report CDC performs structural analysis:

- On all paths between asynchronous clocks.
- Only on paths between synchronous clocks that have the following timing exceptions:
  - Clock groups
  - False Path
  - Max Delay Datapath Only

Synchronous clock paths with no such timing exception are assumed to be safely timed and are not analyzed by the CDC engine. The Report CDC operates without taking into consideration any net or cell delays.

Terminology

The terminology for safe, unsafe, and endpoints is different in the context of Cross Domain Crossing (CDC) and inter-clock timing analysis.

In the context of CDC, an asynchronous crossing is safe when proper synchronization circuitry is used to prevent metastability. For example, a safe single-bit CDC can be implemented by a synchronizer, which is a chain of registers with same clock and control signals. A safe multi-bit CDC can be implemented with a MUX Hold circuitry or a Clock Enabled Controlled circuitry.

Conversely, an unsafe CDC is when the CDC analysis engine does not recognize a known safe synchronization circuit on an asynchronous CDC path.

The number of endpoints reported for CDC between two clock domains can be different than the number of endpoints reported by the timing analysis commands. For example, an asynchronous reset synchronizer involves multiple timing path endpoints. However, the synchronization circuitry is reported as a single element and therefore as a single CDC endpoint. Similarly, a multi-bit CDC contains multiple single bit crossings but is reported as a single CDC endpoint. However, the same bus is reported as multiple timing endpoints by other timing reports.

IMPORTANT: Because report_clock_interaction and report_cdc have different purposes, do not compare the number of endpoints reported by each command. In the context of report_clock_interaction, safe/unsafe refers to the ability for the timing analysis engine to provide a slack that matches the worst situation in hardware. For report_cdc, safe/unsafe refers to the type of CDC circuitry implemented in the design.
Running Report Clock Domain Crossings

When you run Report CDC from the Vivado IDE, it provides all the details for the CDC paths between the specified clocks by default. When you run Report CDC from the Tcl Console, however, it only prints the Summary by Clock Pairs table. You must specify the -details option in order to report all the details as in the GUI mode. Reporting the details can create very long files or log files.

To run the Report Clock Domain Crossings in the Vivado IDE, select Tools > Timing > Report CDC.

Equivalent Tcl command: report_cdc -name cdc_1

In the Vivado IDE, the Report CDC dialog box includes the following fields, as shown in Figure 2-38:

- Results Name Field
- Clocks Field (From/To)
- File Output Field
- Options Field

![Report CDC Dialog Box](image)

*Figure 2-38: Report CDC Dialog Box*
Results Name Field

In the Results Name field at the top of the Report Clock Domain Crossings dialog box, specify the name of the graphical window for the report.

Equivalent Tcl option: -name <windowName>

Clocks Field (From/To)

The Clocks To and From fields allow you to optionally specify the source and/or destination clocks on which to run the CDC analysis. You can use the From/To options to control the scope of Report CDC to specific clocks and result in more readable reports. Click the Browse button to the right to open a search dialog box to aid in finding clock objects.

Equivalent Tcl option: -from <clockNames> -to <clockNames>

File Output Field

The File Output field allows you to optionally specify a file into which to write the results. You can overwrite the file or append to it.

Equivalent Tcl option: -file <fileName> -append

Options Field

The Options field allows you to:

- Suspend message limits during command execution
  
  Equivalent Tcl option: -verbose

- Ignore command errors
  
  Equivalent Tcl option: -quiet

Understanding the Clock Domain Crossings Report Rules

Report CDC tries to match each CDC path to a known CDC topology. Each CDC topology is associated with one or several CDC rules, as presented in Table 2-3. Note that you cannot modify the severity of the rules as with DRCs and Messages. Simplified schematics and descriptions of the CDC Topologies being detected are included in Simplified Schematics of the CDC Topologies, page 79.
### Table 2-3: CDC Rules and Description

<table>
<thead>
<tr>
<th>CDC Topology</th>
<th>CDC Rule</th>
<th>Severity</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-bit CDC</td>
<td>CDC-1</td>
<td>Critical</td>
<td>A single-bit CDC path is not synchronized or has unknown CDC circuitry.</td>
</tr>
<tr>
<td></td>
<td>CDC-2</td>
<td>Warning</td>
<td>A single-bit CDC path is synchronized with a 2+ stage synchronizer but the ASYNC_REG property is missing on all or some of the synchronizer flip-flops.</td>
</tr>
<tr>
<td></td>
<td>CDC-3</td>
<td>Info</td>
<td>A single-bit CDC path is synchronized with a 2+ stage synchronizer and the ASYNC_REG property is present.</td>
</tr>
<tr>
<td>Multi-bit CDC</td>
<td>CDC-4</td>
<td>Critical</td>
<td>A multi-bit bus CDC path is not synchronized or has unknown CDC circuitry.</td>
</tr>
<tr>
<td></td>
<td>CDC-5</td>
<td>Warning</td>
<td>A multi-bit bus CDC path is synchronized with a 2+ stage synchronizer but the ASYNC_REG property is missing on all or some of the synchronizer flip-flops.</td>
</tr>
<tr>
<td></td>
<td>CDC-6</td>
<td>Warning</td>
<td>A multi-bit bus CDC path is synchronized with a 2+ stage synchronizer and the ASYNC_REG property is present.</td>
</tr>
<tr>
<td>Asynchronous Reset</td>
<td>CDC-7</td>
<td>Critical</td>
<td>An asynchronous signal (clear or preset) is not synchronized or has unknown CDC circuitry.</td>
</tr>
<tr>
<td></td>
<td>CDC-8</td>
<td>Warning</td>
<td>An asynchronous signal (clear or preset) is synchronized but the ASYNC_REG property is missing on all or some of the synchronizer flip-flops.</td>
</tr>
<tr>
<td></td>
<td>CDC-9</td>
<td>Info</td>
<td>An asynchronous reset is synchronized and the ASYNC_REG property is present.</td>
</tr>
<tr>
<td>Combinatorial Logic</td>
<td>CDC-10</td>
<td>Critical</td>
<td>Combinatorial logic has been detected in the fanin of a synchronization circuit.</td>
</tr>
<tr>
<td>Fanout</td>
<td>CDC-11</td>
<td>Critical</td>
<td>A fanout has been detected before a synchronization circuit.</td>
</tr>
<tr>
<td>Multi-Clock Fanin</td>
<td>CDC-12</td>
<td>Critical</td>
<td>Data from multiple clocks are found in the fanin of a synchronization circuit.</td>
</tr>
<tr>
<td>non-FD primitive</td>
<td>CDC-13</td>
<td>Critical</td>
<td>CDC detected on a non-FD primitive.</td>
</tr>
<tr>
<td>CE-controlled CDC</td>
<td>CDC-1</td>
<td>Warning</td>
<td>Clock Enable controlled CDC.</td>
</tr>
<tr>
<td>Mux-controlled CDC</td>
<td>CDC-2</td>
<td>Warning</td>
<td>Multiplexer controlled CDC.</td>
</tr>
<tr>
<td>Mux Data Hold CDC</td>
<td>CDC-3</td>
<td>Warning</td>
<td>Multiplexer data holding CDC.</td>
</tr>
<tr>
<td>HARD_SYNC primitive</td>
<td>CDC-18</td>
<td>Info</td>
<td>A signal is synchronized with a HARD_SYNC primitive.</td>
</tr>
</tbody>
</table>

### Reviewing the Clock Domain Crossings Report Sections

In the GUI mode, three sections are generated by default:

- **Summary by Clock Pair**
- **Summary by Type**
- **Detailed Report**
The summary sections provide a convenient overview of the issues that need review and possibly a change in the design. These sections can be used to navigate to the violations of highest Severity where additional information is contained within the Detailed Report section.

**Note:** By default, only the Summary by clock pair section is generated when running the report in text mode.

### Summary by Clock Pair

In the Summary (by clock pair) section, useful information about the number of CDC paths between two clocks are presented, along with the severity of the most critical issue found among these paths. The table includes the following columns:

- **Severity:** Reports the worst severity of all CDC paths from/to the listed clocks. Values are Info, Warning, or Critical.
- **Source Clock:** Shows the name of the CDC Source Clock.
- **Destination Clock:** Shows the name of the CDC Destination Clock.
- **CDC Type:** Reflects the relationship between two clocks and their dominant timing exception, if any. Possible types are:
  - Safely Timed: All CDC paths are safely timed because the clocks are synchronous and accurate timing is not prevented by a timing exception.
  - User Ignored: All CDC paths are covered by `set_false_path` or `set_clock_groups`.
  - No Common Primary Clock: The CDC clocks are asynchronous and at least 1 CDC path is normally timed between two clocks that do not have a common primary clock.
  - No Common Period: The CDC clocks are asynchronous and at least 1 CDC path is normally timed between two clocks that do not have a common period. For the definition of clocks with no common period, refer to Understanding the Basics of Timing Analysis, page 165.
- **Exceptions:** The timing exceptions applied to the CDC (if any) are:
  - None: No timing exceptions exist on the CDC paths.
  - Asynch Clock Groups: The `set_clock_groups -asynchronous` exception was applied to the CDC clocks.
  - Exclusive Clock Groups: The `set_clock_groups -exclusive` exception was applied to the CDC clocks.
  - False Path: The `set_false_path` exception was applied to from/to the CDC clocks or to all CDC paths.

<table>
<thead>
<tr>
<th>Severity</th>
<th>Source Clock</th>
<th>Destination Clock</th>
<th>CDC Type</th>
<th>Exceptions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Info</td>
<td></td>
<td></td>
<td>Safely Timed</td>
<td>None</td>
</tr>
<tr>
<td>Warning</td>
<td></td>
<td></td>
<td>User Ignored</td>
<td>Asynch Clock Groups</td>
</tr>
<tr>
<td>Critical</td>
<td></td>
<td></td>
<td>No Common Primary Clock</td>
<td>Exclusive Clock Groups</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>No Common Period</td>
<td>False Path</td>
</tr>
</tbody>
</table>
• Max Delay Datapath Only: The `set_max_delay -datapath_only` exception was applied to all CDC paths. Note that “Max Delay Datapath Only” is reported when at least one CDC path is only covered by `set_max_delay -datapath_only`, while all other CDC paths are ignored due to `set_false_path` constraints.

• Partial Exceptions: A mix of `set_false_path` and `set_max_delay -datapath_only` constraints are applied to some of the CDC paths, and at least one CDC path is normally timed.

• Endpoints: The total number of CDC path endpoints. This is the sum of Safe, Unsafe, and Unknown endpoints. In this context, an endpoint is a sequential cell input data pin. An FD cell can be counted several times depending on the D, CE, and SET/RESET/CLEAR/PRESET connectivity. For some CDC topologies, only one endpoint is counted while there are effectively several paths crossing the clock domain boundary to reach the CDC structure. For example, in an asynchronous reset synchronizer, several CLEAR pins are connected to the crossing net, but only the first pin of the synchronizer chain is counted.

• Safe: The number of safe CDC path endpoints. Safe endpoints are endpoints on CDC paths identified as:
  - Asynchronous Clocks with known Safe CDC structures
  - Synchronous Clocks with exceptions and known Safe CDC structures
  - Synchronous Clocks without exceptions that are safely timed regardless of the CDC structure
  - CDC synchronized with `HARD_SYNC` macro

• Unsafe: The number of CDC path endpoints that are recognized as having an unsafe structure. The unsafe endpoints are CDC-10, CDC-11, CDC-12 and CDC-13.
  - Combinatorial Logic Topology
  - Fanout Topology
  - Multi-Clock Fan-in Topology
  - non-FD primitive Topology

• Unknown: The number of unknown CDC path endpoints. No CDC structure can be matched on these endpoints or an unknown CDC circuitry has been detected (CDC-1, CDC-4 and CDC-7).

• No ASYNC_REG: The number of identified synchronizers that are missing the `ASYNC_REG` property on at least one of the two first FD cells of the chain.

The following figure shows an example of a Summary by clock pair section.
Summary by Type

The Summary by Type table is convenient for quickly reviewing the nature of CDC structures found in the current report. An example is shown in Figure 2-40.

The Summary by Type table includes the following columns:

- **Severity**: Reports the severity of the CDC Rule as Info, Warning, or Critical.
- **ID**: Unique identification number of the CDC Rule, as listed in Table 2-3.
- **Count**: Number of occurrences of the CDC Rule in the entire report.
- **Description**: Short description of the CDC Rule.
When analyzing the summary tables, it is important to start with the highest severity. Severity levels are:

- **Critical:** This severity is for CDC paths with unknown or unsafe CDC Structures. You must review each individual path to either fix the structure by modifying the RTL, or waive the issue. The path details are generated by default when using the Vivado IDE, and only when `-details` is used with `report_cdc` on the command line.
  - There is some combinatorial logic on the crossing net or several source clocks are found in the fanin of the crossing net. This can degrade the Mean Time Between Failures (MTBF) characteristics.
  - There is a fanout on the crossing net to the same destination clock domain. This can lead to data coherency problems.

- **Warning:** This severity is for CDC paths with known CDC Structures that are safe but non-ideal due to one of the following reasons:
  - At least one of the two first synchronizer flip-flops does not have the `ASYNC_REG` property set to 1 (or true)
  - The CDC structure identified requires functional correctness that the CDC engine cannot verify. These structures are Clock Enable Controlled, MUX Controlled, and MUX Data-Hold controlled CDC topologies.

- **Info:** This severity indicates that CDC structures are all safe and properly constrained.

**Detailed Report**

The Report CDC details can be viewed by looking at the CDC Details section in the report. You can use the detailed report to view the schematic of the selected path (by pressing the `F4` key), view the timing report, or generate a new timing report by right-clicking on the individual entry.

You can use the timing reports and schematics to review unexpected CDC paths in the design, to identify incorrect or missing timing exceptions, and to find missing `ASYNC_REG` properties. An example of the CDC Detailed Report is shown in the following figure.

![Figure 2-41: CDC Detailed Report](Image)
The CDC Detailed Report table includes the following columns:

- **Severity**: Reports the severity of the CDC Rule as Info, Warning, or Critical.
- **ID**: The unique identification number of the CDC Rule, as listed in Table 2-3, page 73.
- **Description**: A short description of the CDC Rule.
- **Depth**: The number of synchronizer stages found (only applies to synchronizer topologies).
- **Exception**: The timing exception applied to the CDC path.
- **Source (From)**: The CDC timing path startpoint.
- **Destination (To)**: The CDC timing path endpoint.
- **Category**: Displays Safe, Unsafe, Unknown, etc.
- **Source Clock (From)**: The name of the source clock.

*Note:* This column displays only when you click **CDC Details** (left column of Timing-Report CDC window)

- **Destination Clock (To)**: The name of the destination clock.

*Note:* This column displays only when you click **CDC Details** (left column of Timing-Report CDC window)

**IMPORTANT:** The CDC report can flag issues in some of the Xilinx IPs because the CDC engine does not recognize all possible CDC topologies and does not provide a built-in waiver mechanism. More information can be found in each Xilinx IP Product Guide.
Simplified Schematics of the CDC Topologies

Simplified schematics of the CDC Topologies along with brief descriptions are shown in the following sections. In all schematics, the Source Clock net (typically clka) is highlighted in blue and the Destination Clock net (typically clkb) is highlighted in orange.

**Single-Bit Synchronizer**

The simplified topology of a Single-bit synchronizer is shown in Figure 2-42. The async_reg property must be set on at least the first two flip flops of the synchronization chain. The synchronizer depth is defined by the number of chained flip-flops that share the same control signals.

If the CLEAR or PRESET pins of the flip-flops are also connected to an asynchronous source, the synchronizer is only reported as a single-bit synchronizer and not as an asynchronous reset synchronizer.
**Multi-Bit Synchronizer**

The multi-bit synchronizer topology that is detected is equivalent to multiple single-bit synchronizers grouped together based on the startpoint-endpoint names and matching CDC rules. In this context, a bus is defined by the startpoint and endpoint cell names and not by the net names. The expected bus name format is `baseName[index]`. Also the startpoint and endpoint indexes must match. The following figure shows an example of a multi-bit synchronizer that is 2 bits wide.

![Multi-Bit Synchronizer with 2-Bit Width](image)

*Figure 2-43: Multi-Bit Synchronizer with 2-Bit Width*

If all bits of a CDC bus do not match the same CDC rule, the bus is reported as single bits or bus segments with continuous indexes that match a same CDC rule.

It is essential to understand that having a register-based synchronizer on a bus does not make the domain crossing safe for the bus. This is the reason the CDC rule CDC-6 is a Warning, as the tool cannot decide whether or not the topology is adequate for the design. It is up to the designer to confirm the safety of the CDC.

If the bus is Gray coded, it is safe to use a register-based synchronizer on all the bits of the bus as long as the adequate timing constraints have been set on the bus to make sure that no more than one data at a time can be captured by the receiving domain.

If the bus is not Gray coded, other synchronizer topologies should be used instead, such as CE Controlled CDC or MUX Controlled CDC.

**Asynchronous Reset Synchronizer**

The synchronization of an asynchronous reset is shown in the following figure for CLEAR-based synchronization, and in Figure 2-45 for PRESET-based synchronization. The FF1 cell is respectively connected to the synchronized clear or preset signals and their deassertion can safely be timed against `clk_a`. Note that flip-flops with CLEAR and PRESET cannot be mixed within an asynchronous reset synchronizer.
The general recommendation is to avoid multiple synchronizations of the reset signal inside the destination clock domain. This means that there should not be any fanout of the reset from the source clock domain into the destination clock domain. This recommendation prevents the destination clock domain to come out of reset at different time which could
put the design in an unknown state. Failing to follow this recommendation results in a critical CDC-11 Fan-out from launch flop to destination clock violation.

However, there are scenarios involving the FIFO Generator IP where it is safe to have multiple synchronizations of the reset signal inside the destination clock domain. The FIFO Generator enters the reset state asynchronously and comes out synchronously. It applies true synchronous reset to BRAM though the FIFO receives the asynchronous reset. There will not be a situation where some part of logic is out of reset and some part is still in reset as long as its wr_rst_busy signal is used by the design to hold the data flow.

The AXI interface uses 5 FIFO Generator IPs to synchronize the reset in each of the destination clock domains and is another example of a reset circuitry that is safe by construction. In those scenarios when it is safe to synchronize the reset signal multiple times, the CDC-11 violations can be ignored.

**Figure 2-46** illustrates an example of safe reset synchronization involving two FIFO Generators in the same destination clock domain.
**Combinatorial Logic**

In the combinatorial logic simplified example presented in the following figure, a logic function represented by the LUT3 is placed between the CDC from `clk_a` to `clk_b` synchronizers.

![Combinatorial Logic Simplified Example](image)

**Figure 2-47: Combinatorial Logic Simplified Example**

This structure is traditionally not recommended due the potential occurrence of glitches on the output of the combinatorial logic, which is captured by the synchronizer and propagated downward to the rest of the design.
**Fanout**

In the simplified Fanout example shown in the following figure, the source flip-flop drives a net that is synchronized three times in the `clk_b` domain highlighted in red. This structure is not recommended as it can lead to data coherency issues in the destination clock domain because the latency through the synchronizers is bounded but not cycle-accurate.

*Note:* A fanout of $N$ to $N$ different clock domains is not a CDC problem and does not trigger a CDC-11 violation. Refer to the section Asynchronous Reset Synchronizer for examples of safe fanout on reset signal.

*Figure 2-48: Simplified Fanout Example*
Multi-Clock Fanin

In the Multi-Clock Fanin example shown in the following figure, both $\text{clk}_a$ and $\text{clk}_x$ are transferring data through combinatorial logic (LUT2) to the synchronizer circuit in the $\text{clk}_b$ domain. It is recommended to first synchronize the source data from $\text{clk}_a$ and $\text{clk}_x$ individually before combining them via some glue logic. This improves the MTBF characteristics of the overall CDC structure, and it prevents glitches to propagate to the destination clock domain.

![Multi-Clock Fanin Example](Xilinx Diagram)

*Figure 2-49: Multi-Clock Fanin Example*
Non-FD Primitive

In the Non-FD Primitive example presented in the following figure, a CDC is occurring between a FDRE and a RAMB while no synchronization logic exists inside the RAMB primitive. Even if a single stage flip-flop connected to clk_b is inserted in front of the RAMB, it is still considered an inadequate synchronizer due to the routing distance between the FDRE and RAMB cells.

Figure 2-50:  Non-FD Primitive Example

Note: This rule does not include the HARD_SYNC macro, which is detected and covered by CDC-18.
**CE-controlled CDC**

In the CE-controlled CDC example shown in the following figure, the clock enable signal is synchronized in the destination `clk_b` domain before being used to control the crossing flip-flops.

![CE-Controlled CDC Example](image)

**Figure 2-51:  CE-Controlled CDC Example**

The CDC engine only checks that the signal connected to FF3/CE is also launched by `clk_b`. There is no restriction on how the clock enable signal is synchronized, as long as it is separately reported as a safe CDC path. Also, you are responsible for constraining the latency from the `clk_a` domain to FF3, which is usually done by a `set_max_delay -datapath_only` constraint.
**Mux-Controlled CDC**

In the Mux-controlled CDC example, shown in the following figure, the multiplexer select signal is synchronized to the destination clock domain, `clk_b`.

![Mux-Controlled CDC Example](image)

*Figure 2-52:  Mux-Controlled CDC Example*

Similar to CE-controlled CDC, there is no restriction on how the select signal is synchronized as long as it is reported as safe individually and the user is responsible for constraining the crossing delay on `FF2_c`. 
**Mux Data Hold CDC**

In the Mux Data Hold CDC example, presented in the following figure, the multiplexer select signal is synchronized to the destination clock domain `clk_b` and the `data_out` is fed back to the multiplexer.

![Mux Data Hold CDC Example](image)

**Figure 2-53: Mux Data Hold CDC Example**

Similar to CE-controlled CDC, there is no restriction on how the multiplexer select signal is synchronized as long as it is reported as safe individually and the user is responsible for constraining the crossing delay on `FF2_c`. 
Report Bus Skew

The Bus Skew report covers all the bus skew constraints set in the design using set_bus_skew.

Because the bus skew report is not, at this time, included inside the timing summary report, you must manually generate the bus skew report in addition to the timing summary report for complete timing signoff.

Running Report Bus Skew

The bus skew report is only available from the command line with the report_bus_skew Tcl command. The command shares many options with the report_timing command to filter and format the output report.

Reviewing Bus Skew Path Details

The bus skew report includes two sections:

1. A bus skew report summary.

Report Summary Section

The Report Summary section reports all the set_bus_skew constraints defined in the design. The following information is reported for each constraint:

- Id: constraint Id referred later in the report (makes it easier to search for that constraint inside the report).
- From: pattern provided for the set_bus_skew -from option.
- To: pattern provided for the set_bus_skew -to option.
- Corner: corner (Slow or Fast) in which the worst bus skew was computed.
- Requirement: bus skew target value.
- Actual: worst bus skew computed across all the paths covered by the constraint.
- Slack: difference between the worst bus skew and the constraint requirement.

In the following example, the design has only one bus skew constraint with a 1 ns requirement. The worst skew among all the paths covered by the constraint is 1.107 ns.
Chapter 2: Timing Analysis Features

Report Per Constraint Section

The Report Per Constraint section provides more details for each of the set_bus_skew constraints. Each reported constraint includes two parts:

1. Detailed summary of the paths covered by the constraint.
2. Detailed timing paths for the paths reported in the Per Constraint summary.

The detailed summary table provides the following information:

- From Clock: startpoints clock domain.
- To Clock: endpoints clock domain.
- Endpoint Pin: endpoint pin involved in the reported path.
- Reference Pin: reference pin used to compute the skew. Each row of this table can refer to a different reference pin.
- Corner: Fast/Slow corner used to compute the worst skew to this endpoint.
- Actual: computed skew. The skew is the difference between the relative delay for Endpoint Pin minus the relative delay for Reference Pin and minus the relative CRPR.
- Slack: difference between actual path skew and requirement.

**Note:** Both the -from and -to options must be specified when defining a bus skew constraint.

By default, only the endpoint with the worst bus skew is reported. To report multiple endpoints, the command line options -max_paths and -nworst can be used. They work similarly as for report_timing command. For example, the combination of -nworst 1 -max_path 16 reports, for each constraint, up to 16 endpoints with a single path per endpoint.

1. Bus Skew Report Summary
   ---------------------------------

<table>
<thead>
<tr>
<th>Id</th>
<th>From</th>
<th>To</th>
<th>Corner</th>
<th>Requirement(ns)</th>
<th>Actual(ns)</th>
<th>Slack(ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4</td>
<td>get_pins (data[reg]*[/C])</td>
<td>get_pins (data[reg]*[/D])</td>
<td>Slow</td>
<td>1.000</td>
<td>1.107</td>
</tr>
</tbody>
</table>

2. Bus Skew Report Per Constraint
   ---------------------------------

   Id: 1
   set_bus_skew -from [get_pins {data[reg][*][/C]}] -to [get_pins {data[reg][*][/D]}] 1.000
   Requirement: 1.000ns

<table>
<thead>
<tr>
<th>From Clock</th>
<th>To Clock</th>
<th>Endpoint Pin</th>
<th>Reference Pin</th>
<th>Corner</th>
<th>Actual(ns)</th>
<th>Slack(ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>clk1</td>
<td>clk2</td>
<td>data[reg][1]/D</td>
<td>data[reg][2]/D</td>
<td>Slow</td>
<td>1.107</td>
<td>-0.107</td>
</tr>
<tr>
<td>clk1</td>
<td>clk2</td>
<td>data[reg][2]/D</td>
<td>data[reg][1]/D</td>
<td>Slow</td>
<td>1.107</td>
<td>-0.107</td>
</tr>
<tr>
<td>clk1</td>
<td>clk2</td>
<td>data[reg][3]/D</td>
<td>data[reg][2]/D</td>
<td>Slow</td>
<td>0.986</td>
<td>0.014</td>
</tr>
<tr>
<td>clk1</td>
<td>clk2</td>
<td>data[reg][2]/D</td>
<td>data[reg][3]/D</td>
<td>Slow</td>
<td>0.929</td>
<td>0.071</td>
</tr>
</tbody>
</table>
The detailed timing paths section provides a detailed timing path for each of the pin pairs reported in the Per Constraint summary table. The number of detailed paths that are reported is the same as the number of endpoints reported in the summary table and can be controlled with -max_paths/-nworst command line options.

The format for the detailed bus skew timing path is similar to a traditional timing path, except for the launch time of the destination clock, which is always zero. For each slack, a timing path to the endpoint and a timing path to the reference pin are printed.

The following detailed path was reported using the command line option -path_type short to collapse the clock network details. The path to the endpoint pin precedes the path to the reference pin. The path header summarizes the information from the two detailed paths, plus the requirement and the relative CRPR:
### Slack (VIOLATED):
-0.107ns (requirement - actual skew)

### Endpoint Source:
- `datal_reg[1]/C`
  - (rising edge-triggered cell FDRE clocked by clk1)

### Endpoint Destination:
- `datal_reg[1]/D`
  - (rising edge-triggered cell FDRE clocked by clk1)

### Reference Source:
- `datal_reg[2]/C`
  - (rising edge-triggered cell FDRE clocked by clk1)

### Reference Destination:
- `datal_reg[2]/D`
  - (rising edge-triggered cell FDRE clocked by clk1)

### Path Type:
- Bus Skew (Max at Slow Process Corner)

### Requirement:
- 1.000ns

### Endpoint Relative Delay:
- 1.137ns

### Reference Relative Delay:
- -0.550ns

### Relative CRPR:
- 0.581ns

### Actual Bus Skew:
- 1.107ns (Endpoint Relative Delay - Reference Relative Delay - Relative CRPR)

<table>
<thead>
<tr>
<th>Endpoint path:</th>
<th>Location</th>
<th>Delay type</th>
<th>Incr(ns)</th>
<th>Path(ns)</th>
<th>Netlist Resource(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>(clock clk1 rise edge)</code></td>
<td><code>propagated clock network latency</code></td>
<td>0.000</td>
<td>0.000</td>
<td><code>r</code></td>
<td></td>
</tr>
<tr>
<td><code>SLICE_X1Y3</code></td>
<td><code>FDRE</code></td>
<td>0.000</td>
<td>5.373</td>
<td><code>r</code></td>
<td></td>
</tr>
<tr>
<td><code>SLICE_X1Y3</code></td>
<td><code>FDRE</code></td>
<td>0.223</td>
<td>5.396</td>
<td><code>r</code></td>
<td></td>
</tr>
<tr>
<td><code>SLICE_X0Y3</code></td>
<td><code>net (fc=1, routed)</code></td>
<td>0.452</td>
<td>6.079</td>
<td><code>r</code></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Reference path:</th>
<th>Location</th>
<th>Delay type</th>
<th>Incr(ns)</th>
<th>Path(ns)</th>
<th>Netlist Resource(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>(clock clk1 rise edge)</code></td>
<td><code>propagated clock network latency</code></td>
<td>0.000</td>
<td>0.000</td>
<td><code>r</code></td>
<td></td>
</tr>
<tr>
<td><code>SLICE_X1Y8</code></td>
<td><code>FDRE</code></td>
<td>4.248</td>
<td>4.248</td>
<td><code>r</code></td>
<td></td>
</tr>
<tr>
<td><code>SLICE_X1Y8</code></td>
<td><code>FDRE</code></td>
<td>0.189</td>
<td>4.137</td>
<td><code>r</code></td>
<td></td>
</tr>
<tr>
<td><code>SLICE_X0Y3</code></td>
<td><code>net (fc=1, estimated)</code></td>
<td>0.459</td>
<td>4.896</td>
<td><code>r</code></td>
<td></td>
</tr>
</tbody>
</table>

Data arrival: 6.079
Clock arrival: 4.941
Relative delay: 1.137

Data arrival: 4.96
Clock arrival: 4.446
Relative delay: -0.550
Chapter 3

Implementation Results Analysis Features

Using the Design Runs Window

The Design Runs window displays the state of the current runs.

For more information, see this link in the Vivado Design Suite User Guide: Using the Vivado IDE (UG893) [Ref 1].

If the run is running, finished cleanly, or finished with errors, the Design Runs window appears when a run is done.

**TIP:** If the run is not up to date, you can select **Force Up-to-Date** from the pop-up menu.

The Design Runs Window columns show:

- The name of the run
- The target part
- The constraints set associated with a run
- The run strategy
- The status of the last completed step of a run
- The progress of a run
- The start time of a run
- The elapsed time of a run during execution or the final runtime of a completed run
• The timing score of a run: WNS, TNS, WHS, THS and TPWS (see Report Timing Summary in Chapter 2 for more information on these numbers). This is where you can quickly verify that a run meets timing. If it does not meet timing, you must start the analysis with the Timing Summary Report.

• The number of nets that were not successfully routed

• The utilization of the design LUT, FF, BRAMs, DSP, and if applicable, URAMs.

• The total power estimate

• A brief description of the run strategy

If you are using the Vivado® IDE project flow, review the Messages tab for your active synthesis and implementation runs. Messages are grouped by run steps in the flow. All the information saved in the run log files, and the main Vivado session log file, appear in this consolidated and filtered view.

Some messages crossprobe back to a source file that can always be opened by clicking on the file name, or in some cases to a design object related to the message. Depending on which step of the flow you are analyzing, you must open either the synthesized design or the implemented design in order to be able use the object crossprobing from the message.
Placement Analysis

This section discusses Placement Analysis and includes:

- Highlighting Placement
- Showing Connectivity
- Viewing Metrics

Highlighting Placement

Another way to review design placement is to analyze cell placement. The Highlight Leaf Cells command helps in this analysis.

1. In the Netlist Window, select the levels of hierarchy to analyze.
2. From the popup menu, select Highlight Leaf Cells > Select a color.
3. If you select multiple levels of hierarchy, select Cycle Colors.

The leaf cells that make up the hierarchical cells are color coded in the Device window.

**Figure 3-3: Highlight Hierarchy**
The color coding shows the placement of the key hierarchical blocks in the device. The `usbEngine0` (in blue):

- Uses a number of Block RAM and DSP48 cells.
- Is in the middle clock regions of the chip.
- Is intermingled with other logic (`fftEngine`) in the design.

It is easy to see that the `fftEngine` (in green) and the `cpuEngine` (in yellow) are intermingled. The two blocks primarily use different resources (DSP48 as opposed to slices). Intermingling makes best use of the device.

### Showing Connectivity

It can be useful to analyze a design based on connectivity. Run **Show Connectivity** to review the placement of all logic driven by an input, a Block RAM, or a bank of DSPs. Show Connectivity takes a set of cells or nets as a seed, and selects objects of the other type.

**TIP:** *Use this technique to build up and see cones of logic inside the design.*

Figure 3-4 shows a Block RAM driving logic inside the device including OBUFs. A synthesis pragma stops synthesis from placing the output flop in the Block RAM during memory inferencing.
Fixed and Unfixed Logic

The Vivado tools track two different types of placement:

- Elements placed by the user (shown in orange) are Fixed.
  - Fixed logic is stored in the XDC.
  - Fixed logic normally has a LOC constraint and might have a BEL constraint.
- Elements placed by the tool (shown in blue) are Unfixed.

In Figure 3-5, the I/O and Block RAM placement is Fixed. The slice logic is Unfixed.
Cross Probing

For designs synthesized with Vivado Synthesis, it is possible to cross probe back to the source files once the netlist design is in memory.

To cross probe:

1. Select the gate.
2. Select Go to Source from the popup menu, shown in the Figure 3-6.
Use cross probing to determine which source is involved in netlist gates. Due to the nature of synthesis transforms, it is not possible to cross probe back to source for every gate in the design.
Viewing Metrics

After implementation finishes, you may want to analyze the design to see how it interacts with the device. The Vivado IDE has a number of metrics to help you determine logic and routing usage inside the device. The Metrics color code the device window based on a specified rule. To view a metric, right-click in the Device window, select Metric, and then select the metric you would like to view. See Figure 3-7.

Figure 3-7: Metrics
Metrics Requiring a Placed Design

Four metrics require a placed design in order to be accurate. They do not require a fully routed design.

- LUT Utilization per CLB: Color codes slices based on placed LUT utilization.
- FF Utilization per CLB: Color codes slices based on placed FF utilization.
- Vertical Routing Congestion per CLB: Color codes the fabric based on a best case estimate of vertical routing usage.
- Horizontal Routing Congestion per CLB: Color codes the fabric based on a best case estimate of horizontal routing usage.

Metrics in a Netlist Design with No Placement

Two metrics are applicable if there are Pblocks. They do not depend on placement.

- LUT Utilization per Pblock: Color codes the Pblock based on an estimate of how the LUTs will be placed into the slices contained in the Pblock.
- FF Utilization per Pblock: Color codes the Pblock based on an estimate of how the FFs will be packed into the slices contained in the Pblock.

More than one rule can be used at a time as shown in Figure 3-7. Both LUT Utilization per CLB and FF Utilization per CLB are on.

**TIP:** If there are sections of the design with high utilization or high estimates of routing congestion, consider tweaking the RTL or placement constraints to reduce logic and routing utilization in that area.
Routing Analysis

Turn on Routing Resources in the Device window to view the exact routing resources.

*Figure 3-8: Enable Routing*
Displaying Routing and Placement

Routing and placement display in two different ways depending on the zoom level:

- When zoomed out
- At closer zoom levels

**TIP:** The two visualizations of the Device window minimize runtime and memory usage while showing the details of designs of all sizes.

Displaying Routing and Placement when Zoomed Out

When zoomed out, an abstract view is shown. The abstract view:

- Condenses the routes through the device.
- Shows lines of different thicknesses depending on the number of routes through a particular region.

Placement similarly displays a block for each tile with logic placed in it. The more logic in a tile, the larger the block representing that tile will be.
Figure 3-9: Abstract View
Displaying Routing and Placement at Closer Zoom Levels

At closer zoom levels, the actual logic cells and routes show.

Figure 3-10: Detailed View
Viewing Options

The Device window is customizable to show the device, and design, in a variety of ways. Most of these are controlled through the Device Options slideout.

You can enable or disable the graphics for different design and device resources, as well as modify the display colors.

Figure 3-11: Device Window Layers
Navigating in the Device Window

Use the following tools to navigate in the Device window.

- **Zoom Controls**: Standard Zoom In, Zoom Out, and Zoom Full tools.
- **Auto-fit Selection**: Automatically zoom and pan to an object selected in any view outside of the device. Autofit Selection is particularly useful for cross probing.
- **World View**: The World View shows where the currently visible portion of the device is on the overall device. You can move and resize the World View, as well as drag and resize the yellow box to zoom and pan.
- **Control Hotkey**: Press Ctrl while clicking and dragging to pan the view. Use Ctrl and the mouse wheel to zoom in and out at the position of the cursor.

*Figure 3-12: Navigating the Device Window*
Report Design Analysis

The Design Analysis report provides information on timing path characteristics, design interconnect complexity, and congestion. You can use this information to make design or constraint changes that improve QoR and possibly alleviate routing congestion.

Running Report Design Analysis

You can run Report Design Analysis from the Tcl console or the Vivado IDE. Report Design Analysis generates three categories of reports:

- Timing: reports timing and physical characteristics of timing paths
- Complexity: analyzes the design for routing complexity and LUT distribution
- Congestion: analyzes the design for routing congestion

To run Report Design Analysis in the Vivado IDE, select **Tools > Report > Report Design Analysis**.

Equivalent Tcl command: `report_design_analysis -name design_analysis_1`

**Note:** There are some Report Design Analysis options that are only available when running the `report_design_analysis` Tcl command. You can use the `-name` option to view the results of this Tcl command in the GUI.

In the Vivado IDE, the Report Design Analysis dialog box (shown in **Figure 3-13**) includes the following:

- Results Name Field
- Options Tab
- Advanced Tab
- Timer Settings Tab
**Results Name Field**

In the Results Name field at the top of the Report Design Analysis dialog box, specify the name of the graphical window for the report.

Equivalent Tcl option: `-name <windowName>`

**Options Tab**

In the Options tab (shown in Figure 3-13), the following fields are available:

- Timing
- Complexity
- Congestion
Timing Field

The Timing field allows you to report timing and physical characteristics of timing paths.

Equivalent Tcl option: `-timing`

You have the option to generate reports for all paths or specific timing paths. If you select the **All Paths** option you can specify the path delay type: **max** for setup, **min** for hold or **min_max** for setup and hold.

Equivalent Tcl option: `-setup/-hold`

You can also specify the maximum number of paths per clock group (default is 10).

Equivalent Tcl option: `-max_paths <arg>`

When you select the **Specific Paths** option, analysis is performed on the specified path objects. Click the **Browse** button (on the right) to open a search dialog box to aid in finding path objects. For more information about `get_timing_paths`, refer to [this link](#) in the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3].

Equivalent Tcl option: `-of_timing_paths <args>`

Select the **Extend Analysis** option to perform an extended analysis for each path of interest by also reporting the worst path to the startpoint and the worst path from the endpoint.

Equivalent Tcl option: `-extend`

**Note:** When running the Extend Analysis option (Tcl option `-extend`) for hold path analysis, the tool generates a report showing the setup and hold characteristics of the paths with the same start and endpoints to show if hold fixing is impacting setup timing.

**Include logic-level distribution** information by selecting that option and specifying the number of paths to be used. If you are also analyzing **all paths**, the number of paths selected overrides the maximum number of paths per clock group. If you are analyzing specific paths, logic-level distribution information is limited to the specified paths.

Equivalent Tcl option: `-logic_level_distribution
-logic_level_dist_paths <arg>`
Complexity Field

The Complexity field allows you to report the complexity of the design netlist.

Equivalent Tcl option: -complexity

Select the **Cells to Analyze** option to specify the hierarchical cells to use for the complexity analysis. Click the **Browse** button (on the right) to open a search dialog box to aid in finding cell objects.

Equivalent Tcl option: -cells <args>

When you select the **Hierarchical Depths** option, you can select the levels of hierarchy to examine at the top level by default or at the level of the cells specified by the -cells option.

Equivalent Tcl option: -hierarchical_depth <arg>

Congestion Field

The Congestion field toggles the **-congestion** Tcl switch on and off.

Advanced Tab

In the Advanced tab (Figure 3-14), the following fields are available:

- File Output
- Miscellaneous

File Output Field

You can write the results to a file in addition to generating a GUI report by selecting **Write results to file** and specifying a file name in the field to the right. Click the **Browse** button to select a different directory.

Equivalent Tcl option: -file <arg>

Select the **Overwrite** option to overwrite an existing file with the new analysis results.

Select **Append** to append the new results.

Equivalent Tcl option: -append

Miscellaneous Field

The Miscellaneous field provides options to ignore command errors and suspend message limits during command execution.

Equivalent Tcl option: -quiet/-verbose
Timer Settings Tab

In the timer settings tab (shown in Figure 3-15), the following fields and options are available.

- Interconnect Option
- Speed Grade Option
- Multi-Corner Configuration Field
- Disable Flight Delays Option
Interconnect Option

You can select the interconnect model to be used in your analysis of timing paths:

- **actual** provides the most accurate delays for a routed design.
- **estimated** includes an estimate of the interconnect delays based on the placement and connectivity of the design onto the device prior to implementation. Estimated delay can be specified even if the design is fully routed.
- **none** includes no interconnect delay in the timing analysis; only the logic delay is applied.

Equivalent Tcl command: `set_delay_model -interconnect <arg>`

For more information about `set_delay_model`, refer to the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].

Speed Grade Option

You can perform analysis on the default speed grade or select a different speed grade for analysis.

Equivalent Tcl command: `set_speed_grade <arg>`

For more information about `set_speed_grade`, refer to the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].

Multi-Corner Configuration Field

You can limit the default four-corner analysis performed by the Vivado timing analysis engine, as appropriate, using the options available in this field.

Equivalent Tcl command: `config_timing_corners -corner <arg> -delay_type <arg>`

For more information about `config_timing_corners`, refer to the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].

Disable Flight Delays Option

You can select this option to disable the addition of package delays to I/O timing calculations.

Equivalent Tcl command: `config_timing_analysis -disable_flight_delays <arg>`

For more information about `config_timing_analysis`, refer to the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].
Command Line Only Options

The following Timing options are only available from the Tcl command line and can be used with the \texttt{-name} option to generate a GUI report.

- \texttt{-routed\_vs\_estimated}

  This option reports the estimated versus actual routed delays side-by-side for the same path. Some fields within the Timing Category in the report are prefaced with "Estimated" or "Routed" for comparison.

- \texttt{-return\_timing\_paths}
- \texttt{-end\_point\_clock}
- \texttt{-logic\_levels}
The following Complexity options are only available from the command line and can be used with the -name option to generate a GUI report.

- **-bounding_boxes <arg>**

  This option performs the complexity analysis of the specified bounding boxes. For example:

  ```
  -bounding_boxes ( "CLE_M_X21Y239:CLEL_R_X28Y254" "CLEL_R_X18Y171:CLE_M_X26Y186" )
  ```

  **Note:** A space is required between the open bracket `{` and the start of the bounding box, as shown in the previous example.

### Timing Path Characteristics Report

The following figure shows example output after running the Report Design Analysis in Timing Mode to show the path characteristics of only the 10 Worst Setup paths in the design. You can generate the report from the GUI (Tools > Report > Report Design Analysis) or using the Tcl command:

```tcl
report_design_analysis -name <arg>
```

**TIP:** To create hold path characteristics, select **Path delay type: min** in the Options tab of the Report Design Analysis dialog box or add `-hold` to the Tcl command. For more information on Tcl command syntax, see the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3].

![Figure 3-16: Example Setup Path Characteristics](image)

Figure 3-16: Example Setup Path Characteristics

Report Design Analysis can also provide a Logic Level Distribution table for the worst timing paths. The default number of paths analyzed for the Logic Level Distribution table is 1,000 and can be changed in the Report Design Analysis dialog box. The Logic Level Distribution table is not generated by default but can be generated when you select the **Include logic level distribution** in the Report Design Analysis dialog box Options tab. An example of the Logic Level Distribution table is shown in the following figure.
Chapter 3: Implementation Results Analysis Features

Analyzing Specific Paths

Figure 3-18 shows an example report from Report Design Analysis in Timing Mode with specific paths selected.

In this case, the Path Characteristics and the Logic Level Distribution tables (if selected) are limited to the specified path. To specify the paths, click the **Browse** button to the right of the Specific paths selection in the Report Design Analysis dialog box. This opens the Find Timing Paths dialog box (shown in Figure 3-19).
Analyzing the Worst Path along with Preceding and Following Worst Paths

The figure below shows an example report from Report Design Analysis in Timing Mode with the **Extend analysis** option selected.

**Note:** The Extend Analysis for All Paths option is currently only available for setup analysis.

The Path Characteristics are reported on the worst setup path along with the worst setup path to the startpoint cell (PrePath) and the worst setup path from the endpoint cell (PostPath). The -extend option incurs higher runtime as several timing analyses are required to collect the characteristics of all reported paths.

Equivalent Tcl Command: `report_design_analysis -extend`
Reading and Interpreting Timing Path Characteristics Reports

The path characteristics fall into four main categories: timing, logic, physical, and property. You can find the definition of each characteristics in the command long help.

Tcl Command: report_design_analysis -help

Alternatively, you can find the same information in the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3].

Category 1: Timing

- Timing Analysis: The Path Type and Requirement detail the timing analysis type (SETUP or HOLD) along with the timing path requirement. The Slack indicates whether or not the timing path requirement is met based on the timing analysis as dictated by the timing constraints. The Timing Exception indicates if any timing exceptions such as multicycle path or max delay have been applied to the timing path.

Checking the path requirement is often the first step in debugging missing or incorrect timing constraints:

- Paths with setup requirement under 4 ns must be reviewed to verify their validity in the design, especially for clock domain crossing paths.
- Paths with setup requirement under 2 ns are difficult to meet and must be avoided in general, especially for the older architectures.
- In general, when small setup requirements are present, check for missing timing exception constraints and also check the source and destination clock edges. The timing analysis always assumes the smallest positive difference between source and destination clock edges unless overridden by a timing exception constraint.
- Positive hold path requirements need to be reviewed as they are not common and are difficult to meet. When positive hold path requirements are present, check for missing multicycle path constraints for hold analysis that might have only been applied to the path for setup analysis. Also check the relationship between source and destination clocks for correctness.
Chapter 3: Implementation Results Analysis Features

- **Datapath:** The Path Delay, Logic Delay, and Net Delay detail the total datapath delay along with its breakdown into delay contribution by logic cells and nets.
  - If the Logic Delay makes up an unusually high proportion of the total datapath delay, for example 50% or higher, it is advised to examine the datapath logic depth and types of cells on the logic path, and possibly modify the RTL or synthesis options to reduce the path depth or use cells with faster delays.
  - If the Net Delay dominates the total path delay for a setup path where the Requirement is reasonable, it is advised to analyze some of the physical characteristics and property characteristics of the path listed in this section. Specific items to look at include the High Fanout and Cumulative Fanout characteristics to understand if some nets of the path have a high fanout that could potentially be causing a placement problem. Also check the Hold Fix Detour characteristic to understand if hold fixing has occurred on the path (this characteristic is only updated when report_design_analysis is run in the same session as route_design, and not after loading a post-route checkpoint).

**IMPORTANT:** The LUT input pins have different delay characteristics. The physical pins (or site pins) of higher index are faster than the pins of lower index. Be aware of the difference in 7 series and UltraScale™ device LUT delay reporting. In 7 Series devices, the variable portion of LUT delay is reported as part of the net delay in front of the LUT. In UltraScale devices, the variable portion of LUT delay is reported as logic delay. Therefore, the 7 Series device Net Delay/Logic Delay ratio will be larger than the ratio for UltraScale devices.

- **Clocks:** The Start Point Clock, End Point Clock, Clock Relationship, and Clock Skew detail information regarding the timing path clocks. The Start Point Clock and Endpoint Clock list the respective source clock and destination clock for the timing path.
  - Check that the Clock Relationship is correct and expected. For intra-clock paths or synchronous clock domain crossing paths, the relationship is labeled as "Safely Timed." You must verify that the Requirement and Clock Skew are reasonable. For asynchronous clocks, the relationship is labeled as "No Common Primary Clock" or "No Common Period." Asynchronous clock domain crossing paths must be covered by timing exceptions (check the Timing Exception value).
  - Check that the Clock Skew is reasonable. When analyzing clock skew, check the clock tree structure for cascaded clock buffers. In 7 Series devices, check for different clock buffer types for the source and destination clocks. In UltraScale devices, it might be necessary to examine the placement and routing of the clock nets because it depends on logic loads placement. The crossing of a Clock Region boundary or an I/O Column can result in higher clock skew; this is expected.

Note that almost all of the Timing Characteristics provided by report_design_analysis are available in a timing report.
Chapter 3: Implementation Results Analysis Features

Category 2: Logic

- **Path:** The Start Point Pin Primitive, End Point Pin Primitive, Start Point Pin, End Point Pin, Logic Levels, Logical Path, and Comb DSP logic characteristics provide some basic information about the timing path.
  - The Start Point Pin Primitive and End Point Pin Primitive are the reference pin names of the timing path start point and end point. Check that the Start Point Pin Primitive and End Point Pin Primitive are expected timing path start and endpoints. The Start Point Pin and End Point Pin identify the actual timing path pin startpoints and endpoints that would show in the header of a typical timing report.
    - Check for endpoint pins such as CLR, PRE, RST, and CE that could potentially be part of high-fanout nets for control signals such as asynchronous resets and clock enable signals. Also check the type of cell, because some primitives like block RAMs and DSPs have larger Clock-to-Q delay and setup/hold requirements than other cells. Their presence in the path can potentially consume a significant portion of the path timing budget.
  - The Logic Levels and Logical Path detail the number of logic levels and the types of primitives in the datapath. You can use this information to quickly check if a high number of logic levels is mostly due to LUTs or to a mix of LUT/CARRY/MUXF cells. CARRY and MUXF cells are usually connected to nets with dedicated routes that have null or very small delays, while LUT inputs always need to be routed through the fabric.
    - When the path mostly contains LUTs, it is also important to check their size. Try to understand why there are several smaller LUTs (non-LUT6) that are chained and what prevents synthesis from targeting LUT6 only, which can reduce the logic levels. There can be properties like KEEP/DONT_TOUCH/MARK_DEBUG or mid-to-high fanout nets in the path that also impact mapping efficiency.
  - Based on the outcome of your analysis, you can either modify the RTL source, add/modify attributes in the RTL, or use different synthesis settings to reduce the number of LUTs on the path. Also, you can use the option -remap of the opt_design command to re-optimize LUT mapping and possibly eliminate some smaller LUTs.
  - The COMB DSP details the number of DSPs used as combinatorial logic that are part of the datapath.

- **Cells:** DOA_REG, DOB_REG, MREG, PREG correspond to Block RAMs and DSPs optional register properties. Timing is more difficult to meet on paths from RAMBs or DSPs with no output registers and with several logic levels. You should consider modifying your design to use the RAMB or DSP output registers if these paths are having difficulty meeting the timing requirements.
Chapter 3: Implementation Results Analysis Features

Category 3: Physical

- Architectural Boundary Crossings: The BRAM Crossings, DSP Crossings, IO Crossings, Config Crossings, and SLR Crossings identify whether the path is crossing architectural resources such as BRAM columns, DSP columns, IO Columns, CONFIG Block Columns, or SLR boundaries.

  The crossing of many architectural columns does not always represent a problem. Check for high net delay or large skew in conjunction with the crossing of many architectural columns. If many architectural column crossings appear to be the cause of timing issues across multiple implementation runs for a particular module, consider minimal floorplanning using Pblocks to reduce the crossings of the architectural column(s) or SLR boundary.

- Path Placement Restrictions: Pblocks. Excessive floorplanning can sometimes prevent the tool from achieving the optimal results. Paths that cross multiple Pblocks can sometimes experience timing issues.
  - If the path crosses multiple Pblocks, examine the location of the Pblocks and the impact on the timing path placement.
  - If the Pblocks are adjacent, consider creating a single Pblock that is a super-set of each individual Pblock. This could potentially improve timing by being less restrictive on the placer.

  If physical requirements dictate that the Pblocks are placed far apart, consider pipelining between the Pblocks to help meet timing requirements.

- Placement Box: Bounding Box Size, Clock Region Distance, Combined LUT Pairs
  - If the Bounding Box Size or Clock Region Distance of the timing path is too large, try using directives in place_design. In UltraScale devices, be especially aware of the Clock Region Distance and its possible impact on timing path Clock Skew.

- Net Fanout and Detour:
  - High Fanout shows the highest fanout of all nets in the datapath, and Cumulative Fanout corresponds to the sum of all datapath net fanouts.

    If High Fanout and Cumulative Fanout are large, the timing violations are very likely due to the fanout impact on routing and net delay.

    If physical optimization was run and did not reduce the fanout, check for MARK_DEBUG and DONT_TOUCH constraints preventing replication.

    If replication is desired on the net prior to implementation, you can use the MAX_FANOUT constraint in synthesis, either inside the RTL or in an XDC file. Due to reliance on placement for good timing for high fanout nets, it is usually not recommended to have synthesis perform replication and it is best to rely on post-placement physical optimization (phys_opt_design) for replication. You can
also increase the physical optimization effort to also optimize paths with a small positive slack by using different directives such as Explore, AggressiveExplore, or AggressiveFanoutOpt.

If fanout reduction is desired on a specific net during implementation, you can force the replication using the command:
phy_opt_design -force_replication_on_nets <netName>

- When the Hold Fix Detour is asserted, the routing on the datapath was delayed in order to meet the path hold time requirement. If the path is failing setup, check for excessive skew between the Source and Destination clocks. Also check for proper timing constraints between the Source and Destination clocks in case the hold path requirement is positive (it should be zero or negative in most common cases).

Category 4: Property

- LUT Combining: Combined LUT Pairs indicates that there are combined LUT pairs present in the path. While combining LUT pairs can reduce logic utilization, it can also restrict the placement solutions and can create congestion due to high pin density. If LUT combining appears to be an issue in the design, it is recommended to disable LUT combining in synthesis by using the -no_lc option.

- Optimization Blocking: Mark Debug and Dont Touch can quickly identify whether there are any nets or cells in the path that the tool is not allowed optimize.
  - The default behavior of setting the MARK_DEBUG property is to also set the DONT_TOUCH property. Consider setting DONT_TOUCH to FALSE to allow for optimization.
  - DONT_TOUCH disables optimizations such as cell or net replication. Evaluate the need for DONT_TOUCH constraints and remove them if possible. When a net enters a hierarchical cell with DONT_TOUCH, the portion of the net inside the hierarchical cell cannot be replicated. If DONT_TOUCH is used to prevent logic trimming, check the design for correctness. One simple example would be logic removed due to unconnected outputs.

- Fixed Placement and Routing: The Fixed Loc, Fixed Route can quickly identify whether there are any fixed placement or fixed routing constraints that might be impacting the timing path slack.
  - Using cell location constraints can help stabilizing QoR for a difficult design. If timing can no longer be met after modifying the design, you can try removing the placement constraints to give more flexibility to the placer.
  - Having fixed routes prevents the router from optimizing the net delays to meet timing. A timing path with locked routing usually shares nets with other paths that can be negatively impacted by this constraint. Use fixed routes only when necessary and when it does not affect interacting paths. Always be aware that changes to other physical constraints such as Pblocks might require the fixed cell locations or fixed routes to also be updated.
Category 5: Partial Reconfiguration

For Partial Reconfiguration (PR) designs, the logical path is appended to identify the cell as belonging to a reconfigurable partition (:RP#), or to the static region of the design (:S). A translation table at the bottom of the report maps :RP# to a specific reconfigurable partition.

- **PR Path Type**: Specifies the path as being completely in the static region, completely in a reconfigurable partition (RP), or as crossing the boundary between regions. The delay elements for the timing path are also broken down between the regions.
- **Static Crossings**: Reports the number of times a RP path crosses into the static region.
- **RP Crossings**: Reports the number of times a static region path crosses into a RP region.
- **Boundary Fanout**: Reports the fanout of a boundary path at the PPLOC to its downstream loads.

Complexity Report

The complexity report shows the Rent Exponent, Average Fanout, and distribution of the types of leaf cells of the top-level design and/or of hierarchical cells that contain more than 1000 leaf cells. The Rent exponent is the relationship between the number of ports and the number of cells of a netlist partition when recursively partitioning the design with a min-cut algorithm. It is computed with similar algorithms as the ones used by the placer during global placement. Therefore it can provide a good indication of the challenges seen by the placer, especially when the hierarchy of the design matches well the physical partitions found during global placement.

The Rent Exponent is defined by the Rent's rule:

\[
\text{ports} = \text{constant} \times \text{cells}^{\text{Rent}}
\]

\[
\log(\text{ports}) = \text{Rent} \times \log(\text{cells}) + \text{constant}
\]

A design with higher Rent exponent corresponds to a design where the groups of highly connected logic also have strong connectivity with other groups. This usually translates into a higher utilization of global routing resources and an increased routing complexity. The Rent exponent provided in this report is computed on the unplaced and unrouted netlist.

After placement, the Rent exponent of the same design can differ as it is based on physical partitions instead of logical partitions. The post-placement Rent exponent is not reported by the Report Design Analysis command as it is recommended to analyze the congestion reports once the design is placed instead.

Report Design Analysis runs in Complexity Mode when you do either of the following:

- Check the **Complexity** option in the Report Design Analysis dialog box Options tab.
- Execute the `report_design_analysis` TCL command and use any of the options shown in the following table.
Chapter 3: Implementation Results Analysis Features

Table 3-1: Options that Run Report Design Analysis in Complexity Mode

<table>
<thead>
<tr>
<th>Tcl Option</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>-complexity</td>
<td>Must be specified to run the report design analysis in Complexity Mode.</td>
</tr>
<tr>
<td>-cells &lt;arg&gt;</td>
<td>Specifies the hierarchical cells to use when analyzing the complexity.</td>
</tr>
<tr>
<td>-hierarchical_depth &lt;arg&gt;</td>
<td>The levels of hierarchy to examine at the top level by default or at the level of the cells specified by the -cells option.</td>
</tr>
</tbody>
</table>

Analyzing the Design Complexity at the Top Level

The following figure shows an example report from Report Design Analysis in Complexity Mode that reports up to one level of hierarchy from the top module.

Tcl Command:

```
report_design_analysis -complexity -hierarchical_depth 1
```

![Complexity Analysis at the Top Level and Hierarchical Depth of 1](image)

Reading and Interpreting a Complexity Report

The Complexity Characteristics table from the previous example shows the Rent exponent and average fanout for each level of hierarchy below the top level. The typical ranges to consider when reviewing these metrics are the following:

- Rent exponent:
  - Between 0.0 and 0.65: The complexity is considered low to normal and does not highlight any potential problems.
  - Between 0.65 and 0.85: The complexity is considered high, especially when the total number of instances is above 25k.
  - Above 0.85: The complexity is very high, and if the number of instances is also high, the design can potentially fail during implementation.

- Average fanout:
  - Below 4: It is considered normal.
- Between 4 and 5: The implementation tools can show difficulty to place the design without congestion. In the case of a SSI device, if the total number of instances is above 100k, the placer can have problems finding a placement solution that fits in 1 SLR or that is spread over 2 SLRs.

- Above 5: The design can potentially fail during implementation.

You must treat high Rent exponents and/or high average fanouts for larger modules with higher importance. Smaller modules, especially under 10k total instances, can have higher Rent exponent and average fanout, and yet be simple to place and route successfully. For this reason, the Total Instances column must always be reviewed along with the Rent exponent and average fanout.

The complexity characteristics might not always predict routing congestion. Other factors such as I/O location constraints, floorplanning, and macro primitive location in the target device can limit the placement solution space and introduce congestion. The effect of such constraints is better analyzed by the congestion reports available after placement.

Other items to consider when interpreting the Complexity Characteristics table:

- A higher percentage of LUT6s in a module usually increases the average fanout and potentially the Rent exponent.

- A high number of RAMB and DSPs can increase the Rent exponent because these primitives have a large amount of connectivity.

- The hierarchical instances with higher Rent exponents or higher average fanouts are not always a problem because the placer operates on a flat netlist and can break these instances into easier groups of logic to place. This report provides an indication of where a netlist problem can possibly exist if a module stands out clearly.

When a large module exhibits a high Rent exponent and/or average fanout that is causing congestion and timing issues, consider the following actions:

- Reduce the connectivity of the module. Preserving the hierarchy to prevent cross-boundary optimization in synthesis can reduce the use of LUT6s and consequently reduce the netlist density.

- Try to disable LUT combining in synthesis.

- Use a Congestion Strategy during Implementation or SpreadLogic placement directive that can potentially help to relieve congestion. If the design is targeting an SSI Device, consider trying several SSI placement directives.

- Use simple floorplanning at the SLR level for SSI devices, or at the clock region level in general, to keep congested groups of logic separate, or to guide global placement towards a solution similar to a previously found good placement.
Chapter 3: Implementation Results Analysis Features

Congestion Report

The Congestion reports show the congested areas of the device and the name of design modules present in these areas. Congestion can potentially lead to timing closure issues if the critical paths are placed inside or next to a congested area.

Analyzing the Design Congestion

To run Report Design Analysis in Congestion Mode, the Congestion option must be specified in the Options tab of the Report Design Analysis dialog box, and the design must be placed and/or routed. Running Report Design Analysis with Congestion Mode on an unplaced design results in nothing being reported.

Report Design Analysis produces six congestion tables:

- Placed Maximum Level Congestion Reporting
- Initial Estimated Router Congestion Reporting
- Router Maximum Level Congestion Reporting
- SLR Net Crossing Reporting
- Placed Tile Based Congestion Metric (Vertical)
- Placed Tile Based Congestion Metric (Horizontal)

Maximum Congestion Reports

These tables report all the windows with the same maximum congestion level seen in a particular direction. The columns are defined as follows:

- Direction: The direction of the congested routing resources (North, South, West, or East).
- Congestion Level: The maximum congestion level in CLB tiles.
- Congestion: Indicates the estimated routing resource utilization in the defined window. This value can be greater than 100%.
- Congestion Window: Indicates the bounding CLB tiles where the congestion for the identified Direction is present. The CLB coordinates correspond to the lower left and upper right corners of the window.

TIP: The Congestion Window column is only available in the text report. In the GUI report, you can select the congestion window, which highlights the congested area in the Device window.

- Cell Names: Indicates the parent instance that contains the hierarchical cells involved in the Congestion Window, up to the three largest contributors along with their contribution percentage.
**TIP:** In the GUI report, you can select the hyperlinked cell names to highlight the respective leaf cells in the congestion window.

- **COMBINED LUTs %:** Indicates the percentage of LUTs combined in the window.
- **LUT6 usage %:** The percentage of LUT6 utilization in the Window.
- **LUT5 usage %:** The percentage of LUT5 utilization in the Window.
- **Flop usage %:** The percentage of FD (including LD) utilization in the Window.
- **MUX usage %:** The percentage of MUXF utilization in the Window.
- **RAMB usage %:** The percentage of RAMB utilization in the Window.
- **URAM usage %:** The percentage of URAM utilization in the Window.
- **DSP usage %:** The percentage of DSP utilization in the Window.

### Placed Maximum Level Congestion Reporting

When analyzing the Placed Maximum Level Congestion Reporting Table of your design for Congestion and Timing QoR, look for the following:

- If a high level of LUT usage exists, examine the instances that have a high percentage of LUT6s in the Complexity report.
- In case of high RAMB or DSP utilization in the congested area, check for Pblock constraints that might be limiting the available placement area of the reported modules. Use various targeted placement directives to relieve congestion such as the BlockPlacement or SpreadLogic directives. In some cases, it might be beneficial to reuse the RAMB or DSP placement from a previous run that showed low congestion and resulted in good Timing QoR.

Figure 3-22 shows an example of the Placed Maximum Level Congestion Reporting table. Using this report, you can examine areas of the device defined by the Congestion window along with the modules residing in that window. The resource usage percentages gives an indication of the types of resources located in the congested area.
Initial Estimated Router Congestion Reporting

Initial Estimated Router Congestion is only available when the router has been run and is similar to the Congestion Report in the route_design log file. It shows the routing congestion initially faced by the router during the early stages of routing.

![Initial Estimated Router Congestion Reporting Table]

Figure 3-23: Example of Initial Estimated Router Congestion Reporting Table

When the congestion level is 4 or higher, the router prints an initial estimated congestion table that provides details about the nature of congestion.

- Global congestion is estimated similar to placer congestion and is based on all types of interconnects.
- Long congestion only considers long interconnect utilization for a given direction.
- Short congestion considers all other interconnect utilization for a given direction.

Any congestion area greater than 32x32 (level 5) is likely to impact QoR and routability. Congestion on long interconnects increases usage of short interconnects and results in longer routed delays. Congestion on short interconnects usually induces longer runtimes and if their tile % is more than 5%, it is also likely to cause QoR degradation.

When analyzing the Initial Estimated Router Congestion table, look for the following:

- If the congestion level is greater than 6, the design is unlikely to meet timing and might fail during routing.
- If the congestion level is 4 or 5, then identify the module(s) located in the congested area(s). You can apply a congestion alleviation technique on these modules or rerun the placer with different directives, such as *SpreadLogic*.
- If the congestion level is 3 or less, the congestion is probably not a cause for concern unless the design has a very tight timing budget.
Router Maximum Level Congestion Reporting

The Router Maximum Level Congestion Reporting is only available when the router has been run and is similar to the Congestion Report in the route_design log file.

The congestion level reported here is usually lower than the congestion level reported at the start of routing in the Initial Estimated Router Congestion. This is because the congestion has already been resolved by the router.

SLR Net Crossing Reporting

The SLR Net Crossing Reporting is only applicable to SSI Devices and reports the number of nets contained in a module that cross the SLR boundaries. For each module, the table provides further details of which SLRs are crossed by the nets. The following figure shows an example of the SLR Net Crossing Reporting table.

Note: When a net has loads in multiple SLRs, it is only counted once for the furthest cut. For example, a net driven from SLR0 to loads in SLR1, SLR2, and SLR3 is only counted once under the 0-3 cuts, with SLR3 being the "furthest fanout" from SLR0. This counting method enables to sum the number of nets under each column (0-1 Cuts, 1-2 Cuts, and so on) to match to total number of nets crossing, as each net is only counted once.
When analyzing the SLR Net Crossing Reporting Table of your design for Congestion and Timing QoR, look for the following:

- When using SSI Devices, the SSI placement directives can be beneficial for both timing and congestion.
- If a particular module that is crossing SLRs is consistently experiencing timing issues across multiple implementation runs using various placement directives, attempt light Pblocking to constrain the module to a single SLR.

**Placed Tile Based Congestion Metrics**

The Placed Tile Based Congestion Metric reports the 10 CLB tiles with highest congestion, along with the modules that have cells located in the CLB tile. Figure 3-26 and Figure 3-27 show examples of the Placed Tile Based Congestion Metric for both Vertical and Horizontal routing.

- Tile Name: The CLB tile where the congestion is occurring.
- RPM Grid Column/Row: The RPM location of the CLB tile in the device.
- Congestion in Window (%): Indicates the percentage of estimated routing resource utilization through the CLB tile. This value can be greater than 100%.
- Cell Names: Indicates the parent instance that contains the cells involved in the Congestion Window for up to three largest contributors along with their contribution percentage.
- Placer Max Overlap: indicates whether or not the particular tile overlaps with a Placer Maximum region.

You can view this data graphically by selecting **Window > Metrics** and showing Vertical/Horizontal routing congestion per CLB beneath CLB Metrics.
Chapter 3: Implementation Results Analysis Features

Placed Tile Based Congestion Metric (Vertical)

Figure 3-26: Placed Tile Based Congestion Metric (Vertical)

Placed Tile Based Congestion Metric (Horizontal)

Figure 3-27: Placed Tile Based Congestion Metric (Horizontal)
Report QoR Suggestions

The QoR Suggestions report provides a list of recommendations to improve timing closure, based on design changes or by setting additional constraints and tool options for the synthesis and implementation steps. The report must be run on a design loaded in memory after synthesis or after any implementation step. The analysis uses a combination of netlist characteristics, timing violations, and congestion information. The recommendations can vary as the timing critical paths usually change after each implementation step and the congestion information becomes more accurate after placement and routing.

The QoR Suggestions report is an extension of the Design Analysis report and shares the same concepts and terminology. See the Report Design Analysis for the terminology definitions.

Running Report QoR Suggestions

You can only run Report QoR Suggestions from the Tcl Console using the `report_qor_suggestions` Tcl command. By default, Report QoR Suggestions generates the QoR Suggestions Report Summary table, that is organized around three main categories; Congestion, Generic, and Timing as shown in the example in Figure 3-28.
Each category is composed of one or more suggestion types. The detailed tables for each suggestion provide additional information related to the nature of the QoR challenge, the resolution step, and the characteristics of the most critical path covered by the suggestion.

By default, the QoR Suggestions report limits the analysis to the worst 100 violating timing paths. To decrease or increase the scope of the analysis, the `-max_paths` option can be used. When using the `-output_dir` option, the report generates up to 3 XDC or Tcl files that contain constraints which correspond to the suggestions reported in the Detailed Report tables:

- **RQSPreSynth.xdc**: This file contains constraints for tuning Vivado Synthesis optimization of specific hierarchies or logic operators.
- **RQSPreImpl.tcl**: This file contains optimization constraints that force specific logic optimizations during `opt_design`.
- **RQSImplCommon.tcl**: This file contains optimization constraints that are not provided in `RQSPreSynth.xdc` and `RQSPreImpl.tcl`.

The constraints and tool optimizations suggested in the `RQSPreSynth.xdc`, `RQSPreImpl.tcl`, and `RQSImplCommon.tcl` files do not affect the functionality of the design. If some critical paths start or end with DSP or BRAM primitives, where some of the optional pipeline registers are not enabled, you can use the `-evaluate_pipelining` option to generate additional constraints that will enable the pipeline registers. These constraints must only be used to evaluate the QoR impact and must not be kept in the final design constraints as they affect the original design functionality. Instead you must modify the design source files, typically the RTL files, accordingly to implement the suggestion appropriately.

**Using the Constraints Generated by Report QoR Suggestions**

The generated constraints must be added to the compilation flow manually to quickly benefit from the suggestions.

In project mode, when starting from the Synthesis step:

- Add `RQSImplCommon.tcl` to the Opt Design `Tcl.pre` hook.

In project mode, when starting from the Implementation step:

- Add both `RQSPreImpl.tcl` and `RQSImplCommon.tcl` to the Opt Design `Tcl.pre` hook.
Chapter 3: Implementation Results Analysis Features

In non-project mode, when starting from the Synthesis step:

- Read the RQSPreSynth.xdc file before running the synth_design command.
- Source the RQSImplCommon.tcl file before running the opt_design command. For example:

  ```
  read_verilog dsgTop.v
  read_xdc timing.xdc
  read_xdc RQSPreSynth.xdc
  synth_design -top dsgTop -part xcvu9p-flgb2104-2-i
  source RQSImplCommon.tcl
  opt_design
  ```

In non-project mode, when starting from the Implementation step:

- Source both the RQSPreImpl.tcl and RQSImplCommon.tcl files before running opt_design. For example:

  ```
  open_checkpoint dsgTop_synth.dcp
  source RQSPreImpl.tcl
  source RQSImplCommon.tcl
  opt_design
  ```

**Reviewing the QoR Suggestions Details**

The QoR Suggestions report provides recommendations in separate detailed tables. Each table corresponds to a category of suggestions with sub-categories, additional details on the nature of the QoR issues, and suggested next steps. Additional columns show more information about the congested logic, high fanout nets, or violating timing path characteristics when applicable. Most suggestions cover several timing paths at once, which is reported in the No. of Paths columns. The other timing path characteristics columns only show information related to the worst violating path covered by a suggestion.

- Congestion due to macro primitives/high fanout nets
  - Congestion due to LUT combining
  - Congestion due to high MUXF usage
  - Congestion due to high LUTRAM usage
  - Congestion due to high SRL usage
  - Congestion due to high CARRY usage
  - Congestion due to high fanout reset nets
Chapter 3: Implementation Results Analysis Features

- Control Sets
  - Large number of control sets
    
    **Note:** The recommended number of unique control sets correspond to the guideline documented in this section in the *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949) [Ref 6].

- BRAM or DSP Pipelines
  - BRAM pipelining
  - DSP pipelining

- Clock Gated BRAMs
  - Disable BRAM power optimization

- Critical Cascaded BRAMs
  - Reduce Cascaded BRAMs Height

- Critical Control Signals Remap
  - Move control logic to the datapath

- Critical Nets Replication
  - Loads placed far apart

- Critical SRLs
  - Mapping SRL into registers
  - Unrolling the last flop in SRL

- High Clock Skew
  - Rebalancing Source and Destination Clock Paths

- Tight Path Requirements
  - Tight constraints with timing exceptions
Chapter 4

Viewing Reports and Messages

Introduction to Reports and Messages

The Xilinx® Vivado® Integrated Design Environment (IDE) generates reports and messages to inform you of the state of the design or design processes during various tool interactions. Reports are generated by you (or by the tool) at key steps in the design flow. The reports summarize specific information about the design.

The tool generates messages automatically at each step of the design process, and for many user actions.

Messages and reports are stored in the Messages and Reports windows in the Results window area.

When you run any of the following commands, the tool starts a new process:

• Run Synthesis
• Run Implementation
• `launch_runs (Tcl)`

For more information on Tcl commands, see the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3], or type `<command> --help`.

The process generates messages and reports that persist on disk until you reset the run. Messages that relate to a run appear when a project is open. The tool displays only the messages for the active run in the Messages window.

Reports result from a variety of actions in the Vivado IDE:

• When you load a design, many different reporting commands are available through the Tools menu.
• Running Synthesis or Implementation creates reports as part of the run.
Chapter 4: Viewing Reports and Messages

Viewing and Managing Messages in the IDE

Messages provide brief status notes about specific elements of the design, or about errors that occurred in tool processes.

**TIP:** Review the messages to determine whether the Vivado tools are having difficulty, or are encountering errors in any sections of the design.

Using the Reports Window

The reports for the active Synthesis and Implementation runs appear in the Reports window. Double click a report to view it in the text viewer. Select the Reports tab of the Run Properties window to view reports of the run selected in the Design Runs window.

![Reports Window](image)

**Figure 4-1:** Reports Window

Using the Messages Window

There are two types of messages:

- Messages stored on disk
- Messages stored in memory
The Vivado Integrated Design Environment (IDE) groups messages in the Messages window by the action that created the message. Use the command buttons on the toolbar menu to group the messages by message ID or file.

![Messages Window](image)

Figure 4-2: Messages Window

Some messages include hyperlinks to a file or a design element to help in debugging. Click the link to view the source.

TIP: Use the popup menu to copy messages to paste into another window or document.

Each message is labeled with a message ID and a message severity.

- **Message ID**: The message ID identifies different messages, allowing them to be grouped and sorted.
- **Message Severity**: The message severity describes the nature of the information presented.

Some messages require your attention and resolution before the design can be elaborated, synthesized, or implemented. Some messages are informational only. Informational messages provide details about the design or process, but require no user action.

<table>
<thead>
<tr>
<th>Icon</th>
<th>Severity</th>
<th>Message</th>
</tr>
</thead>
<tbody>
<tr>
<td><img src="image" alt="Status" /></td>
<td>Status</td>
<td>Communicates general status of the design processing.</td>
</tr>
<tr>
<td><img src="image" alt="Info" /></td>
<td>Info</td>
<td>General status of the process and feedback regarding design processing.</td>
</tr>
<tr>
<td><img src="image" alt="Warning" /></td>
<td>Warning</td>
<td>Design results may be sub-optimal because constraints or specifications may not be applied as intended.</td>
</tr>
<tr>
<td><img src="image" alt="Critical Warning" /></td>
<td>Critical Warning</td>
<td>Certain user input or constraints will not be applied, or are outside the best practices, which usually leads to an error later on in the flow. Examine their sources and constraints. Changes are highly recommended.</td>
</tr>
<tr>
<td><img src="image" alt="Error" /></td>
<td>Error</td>
<td>An issue that renders design results unusable and cannot be resolved without user intervention. The design flow stops.</td>
</tr>
</tbody>
</table>
**RECOMMENDED:** Carefully review all errors and critical warnings issued by the tools when loading a design in memory, or from your active synthesis and implementation run. The messages provide information about problems that require your attention. Many messages include a longer description along with resolution advice that can be displayed by clicking on the message ID.

For an example, see Figure 4-3. In this example, a primary clock constraint refers to a port that cannot be found in the design (first warning), so the clock is not created (first critical warning) and any other constraints that refer to this clock fail as well.

![Figure 4-3: Reviewing Errors and Critical Warning](image)

**Filtering Messages**

You can filter messages by severity.

To enable or disable the display of a specific message type:

1. Go to the Messages window.
2. Select (to enable) or deselect (to disable) the check box next to a message severity in the window header.

You can change the severity of a specific message ID. For example, you can decrease the severity of a message you do not believe is critical, or increase the severity of a message you think demands more attention.

To increase or decrease the severity of a message, use the `set_msg_config` Tcl command. For example:

```
set_msg_config -id "[Common 17-81]" -new_severity "CRITICAL WARNING"
```

For more information on the `set_msg_config` Tcl command, see [this link](#) in the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].
Vivado Generated Reports and Messages

This section discusses Vivado Generated Reports and Messages and includes:

- Synthesis Report and Messages
- Implementation Log
- WebTalk Report

Synthesis Report and Messages

The Vivado Synthesis Report is the primary output from the Vivado Synthesis tool including:

- The files processed, which are:
  - VHDL
  - Verilog
  - System Verilog
  - XDC
- Parameter settings per cell
- Nets with Multiple Drivers
- Undriven hierarchical pins
- Optimization information
- Black boxes
- Final Primitive count
- Cell usage by Hierarchy
- Runtime and memory usage

**IMPORTANT:** Review this report or the messages tab for Errors, Critical Warnings and Warnings. The Synthesis tool can issue Critical Warnings and Warnings that become more serious later in the flow.
Implementation Log

The Vivado Implementation Log includes:

- Information about the location, netlist, and constraints used.
- Logic optimization task. The tool runs logic optimization routines by default to generate a smaller and faster netlist.
- The placement phases, plus a post-placement timing estimate (WNS and TNS only).
- The router phases, plus several timing estimates and an estimated post-routing timing summary (WNS, TNS, WHS and THS only).
- Elapsed time and memory for each implementation command and phases.

Review this report or the proper section of the messages tab for Errors, Critical Warnings and Warnings. The Placer generates warnings that may be elevated to Errors later in the flow. If using Stepwise runs, the log contains only the results for the last step.

**IMPORTANT:** Review the Timing Summary Report to view: (1) the Pulse Width timing summary, and (2) additional information about timing violations or missing constraints.

WebTalk Report

The WebTalk Report is generated during Bitstream. This report helps Xilinx understand how its customers use Xilinx FPGA devices, software, and Intellectual Property (IP). The information collected and transmitted by WebTalk helps Xilinx improve features most important to customers. No proprietary information is collected. For more information, see [https://www.xilinx.com/webtalk/](https://www.xilinx.com/webtalk/).

Creating Design Related Reports

This section discusses Creating Design Related Reports and includes:

- Report Utilization
- Report I/O
- Report Clock Utilization
- Report Control Sets
- Report DRC
- Report Route Status
- Report Noise
- Report Power
Chapter 4: Viewing Reports and Messages

Report Utilization

You can generate the Utilization Report during various steps in the flow with the `report_utilization` Tcl command. (For details on Tcl command usage see the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].) The report details shown below are for a 7 series design. It includes the device used for the run and utilization for the following (additional items might appear in each category):

- **Slice Logic**
  - LUT
  - MuxFx
  - Register
- **Memory**
  - BlockRam
  - FIFO
- **DSPs**
- **I/O Resources**
- **Clocking Resources**
  - BUFGCTRL
  - BUFR
  - BUFHCE
  - MMCME2_ADV
  - PLL2_ADV
- **Specific Device Resources:**
  - STARTUPE2
  - XADC
- **Primitive type count sorted by usage**
- **Black Boxes**
- **Instantiated Netlists**

When run from the Tcl Console, the report can include usage of a particular hierarchical cell when using the `-cells` option. When run from the Vivado IDE graphical user interface, this information appears in an interactive table.

The numbers may change at various points in the flow, when logic optimization commands change the netlist.
Chapter 4: Viewing Reports and Messages

Report I/O

The I/O Report replaces the Xilinx® ISE® Design Suite PAD file. The I/O Report lists:

- Pin Number: All the pins in the device
- Signal Name: The name of the user I/O assigned to the pin
- Bank Type: The bank type where the I/O is located (High Range, High Performance, Dedicated, etc.)
- Pin Name: Name of the pin
- Use: The I/O usage type (Input, Output, Power/Ground, Unconnected, etc.)
- I/O Standard: The I/O standard for the User I/O

An asterisk (*) indicates that it is the default. This differs from the I/O Ports window of the Vivado IDE.

- I/O Bank Number: The I/O Bank where the pin is located
- Drive (mA): The drive strength in milliamps
- Slew Rate: The Slew Rate configuration of the buffer: Fast or Slow
- Termination: The on/off chip termination settings
- Voltage: The values for various pins, including VCCO, VCCAUX, and related pins
- Constraint: Displays Fixed if the pin has been constrained by the user
- Signal Integrity: The Signal Integrity of the pin

Report Clock Utilization

The Clock Utilization Report helps you analyze the utilization of clocking primitives and routing resources inside the device at the clock region level or at the clock net level. It can be useful for debugging clock placement issues and identify placement constraints to maximize the resource utilization. The Clock Utilization Report provides information on:

- The number of clocking primitives available and utilized, and their physical constraints
- The timing clock name and period associated with each clock net
- Each clock region clocking and fabric loads utilization
- Each clock net loads in each clock region

In addition, the Clock Utilization Report in the Vivado IDE supports netlist and device objects selection for highlighting placement information and creating schematics.
Running Report Clock Utilization

To generate the Clock Utilization Report in the Vivado IDE, select **Tools > Report > Report Clock Utilization**.

Equivalent Tcl command:

```
report_clock_utilization -name clock_utilization_1
```

Results Name Field

In the Results Name field at the top of the Report Clock Utilization dialog box, specify the name of the graphical window for the report.

Equivalent Tcl option:

```
-name <windowName>
```

Show Clock Roots Only

When selecting this option, the Global Clock Resources table only shows the clock root location for each clock net instead of the complete source, load, and timing clock details.

Equivalent Tcl option:

```
-clock_roots_only
```

Write Clock Constraints to File

Select this option and specify the name of a new constraints file to export the clock source and load physical constraints that correspond to the placement information of the design in memory.
Chapter 4: Viewing Reports and Messages

Equivalent Tcl option:

    -write_xdc <filename>

**Export to File**

You can write the results to a file in addition to generating a GUI report by selecting **Export to file** and specifying a file name in the field on the right. Click the **Browse** button to select a different directory.

Equivalent Tcl option:

    -file <arg>

Select the **Overwrite** option to overwrite an existing file with the new analysis results. Select **Append** to append the new results.

Equivalent Tcl option:

    -append

**Report Clock Utilization Tables**

The report presents the clocking topology and placement information organized by categories:

- Clock Primitive Utilization
- Global Clock Resources
- Global Clock Source Details
- Local Clock Resources
- Clock Regions utilization details
- Global Clocks placement details

Due to long netlist object names and to the large number of clock nets and clock primitives in typical designs, a short ID is given to specific clock resources:

- A unique Global Id “g<n>” for each net driven by a clock buffer
- A unique Source Id “src<n>” for clock generator, such as an MMCM or an input buffer.
- A unique Local Id “<n>” for clock nets not routed with global clock resources.

The Global Source and Local IDs simplify searching specific clock nets throughout the report. The original netlist object names are available in the last two columns of each table when applicable.
Clock Primitive Utilization Table

The Clock Primitive Utilization table shows the utilization summary for each clock primitive type and their physical constraints.

Note: The Clock Region constraints do not apply to 7 series devices.

Global Clock Resources Table

The Global Clock Resources table shows a summary for each clock net with important constraints and placement information, as shown in the following figure.

Figure 4-5: Report Clock Utilization – Clock Primitive Utilization Table

Figure 4-6: Report Clock Utilization – Global Clock Resources Table
The columns in the Global Clock Resources table are listed in the following table.

**Table 4-2: Global Clock Resources Table Details**

<table>
<thead>
<tr>
<th>Column</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global Id</td>
<td>Unique global clock net ID</td>
</tr>
<tr>
<td>Source Id</td>
<td>ID of the clock generating primitive connected to the clock buffer</td>
</tr>
<tr>
<td>Driver Type/Pin</td>
<td>Primitive pin connected to the clock net</td>
</tr>
<tr>
<td>Constraint</td>
<td>User physical constraint with highest precedence applied to the clock buffer</td>
</tr>
<tr>
<td></td>
<td>Priority rule is as follows:</td>
</tr>
<tr>
<td></td>
<td>1. LOC</td>
</tr>
<tr>
<td></td>
<td>2. CLOCK_REGION*</td>
</tr>
<tr>
<td></td>
<td>3. PBLOCK</td>
</tr>
<tr>
<td>* Does not apply to 7 series.</td>
<td></td>
</tr>
<tr>
<td>Site</td>
<td>Clock buffer location set by the user or by the Vivado implementation tools.</td>
</tr>
<tr>
<td>Clock Region</td>
<td>Device clock region where the buffer is located.</td>
</tr>
<tr>
<td></td>
<td>Does not apply to 7 series.</td>
</tr>
<tr>
<td>Root</td>
<td>Clock region where the clock net CLOCK_ROOT is located.</td>
</tr>
<tr>
<td></td>
<td>Does not apply to 7 series.</td>
</tr>
<tr>
<td>Clock Delay Group</td>
<td>Name of the group of clock nets specified by the user to force routing</td>
</tr>
<tr>
<td></td>
<td>matching by the Vivado implementation tools.</td>
</tr>
<tr>
<td></td>
<td>Does not apply to 7 series.</td>
</tr>
<tr>
<td>Load Clock Region</td>
<td>Number of clock regions where clock net loads are located.</td>
</tr>
<tr>
<td></td>
<td>Does not apply to 7 series.</td>
</tr>
<tr>
<td>Clock Loads</td>
<td>Number of clock pin loads.</td>
</tr>
<tr>
<td>Non-Clock Loads</td>
<td>Number of non-clock pin loads, such as FDCE/CE pins for example.</td>
</tr>
<tr>
<td>Clock Period</td>
<td>Period in ns of the timing clock which propagates on the clock net.</td>
</tr>
<tr>
<td></td>
<td>If several clocks propagate on the same clock net, the smallest clock period is reported.</td>
</tr>
<tr>
<td>Clock</td>
<td>Name of the timing clock which propagates on the clock net.</td>
</tr>
<tr>
<td></td>
<td>If several clocks propagate on the same clock net, “Multiple” is reported.</td>
</tr>
<tr>
<td>Driver Pin</td>
<td>Logical name of the clock net driver pin.</td>
</tr>
<tr>
<td>Net</td>
<td>Logical name of the clock net segment connected to the clock driver pin.</td>
</tr>
</tbody>
</table>
Global Clock Source Details Table

The Global Clock Source Details table shows the global clock connectivity and timing clock information for each clock generator output. The following figure shows the connectivity of each output of an MMCM (src0/src1) to clock buffers. The output CLKOUT0 of src1 drives two global clocks g7 and g8.

The columns in the Global Clock Source Details table are listed in the following table.

<table>
<thead>
<tr>
<th>Column</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Id</td>
<td>ID of the clock generating primitive.</td>
</tr>
<tr>
<td>Global Id</td>
<td>Global clock ID(s) driven by the Global Clock source pin.</td>
</tr>
<tr>
<td>Driver Type/Pin</td>
<td>Output primitive pin which generates the clock.</td>
</tr>
<tr>
<td>Constraint</td>
<td>User physical constraint with highest precedence applied to the clock buffer. Priority rule is as follows:</td>
</tr>
<tr>
<td></td>
<td>1. LOC</td>
</tr>
<tr>
<td></td>
<td>2. PBLOCK</td>
</tr>
<tr>
<td>Site</td>
<td>Global clock source location set by the user or by the Vivado implementation tools.</td>
</tr>
<tr>
<td>Clock Region</td>
<td>Device clock region where the clock source is located.</td>
</tr>
<tr>
<td>Clock Loads</td>
<td>Number of clock pin loads connected to Global Clock source pin.</td>
</tr>
<tr>
<td>Non-Clock Loads</td>
<td>Number of non-clock pin loads, such as FDCE/CE pins for example.</td>
</tr>
<tr>
<td>Source Clock Period</td>
<td>Period in ns of the timing clock generated by the Global Clock Source pin. If several clocks propagate on the same clock net, the smallest clock period is reported.</td>
</tr>
<tr>
<td>Clock</td>
<td>Name of the timing clock generated by the Global Clock Source pin. If several clocks propagate on the same clock net, &quot;Multiple&quot; is reported.</td>
</tr>
<tr>
<td>Driver Pin</td>
<td>Logical name of the Global Clock Source pin.</td>
</tr>
<tr>
<td>Net</td>
<td>Logical name of the clock net segment connected to the Global Clock Source pin.</td>
</tr>
</tbody>
</table>
Local Clock Details Table

The Local Clock Details table is only reported when local clocks are found in the design. A local clock is a clock net routed with regular fabric routing resources instead of global clocking resources. This situation usually occurs when a clock net is not driven by a clock buffer. The information provided by the table is similar to the one found in the Global Clock Resources table.

The following figure shows a local clock net driven by a 7 series MMCM output which directly drives a register clock pin (FDRE/C).

![Local Clock Net Diagram](image)

*Figure 4-8: Report Clock Utilization – Local Clock Example*
Clock Regions Tables

The Clock Regions section is only available for the UltraScale™ device families and includes several tables to cover primitive and routing resource utilization per clock region. In the Clock Utilization window, the **Show Metrics In Device Window** button can be used to select the resource types to be displayed over each clock region in the Device window, as shown in the following figure.

![Figure 4-9: Report Clock Utilization - Clock Region Resource Utilization Metrics in the Device Window](image)

The Clock Regions tables are:

- **Clock Primitives**: Utilization of each clock primitive type in each clock region.
- **Load Primitives**: Utilization of non-clock sequential primitives in each clock region.

For both Clock Primitives and Load Primitives table, the **Global Clock** column shows the number of global clock nets routed on the horizontal distribution layer with or without loads in the reported clock region. Clock nets routed on the vertical distribution layer with
no branching to the horizontal layer in the reported clock region are not counted. Clock nets routed on the routing layer are not counted.

- **Global Clock Summary**: Shows the utilization of Global Clocks per clock region in a table which corresponds to the device clock region floorplan, as shown in the following figure. This table is only available in the text report.

```
6. Clock Regions : Global Clock Summary

+-----------------------------+
|   | x0 | x1 | x2 | x3 |
+-----------------------------+
| x4 | 4  | 5  | 5  | 3  |
| x3 | 5  | 5  | 6  | 6  |
| x2 | 5  | 9  | 11 | 7  |
| x1 | 6  | 5  | 14 | 8  |
| x0 | 6  | 6  | 13 | 12 |
+-----------------------------+
```

*Figure 4-10: Report Clock Utilization – Global Clock Summary Example*

- **Routing Resource Utilization**: Shows the global clock routing resource utilization per type and per clock region.

**Key Resource Utilization Table**

The Key Resource Utilization table is only available for 7 series devices and is equivalent to the combination of all Clock Regions tables for UltraScale devices. The Global Clock Summary table is also available in the text report only.

**Global Clocks Tables**

The Global Clocks tables report the type of loads in each clock region for each global clock net, as well as timing clock information and the clock track ID used to route the clock net. When sorting the table by Global ID in the Vivado IDE, the clock regions where each global clock net is routed can easily be identified and highlighted in the device by simply selecting the corresponding table rows.

The column description is the same as in the Clock Primitive Utilization, Global Clock Resources, and Global Clock Source Details tables.

For UltraScale devices, the Global ID of clock nets routed over a clock region without driving any loads are tagged with a "+" character, as shown in the following figure.
Chapter 4: Viewing Reports and Messages

Report Control Sets

A control set is the unique combination of a clock signal, a clock enable signal, and a set/reset signal. Each slice supports at most one control set which any flip flop located in it can use. Flip flops with different control sets cannot be placed in the same slice.

The Control Sets Report lists the number of unique control sets in the design. Based on the placement of the designs, the tool displays the minimum number of register sites lost to the control set packing.

- Clock Signal: The logical clock signal name
- Enable Signal: The logical clock enable signal name
- Set/Reset Signal: The logical set/reset signal name
- Slice Load Count: The number of unique slices that contain cells connected to the control set
- BEL Load Count: The number of cells connected to the control set

Report DRC

The DRC Report is generated by the router. Before the router runs, the tool checks for a common set of design issues. The report lists the checks used in the run.

**IMPORTANT:** Review the Critical Warnings. The severity of a particular check may be increased later in the flow.

Report DRC runs common Design Rule checks to look for common design issues and errors.
Elaborated Design

The tool checks for DRCs related to I/O, Clock Placement, potential coding issues with your HDL, and XDC constraints. The RTL netlist typically does not have all the I/O Buffers, Clock Buffers, and other primitives the post synthesis designs have. Elaborated Design DRCs do not check for as many errors as later DRCs.

Synthesized Design and Implemented Design

- Checks for DRCs related to the post synthesis netlist.
- Checks for I/O, BUFG, and other placement.
- Basic checks on the attributes wiring on MGTs, IODELAYs, and other primitives.
- The same DRCs run taking into account any available placement and routing.
- DRCs have four severities: Info, Warning, Critical Warning, and Error. Critical Warnings and Errors do not block the design flow at this point.

Steps of the implementation flow also run the DRCs, which can stop the flow at critical points. The placer and router check for issues that block placement. Certain messages have a lower severity depending on the stage. These are DRCs flagging conditions that do not stop opt_design, place_design, or route_design from completing, but which can lead to issues on the board.

For example, some DRCs check that the user has manually constrained the package pin location and the I/O standard for all design ports. If some of these constraints are missing, place_design and route_design issue critical warnings. However, these DRCs appear as an ERROR in write_bitstream. The tools will not program a part without these constraints.

The decreased severity earlier in the flow allows you to run the design through implementation iterations before the final pinout has been determined. You must run bitstream generation for a comprehensive DRC signoff.

Figure 4-12 shows the Vivado IDE graphical user interface form of Report DRC.
Click a DRC to open the properties for a detailed version of the message. Look in the Properties window to view the details. Most messages have a hyperlink for nets, cells, and ports referenced in the DRC.

The DRC report is static. You must rerun Report DRC for the report to reflect design changes. The tool determines that the links are stale after certain design operations (such as deleting objects and moving objects), and invalidates the links.

Selecting an object from the hyperlink selects the object, but does not refresh the Properties window. To display the properties for the object, unselect and reselect it.

To create a DRC report in Tcl, run the command `report_drc`.

To write the results to a file, run the command `report_drc -file myDRCs.txt`.
Report Route Status

The Route Status Report is generated during the implementation flow and is available by using the `report_route_status` Tcl command.

The Route Status Report displays a breakdown of the nets in the design as follows:

- The total number of logical nets in the design
  - The number of nets that do not need routing resources
    - The number of nets that do not use routing resources outside of a tile. Examples include nets inside of a CLB, BlockRam, or I/O Pad.
    - The number of Nets without loads, if any exist
  - The number of routable nets that require routing resources
    - The number of unrouted nets, if any exist
    - The number of fully routed nets
  - The number of nets with routing errors
    - The number of nets with some unrouted pins, if any exist
    - The number of nets with antennas/islands, if any exist
    - The number of nets with resource conflicts, if any exist

The following is an example of the Report Route Status for a fully routed design:

```
Design Route Status
: # nets :
------------------------------------------- : ----------- :
# of logical nets.......................... :        6137 :
# of nets not needing routing.......... :         993 :
# of internally routed nets........ :         993 :
# of routable nets..................... :        5144 :
# of fully routed nets............. :        5144 :
# of nets with routing errors.......... :           0 :
------------------------------------------- : ----------- :
```
Report Noise

The Report Noise command performs the Simultaneous Switching Noise (SSN) calculation for Xilinx 7 series FPGA devices. By default, the Noise report opens in a new tab in the Noise window area of the Vivado IDE. You can export the results to a CSV or HTML file.

*Figure 4-14: Run SSN Analysis*

The Noise Report has four sections:

- Noise Report Summary Section
- Noise Report Messages Section
- Noise Report I/O Bank Details Section
- Noise Report Links Section

**Noise Report Summary Section**

The Summary section of the Noise Report includes:

- When the report ran
- Number and percentage of applicable ports analyzed
- Status, including whether it passed
- Number of Critical Warnings, Warnings, and Info messages

**Noise Report Messages Section**

The Messages section of the Noise Report includes a detailed list of the messages generated during the report.
Chapter 4: Viewing Reports and Messages

**Noise Report I/O Bank Details Section**

The I/O Bank Details section of the Noise Report includes a list of Pins, Standards, and Remaining Margin.

**Noise Report Links Section**

The Links section of the Noise Report contains links to documentation located online at [www.xilinx.com/support](http://www.xilinx.com/support).

To create an HTML version of the report, select the option or run the following Tcl command:

```
report_ssn -format html -file myImplementedDesignSSN.html
```

**Report Power**

The Power Report is generated after routing to report details of power consumption based on the current operating conditions of the device and the switching rates of the design. Power analysis requires a synthesized netlist or a placed and routed design.

- Use the `set_operating_conditions` command to set operating conditions.
- Use the `set_switching_activity` command to define switching activity.

The Report Power command is available when a Synthesized Design or an Implemented Design is open.
The Power Report estimates power consumption based on design inputs, including:

- Thermal statistics, such as junction and ambient temperature values.
  
  **Note:** You can set the junction temperature using the `-junction_temp` option of the `set_operating_condition` command. If you do not specify the temperature, the software computes it for you based on your design inputs.

- Data on board selection, including number of board layers and board temperature.

- Data on the selection of airflow and the head sink profile used by the design.

- Reporting the FPGA device current requirements from the different power supply sources.

- Allowing detailed power distribution analysis to guide power saving strategies and to reduce dynamic, thermal or off-chip power.

- Simulation activity files can be used to make power estimation more accurate.

---

**Figure 4-16:** Report Power Dialog Box
Analyzing the Power Report

Use the Report Power dialog box (Figure 4-16) to analyze power based on:

- Settings
- Power total
- Hierarchy
- Voltage rail
- Block type

For more information on the power report and analyzing the results, see the Vivado Design Suite User Guide: Power Analysis and Optimization (UG907) [Ref 8].

A text version of the power report is generated by default after route during the implementation process.

Reporting Power in a Non-Project Flow

In the non-project flow, report_power is available after link_design or synth_design. The report generated uses the available placement and routing to give more accurate power numbers. To generate this report from the Tcl Console or a script, run report_power.
Introduction to Timing Analysis

The Xilinx® Vivado® Integrated Design Environment (IDE) provides several reporting commands to verify that your design meets all timing constraints and is ready to be loaded on the application board. Report Timing Summary is the timing signoff report, equivalent to TRCE in the ISE® Design Suite. Report Timing Summary provides a comprehensive overview of all the timing checks, and shows enough information to allow you to start analyzing and debugging any timing issue. For more information, see Chapter 1, Logic Analysis Within the IDE.

You can generate this report in a window, write it to a file, or print it in your log file. Whenever Report Timing Summary shows that your design does not meet timing, or is missing some constraints, you can explore the details provided in the various sections of the summary and run more specific analysis. The other timing reports provide more details on a particular situation or to scope the analysis to some logic by using filters.

Before adding timing constraints to your design, you must understand the fundamentals of timing analysis, and the terminology associated with it. This chapter discusses some of key concepts used by the Xilinx Vivado Integrated Design Environment (IDE) timing engine.

Terminology

- The launch edge is the active edge of the source clock that launches the data.
- The capture edge is the active edge on the destination clock that captures the data.
- The source clock is also referred to as the launch clock.
- The destination clock is also referred to as the capture clock.
- The setup requirement is the relationship between the launch edge and the capture edge that defines the most restrictive setup constraint.
- The setup relationship is the setup check verified by the timing analysis tool.
- The hold requirement is the relationship between the launch edge and capture edge that defines the most restrictive hold constraint.
- The hold relationship is the hold check verified by the timing analysis tool.
Timing Paths

Timing paths are defined by the connectivity between the instances of the design. In digital designs, timing paths are formed by a pair of sequential elements controlled by the same clock, or by two different clocks.

Common Timing Paths

The most common paths in any design are:

- Path from Input Port to Internal Sequential Cell
- Internal Path from Sequential Cell to Sequential Cell
- Path from Internal Sequential Cell to Output Port
- Path from Input Port to Output Port

Path from Input Port to Internal Sequential Cell

In a path from an input port to a sequential cell, the data:

- Is launched outside the device by a clock on the board.
- Reaches the device port after a delay called the input delay [Synopsys Design Constraints (SDC) definition].
- Propagates through the device internal logic before reaching a sequential cell clocked by the destination clock.

Internal Path from Sequential Cell to Sequential Cell

In an internal path from sequential cell to sequential cell, the data:

- Is launched inside the device by a sequential cell, which is clocked by the source clock.
- Propagates through some internal logic before reaching a sequential cell clocked by the destination clock.

Path from Internal Sequential Cell to Output Port

In a path from an internal sequential cell to an output port, the data:

- Is launched inside the device by a sequential cell, which is clocked by the source clock.
- Propagates through some internal logic before reaching the output port.
- Is captured by a clock on the board after an additional delay called the output delay (SDC definition).
Path from Input Port to Output Port

In a path from an input port to output port, the data traverses the device without being latched. This type of path is also commonly called an in-to-out path. The input and output delays reference clock can be a virtual clock or a design clock.

Timing Paths Example

Figure 5-1 shows the paths described above. In this example, the design clock CLK0 can be used as the board clock for both DIN and DOUT delay constraints.

Timing Path Sections

Each timing path is composed of three sections:

- Source Clock Path
- Data Path
- Destination Clock Path

Source Clock Path

The source clock path is the path followed by the source clock from its source point (typically an input port) to the clock pin of the launching sequential cell. For a timing path starting from an input port, there is no source clock path.
Data Path

The data path is the section of the timing path where the data propagates, between the path startpoint and the path endpoint. The following definitions apply: (1) A path startpoint is a sequential cell clock pin or a data input port; and (2) A path endpoint is a sequential cell data input pin or a data output port.

Destination Clock Path

The destination clock path is the path followed by the destination clock from its source point, typically an input port, to the clock pin of the capturing sequential cell. For a timing path ending at an output port, there is no destination clock path. Figure 5-2 shows the three sections of a typical timing path.

Launch and Capture Edges

When transferring between sequential cells or ports, the data is:

- Launched by one of the edges of the source clock, which is called the launch edge.
- Captured by one of the edges of the destination clock, which is called the capture edge.

In a typical timing path, the data is transferred between two sequential cells within one clock period. In that case: (1) the launch edge occurs at 0ns; and (2) the capture edge occurs one period after.

The following section explains how the launch and capture edges define the setup and hold relationships used for timing analysis.
Understanding the Basics of Timing Analysis

Max and Min Delay Analysis

Timing analysis is the static verification that a design timing behavior will be predictable once loaded and run on hardware. It considers a range of manufacturing and environmental variations that are combined into delay models that are grouped by timing corners and corner variations. It is sufficient to analyze timing against all the recommended corners, and for each corner, to perform all the checks under the most pessimistic conditions. For example, a design targeted to a Xilinx FPGA device must pass the four following analyses:

- Max delay analysis in Slow Corner
- Min delay analysis in Slow Corner
- Max delay analysis in Fast Corner
- Min delay analysis in Fast Corner

Depending on the check performed, the delays that represent the most pessimistic situation are used. This is the reason why the following checks and delay types are always associated:

- Max delay with setup and recovery checks
- Min delay with hold and removal checks

Max delay with setup and recovery checks

- The worst-case delays (slowest delays) of a given corner are used for the source clock path and data/reset path accumulated delay.
- The best-case delays (fastest delays) of the same corner are used for the destination clock path accumulated delay.

Min delay with hold and removal checks

- The best-case delays (fastest delays) of a given corner are used for the source clock path and data/reset path accumulated delay.
- The worst-case delays (slowest delays) of the same corner are used for the destination clock path accumulated delay.

When mapped to the various corners, these checks become:

- setup/recovery (max delay analysis)
- hold/removal (min delay analysis)
**setup/recovery (max delay analysis)**

- source clock (Slow_max), datapath(Slow_max), destination clock (Slow_min)
- source clock (Fast_max), datapath(Fast_max), destination clock (Fast_min)

**hold/removal (min delay analysis)**

- source clock (Slow_min), datapath (Slow_min), destination clock (Slow_max)
- source clock (Fast_min), datapath (Fast_min), destination clock (Fast_max)

Delays from different corners are never mixed on a same path for slack computation.

Most often, setup or recovery violations occur with Slow corner delays, and hold or removal violations occur with Fast corner delays. However, since this is not always true (especially for I/O timing) Xilinx recommends that you perform both analyses on both corners.

### Setup/Recovery Relationship

The setup check is performed only on the most pessimistic setup relationship between two clocks. By default, this corresponds to the smallest positive delta between the launch and capture edges. For example, consider a path between two flip-flops that are sensitive to the rising edge of their respective clock. The launch and capture edges of this path are the clock rising edges only.

The clocks are defined as follows:

- **clk0** has a period of 6 ns with first rising @ 0 ns and falling edge @ 3 ns.
- **clk1** has a period of 4 ns with first rising @ 0 ns and falling edge @ 2 ns.

As Figure 5-3 shows, there are two unique setup relationships: Setup(1) and Setup(2).

![Figure 5-3: Setup Relationships](image-url)
Chapter 5: Performing Timing Analysis

The smallest positive delta from clk0 to clk1 is 2 ns, which corresponds to Setup(2). The Common Period is 12 ns, which corresponds to the time between two simultaneous alignments of the two clocks.

**TIP:** The relationships are established when considering the ideal clock waveforms, that is, before applying the insertion delay from the clock root to the flip-flop clock pin.

**IMPORTANT:** If the common period cannot be found over 1000 cycles of both clocks, the worst setup relationship over these 1000 cycles is used for timing analysis. For such case, the two clocks are called unexpandable, or clocks with no common period. The analysis will likely not correspond to the most pessimistic scenario. You must review the paths between these clocks to assess their validity and determine if they can be treated as asynchronous paths instead.

Once the path requirement is known, the path delays, the clocks uncertainty and the setup time are introduced to compute the slack. The typical slack equation is:

\[
\text{Data Required Time (setup)} = \text{capture edge time} + \text{destination clock path delay} - \text{clock uncertainty} - \text{setup time}
\]

\[
\text{Data Arrival Time (setup)} = \text{launch edge time} + \text{source clock path delay} + \text{datapath delay}
\]

\[
\text{Slack (setup)} = \text{Data Required Time} - \text{Data Arrival Time}
\]

As the equation shows, a positive setup slack occurs when the data arrives before the required time.

The recovery check is similar to the setup check, except that it applies to asynchronous pins such as preset or clear. The relationships are established the same way as for setup, and the slack equation is the same except that the recovery time is used instead of the setup time.

**Hold/Removal Relationship**

The hold check (also called hold relationship) is directly connected to the setup relationship. While the setup analysis ensures that data can safely be captured under the most pessimistic scenario, the hold relationship ensures that:

- The data sent by the setup launch edge cannot be captured by the active edge before the setup capture edge (H1a and H2a corresponding to setup edges S1 and S2 respectively in Figure 5-4).
- The data sent by the next active source clock edge after the setup launch edge cannot be captured by the setup capture edge (H2a and H2b corresponding to setup edges S1 and S2 respectively in Figure 5-4).
During hold analysis, the timing engine reports only the most pessimistic hold relationship between any two clocks. The most pessimistic hold relationship is not always associated with the worst setup relationship. The timing engine must review all possible setup relationships and their corresponding hold relationships to identify the most pessimistic hold relationship.

For example, consider the same path as in the setup relationship example. Two unique setup relationships exist.

The following figure illustrates the two hold relationships per setup relationship.

![Figure 5-4: Hold Relationships per Setup Relationship](image)

The greatest hold requirement is 0 ns, which corresponds to the first rising edge of both source and destination clocks.

Once the path requirement is known, the path delays, the clocks’ uncertainty, and the hold time are introduced to compute the slack. The typical slack equation is:

\[
\begin{align*}
\text{Data Required Time (hold)} &= \text{capture edge time} \\
&\quad + \text{destination clock path delay} \\
&\quad - \text{clock uncertainty} \\
&\quad + \text{hold time} \\
\text{Data Arrival Time (hold)} &= \text{launch edge time} \\
&\quad + \text{source clock path delay} \\
&\quad + \text{datapath delay} \\
\text{Slack (hold)} &= \text{Data Arrival Time} - \text{Data Required Time}
\end{align*}
\]

As the equation shows, the hold slack is positive when the new data arrives after the required time.

The removal check is similar to the hold check, except that it applies to asynchronous pins such as preset or clear. The relationships are established the same way as for hold, and the slack equation is the same except that the removal time is used instead of the hold time.
Path Requirement

The path requirement represents the difference in time between the capture edge and the launch edge of a timing path.

For example, when considering the same path and clocks as in the previous section, the following path requirements exist:

Setup Path Requirement (S1) = 1*T(clk1) - 0*T(clk0) = 4ns
Setup Path Requirement (S2) = 2*T(clk1) - 1*T(clk0) = 2ns

The corresponding hold relationships are:

- **Corresponding to setup S1**
  
  Hold Path Requirement (H1a) = (1-1)*T(clk1) - 0*T(clk0) = 0ns
  Hold Path Requirement (H1b) = 1*T(clk1) - (0+1)*T(clk0) = -2ns

- **Corresponding to setup S2**
  
  Hold Path Requirement (H2a) = (2-1)*T(clk1) - 1*T(clk0) = -2ns
  Hold Path Requirement (H2b) = 2*T(clk1) - (1+1)*T(clk0) = -4ns

The timing analysis is performed only with the two most pessimistic requirements. In the example above, these are:

- The setup requirement S2
- The hold requirement H1a

Clock Phase Shift

A clock phase-shift corresponds to a delayed clock waveform with respect to a reference clock due to special hardware in the clock path. In Xilinx FPGAs, clock phase-shift is usually introduced by the MMCM or PLL primitives, when their output clock property CLKOUT*_PHASE is non-zero.
Chapter 5: Performing Timing Analysis

**MMCM/PLL Phase Shift Modes**

During timing analysis, clock phase-shift can be modeled in two different ways by setting the MMCM/PLL `PHASESHIFT_MODE` property, as described in the following table.

Table 5-1: **MMCM/PLL PHASESHIFT_MODE Properties**

<table>
<thead>
<tr>
<th>PHASESHIFT_MODE Property</th>
<th>Phase-Shift Modeling</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>WAVEFORM</td>
<td>Clock Waveform Modification</td>
<td><code>set_multicycle_path -setup</code> constraints are usually needed to adjust the timing path requirement on clock-domain-crossing paths from or to the phase-shifted clock.</td>
</tr>
<tr>
<td>LATENCY</td>
<td>MMCM/PLL Insertion Delay</td>
<td>No additional multicycle path constraint is needed.</td>
</tr>
</tbody>
</table>

The default MMCM/PLL clock phase-shift mode varies across Xilinx FPGA families. However, the default mode can be overridden by the user on a per PLL/MMCM basis.

Table 5-2: **Default MMCM/PLL Clock Phase Shift Handling**

<table>
<thead>
<tr>
<th>Technology</th>
<th>Default MMCM/PLL Clock Phase Shift Handling</th>
</tr>
</thead>
<tbody>
<tr>
<td>7 Series</td>
<td>Clock Waveform Modification (WAVEFORM)</td>
</tr>
<tr>
<td>UltraScale</td>
<td>Clock Waveform Modification (WAVEFORM)</td>
</tr>
<tr>
<td>UltraScale+</td>
<td>MMCM/PLL Insertion Delay (LATENCY)</td>
</tr>
</tbody>
</table>

**IMPORTANT:** The MMCM/PLL PHASESHIFT_MODE property does not affect the device configuration.

The use of `PHASESHIFT_MODE=LATENCY` is particularly convenient when introducing skew between two clocks in order to meet timing. No additional multicycle path constraint is needed for adjusting the timing path requirement when setting the clock phase-shift to negative, null, or positive.

For legacy designs migrated from 7 series or UltraScale to UltraScale+, when the property `PHASESHIFT_MODE` is not set on the MMCM/PLL, the default behavior applies and the MMCM/PLL clock phase-shift is modeled as delay latency instead of clock edge shift. In this case, all multicycle path constraints that were specified in the legacy designs to account for a clock phase-shift need to be reviewed and usually removed. Such constraints can easily be identified by running the Methodology Checks (`report_methodology`). TIMING-31 flags multicycle paths between clocks where one of the clocks is phase-shifted and is generated by a MMCM/PLL with `PHASESHIFT_MODE` set to LATENCY.

The Clocking wizard and High Speed SelectIO™ Wizard both provide options to force the clock phase-shift modeling on each MMCM/PLL. The property `PHASESHIFT_MODE` is automatically saved inside the IP XDC.
**Phase Shift in Timing Reports**

A positive phase shift moves the source clock edge forward, delaying the clock edge. A negative phase shift moves the source clock edge backward. The modification of the clock waveform result in potentially different clock edges being used by the static timing analysis for the source and capture clocks.

In the examples below, clock `clkout0` (period 10 ns) is auto-derived by a MMCM.

- **No phase shift**
  
  ```vivado%
  set_property CLKOUT0_PHASE 0.000 [get_cells qpll/plle2_adv_inst]
  report_timing
  ...
  (clock clkout0 rise edge) 0.000 0.000 r
  ...
  MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
  -5.411   5.903 r mmcm_inst/mmcm_adv_inst/CLKOUT0
  ...
  ```
  
  The source clock edge is 0.0 ns.

- **Positive phase shift of 12.0 with PHASESHIFT_MODE=WAVEFORM**
  
  ```vivado%
  set_property CLKOUT0_PHASE 12.000 [get_cells qpll/plle2_adv_inst]
  report_timing
  ...
  (clock clkout0 rise edge) 0.333 0.333 r
  ...
  MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
  -5.411   5.903 r mmcm_inst/mmcm_adv_inst/CLKOUT0
  ...
  ```
  
  The source clock edge is delayed by 0.333 ns (10 ns / 360 * 12.0).

- **Positive phase shift of 12.0 with PHASESHIFT_MODE=LATENCY**
  
  ```vivado%
  set_property CLKOUT0_PHASE 12.000 [get_cells qpll/plle2_adv_inst]
  report_timing
  ...
  (clock clkout0 rise edge) 0.000 0.000 r
  ...
  MMCME2_ADV (Prop_mmcme2_adv_CLKIN1_CLKOUT0)
  -5.078     6.236 r mmcm_inst/mmcm_adv_inst/CLKOUT0
  ...
  ```
  
  The MMCM insertion delay is increased by 0.333 ns (10 ns / 360 * 12.0). The source clock edge is 0.0 ns.
Chapter 5: Performing Timing Analysis

• Negative phase shift of -15.0 with PHASESHIFT_MODE=WAVEFORM

```
vivado% set_property CLKOUT0_PHASE -15.000 [get_cells qpll/plle2_adv_inst]
vivado% report_timing
... (clock clkout0 rise edge) -0.417 -0.417 r
... MMCME2_ADV (Prop_mmcme2_adv_CLKN1_CLKOUT0)
    -5.411 5.903 r mmcm_inst/mmcm_adv_inst/CLKOUT0
...```

The source clock edge is moved backward by -0.417 ns (10 ns / 360 * -15.0).

• Negative phase shift of -15.0 with PHASESHIFT_MODE=LATENCY

```
vivado% set_property CLKOUT0_PHASE -15.000 [get_cells qpll/plle2_adv_inst]
vivado% report_timing
... (clock clkout0 rise edge) 0.000 0.000 r
... MMCME2_ADV (Prop_mmcme2_adv_CLKN1_CLKOUT0)
    -5.828 5.486 r mmcm_inst/mmcm_adv_inst/CLKOUT0
...```

The MMCM insertion delay is decreased by 0.417 ns (10 ns / 360 * -15.0). The source clock edge is 0.0 ns.

Clock Skew and Uncertainty

Skew and uncertainty both impact setup and hold computations and slack.

Skew Definition

Clock skew is the insertion delay difference between the destination clock path and the source clock path: (1) from their common point in the design; (2) to, respectively, the endpoint and startpoint sequential cell clock pins.

In the equation below:

• $T_{cj}$ is the delay from the common node to the endpoint clock pin.
• $T_{ci}$ is the delay from the common node to the startpoint clock pin:

$$T_{skew i,j} = T_{ci} - T_{cj}$$

Clock Pessimism Removal

A typical timing path report shows the delay details of both source and destination clock paths, from their root to the sequential cell clock pins. As explained below, the source and destination clocks are analyzed with a different delay, even on their common circuitry.
This delay difference on the common section introduces some additional pessimism in the skew computation. To avoid unrealistic slack computation, this pessimism is compensated by a delay called the Clock Pessimism Removal (CPR) value.

\[
\text{Clock Pessimism Removal (CPR)} = \text{common clock circuitry (max delay - min delay)}
\]

The CPR is added or subtracted to the skew depending on the type of analysis performed:

- **Max Delay Analysis (Setup/Recovery)**
  
  CPR is added to the destination clock path delay.

- **Min Delay Analysis (Hold/Removal)**
  
  CPR is subtracted from the destination clock path delay.

The Vivado Design Suite timing reports clock skew for each timing path as shown below (hold analysis in this case):

- **DCD** - Destination Clock Delay
- **SCD** - Source Clock Delay
- **CPR** - Clock Pessimism Removal

Clock Path Skew: 0.301ns (DCD - SCD - CPR)
Destination Clock Delay (DCD): 2.581ns
Source Clock Delay (SCD): 2.133ns
Clock Pessimism Removal (CPR): 0.147ns

In many cases, the CPR accuracy changes before and after routing. For example, let’s consider a timing path where the source and destination clocks are the same clock, and the startpoint and endpoint clock pins are driven by the same clock buffer.
Before routing, the common point is the clock net driver, that is, the clock buffer output pin. CPR compensates only for the pessimism from the clock root to the clock buffer output pin.

After routing, the common point is the last routing resource shared by the source and destination clock paths in the device architecture. This common point is not represented in the netlist, so the corresponding CPR cannot be directly retrieved by subtracting common clock circuitry delay difference from the timing report. The timing engine computes the CPR value based on device information not directly exposed to the user.

**Optimistic Skew**

Xilinx FPGA devices provide advanced clocking resources such as dedicated clock routing trees and Clock Modifying Blocks (CMB). Some of the CMBs have the capability to compensate the clock tree insertion delay by using a Phase Lock Loop circuit (present in PLL or MMCM primitives). The amount of compensation is based on the insertion delay present on the feedback loop of the PLL. In many cases, a PLL (or MMCM) drives several clock trees with the same type of buffer, including on the feedback loop. As the device can be large, the insertion delay on all these clock tree branches does not always match the feedback loop delay. The clocks driven by a PLL become over-compensated when the feedback loop delay is bigger than the source or destination clock delay. In this case, the sign of the CPR changes and it effectively removes skew optimism from the slack value. This is needed in order to ensure that there is no artificial skew at the common node of any timing path clocks during the analysis.

**Recommended:** Always use the CPR compensation during timing analysis to preserve the slack accuracy and the overall timing signoff quality.

**Clock Uncertainty**

Clock uncertainty is the total amount of possible time variation between any pair of clock edges. The uncertainty consists of the computed clock jitter (system, input, and discrete); the phase error introduced by certain hardware primitives; and any clock uncertainty specified by the user in the design constraints (`set_clock_uncertainty`).

For primary clocks, the jitter is defined by `set_input_jitter` and `set_system_jitter`. For clock generators such as MMCM and PLL, the tool computes the jitter based on user-specified jitter on its source clock and its configuration. For other generated clocks (such as flop based clock dividers), the jitter is the same as that of its source clock.

The user-specified clock uncertainty is added to the uncertainty computed by the Vivado Design Suite timing engine. For generated clocks (such as from MMCM, PLL, and flop-based clock dividers), uncertainty specified by the user on source clock does not propagate through the clock generators.
For more information on jitter and phase error definitions, see the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 5].

The clock uncertainty has two purposes:

- Reserve some amount of margin in the slack numbers for representing any noise on the clock that could affect the hardware functionality. Because the delay and jitter numbers are conservative, Xilinx does not recommend adding extra uncertainty to ensure proper hardware functionality.

- Over-constrain the paths related to a clock or a clock pair during one or several implementation steps. This increases the QoR margin that can be used to help the next steps to close timing on these paths. By using clock uncertainty, the clock waveforms and their relationships are not modified, so the rest of the timing constraints can still apply properly.

### Pulse Width Checks

The pulse width checks are some rule checks on the signal waveforms when they reach the hardware primitives after propagation through the device. They usually correspond to functional limits dictated by the circuitry inside the primitive. For example, the minimum period check on a DSP clock pin ensures that the clock driving a DSP instance does not run at higher frequency than what is tolerated by the internal DSP.

The pulse width checks do not affect synthesis or implementation. Their analysis must be performed once before the bitstream generation like any other design rule check provided by the Vivado Design Suite.

When a pulse width violation occurs, it is due to an inappropriate clock definition (pulse width and period checks) or an inappropriate clock topology that induces too much skew (max_skew check). You must review the Xilinx FPGA data sheet of the target device to understand the operation range of the primitive where the violation occurs. In the case of a skew violation, you must simplify the clock tree or place the clock resources closer to the violating pins.

### Reading a Timing Path Report

The timing path report provides the information needed to understand what causes a timing violation. The following sections describe the Timing Path Report.

The Timing Path Summary displays the important information from the timing path details. You can review it to find out about the cause of a violation without having to analyze the details of the timing path. It includes slack, path requirement, datapath delay, cell delay, route delay, clock skew, and clock uncertainty. It does not provide any information about cell placement.
For more information about the terminology used for timing constraints and timing analysis, as well as learn how slack and path requirement are determined, see Understanding the Basics of Timing Analysis, page 165.

Timing Path Summary Header Examples

Figure 5-6 shows an example of the Timing Path Summary Header in a text report.

Figure 5-7 shows an example of the Timing Path Summary header in the Vivado IDE.
Chapter 5: Performing Timing Analysis

Timing Path Summary Header Information

The Timing Path Summary header includes the following information:

- **Slack**
  
  A positive slack indicates that the path meets the path requirement, which is derived from the timing constraints. The Slack equation depends on the analysis performed.
  
  - Max delay analysis (setup/recovery)
    \[ \text{slack} = \text{data required time} - \text{data arrival time} \]
  
  - Min delay analysis (hold/removal)
    \[ \text{slack} = \text{data arrival time} - \text{data required time} \]
  
  Data required and arrival times are calculated and reported in the other subsections of the timing path report.

- **Source**
  
  The path startpoint and the source clock that launches the data. The startpoint is usually the clock pin of a sequential cell or an input port.
  
  When applicable, the second line displays the primitive and the edge sensitivity of the clock pin. It also provides the clock name and the clock edges definition (waveform and period).

- **Destination**
  
  The path endpoint and the destination clock that captures the data. The endpoint is usually the input data pin of the destination sequential cell or an output port. Whenever applicable, the second line displays the primitive and the edge sensitivity of the clock pin. It also provides the clock name and the clock edges definition (waveform and period).

- **Path Group**
  
  The timing group that the path endpoint belongs to. This is usually the group defined by the destination clock, except for asynchronous timing checks (recovery/removal) which are grouped in the **async_default** timing group. User-defined groups can also appear here. They are convenient for reporting purpose.

- **Path Type**
  
  The type of analysis performed on this path.
  
  - Max: indicates that the maximum delay values are used to calculate the data path delay, which corresponds to setup and recovery analysis.
  
  - Min: indicates that the minimum delay values are used to calculate the data path delay, which corresponds to hold and removal analysis.
  
  This line also shows which corner was used for the report: Slow or Fast.
Chapter 5: Performing Timing Analysis

• Requirement

The timing path requirement, when the startpoint and endpoint are controlled by the same clock, or by clocks with no phase-shift, is typically:

- One clock period for setup/recovery analysis.
- 0 ns for hold/removal analysis.

When the path is between two different clocks, the requirement corresponds to the smallest positive difference between any source and destination clock edges. This value is overridden by timing exception constraints such as multicycle path, max delay and min delay.

For more information on how the timing path requirement is derived from the timing constraints, Timing Paths, page 162.

• Data Path Delay

Accumulated delay through the logic section of the path. The clock delay is excluded unless the clock is used as a data. The type of delay corresponds to what the Path Type line describes.

• Logic Levels

The number of each type of primitives included in the data section of the path, excluding the startpoint and the endpoint cells.

• Clock Path Skew

The insertion delay difference between the launch edge of the source clock and the capture edge of the destination clock, plus clock pessimism correction (if any).

• Destination Clock Delay (DCD)

The accumulated delay from the destination clock source point to the endpoint of the path.

- For max delay analysis (setup/recovery), the minimum cell and net delay values are used
- For min delay analysis (hold/removal), the maximum delay values are used.

• Source Clock Delay (SCD)

The accumulated delay from the clock source point to the startpoint of the path.

- For max delay analysis (setup/recovery), the maximum cell and net delay values are used.
- For min delay analysis (hold/removal), the minimum delay values are used.
• Clock Pessimism Removal (CPR)

The absolute amount of extra clock skew introduced by the fact that source and destination clocks are reported with different types of delay even on their common circuitry.

After removing this extra pessimism, the source and destination clocks do not have any skew on their common circuitry.

For a routed design, the last common clock tree node is usually located in the routing resources used by the clock nets and is not reported in the path details.

• Clock Uncertainty

The total amount of possible time variation between any pair of clock edges.

The uncertainty comprises the computed clock jitter (system and discrete), the phase error introduced by certain hardware primitives and any clock uncertainty specified by the user in the design constraints (set_clock_uncertainty).

The user clock uncertainty is additive to the uncertainty computed by the Vivado IDE timing engine.

• Total System Jitter (TSJ)

The combined system jitter applied to both source and destination clocks. To modify the system jitter globally, use the set_system_jitter constraint. The virtual clocks are ideal and therefore do not have any system jitter.

• Total Input Jitter (TIJ)

The combined input jitter of both source and destination clocks.

To define the input jitter for each primary clock individually, use the set_input_jitter constraint. The Vivado IDE timing engine computes the generated clocks input jitter based on their master clock jitter and the clocking resources traversed. By default, the virtual clocks are ideal and therefore do not have any jitter.

For more information on clock uncertainty and jitter, see this link in the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5].

• Discrete Jitter (DJ)

The amount of jitter introduced by hardware primitives such as MMCM or PLL.

The Vivado IDE timing engine computes this value based on the configuration of these cells.
**Chapter 5: Performing Timing Analysis**

- **Phase Error (PE)**

  The amount of phase variation between two clock signals introduced by hardware primitives such as MMCM or PLL.

  The Vivado IDE timing engine automatically provides this value and adds it to the clock uncertainty.

- **User Uncertainty (UU)**

  The additional uncertainty specified by the `set_clock_uncertainty` constraint.

  For more information on how to use this command, see this link in the *Vivado Design Suite Tcl Command Reference Guide* (UG835) [Ref 3].

Additional lines can appear in the Timing Path Summary depending on the timing constraints, the reported path, and the target device:

- **Inter-SLR Compensation**

  The additional margin required for safely reporting paths that cross SLR boundaries in Xilinx 7 series SSI devices only.

- **Input Delay**

  The input delay value specified by the `set_input_delay` constraint on the input port. This line does not show for paths that do not start from an input port.

- **Output Delay**

  The output delay value specified by the `set_output_delay` constraint on the output port. This line does not show for paths that do not end to an output port.

- **Timing Exception**

  The timing exception that covers the path. Only the exception with the highest precedence is displayed, as it is the only one affecting the timing path requirement.

  For information on timing exceptions and their precedence rules, see *Timing Paths*. 
Timing Path Details

The second half of the report provides more details on the cells, pins, ports and nets traversed by the path. It is separated into three sections:

- **Source Clock Path**

  The circuitry traversed by the source clock from its source point to the startpoint of the datapath. This section does not exist for a path starting from an input port.

- **Data Path**

  The circuitry traversed by the data from the startpoint to the endpoint.

- **Destination Clock Path**

  The circuitry traversed by the destination clock from its source point to the datapath endpoint clock pin.

The Source Clock Path and Data Path sections work together. They are always reported with the same type of delay:

- max delay for setup/recovery analysis
- min delay for hold/removal analysis

They share the accumulated delay which starts at the data launch edge time, and accumulates delay through both source clock and data paths. The final accumulated delay value is called the *data arrival time*.

The destination clock path is always reported with the opposite delay to the source clock and data paths. Its initial accumulated delay value is the time when the data capture edge is launched on the destination clock source point. The final accumulated delay value is called the *data required time*.

The final lines of the report summarize how the slack is computed.

- For max delay analysis (setup/recovery)
  \[ \text{slack} = \text{data required time} - \text{data arrival time} \]
- For min delay analysis (hold/removal)
  \[ \text{slack} = \text{data arrival time} - \text{data required time} \]
Figure 5-8 shows an example of the Source Clock, Data and Destination Clock Paths in the text report. Because the path is covered by a simple period constraint of 5 ns, the source clock launch edge starts at 0 ns and the destination clock capture edge starts at 5 ns.

![Figure 5-8: Timing Path Details in Text Report](image)
Timing Path Details in Vivado IDE

The Timing Path Details in the Vivado IDE, as shown in Figure 5-9, shows the same information as is shown in the text report, seen in Figure 5-8.

*Figure 5-9: Timing Path Details in Vivado IDE*
The information on the path is displayed in five columns when the standard flow is used or six columns when the Incremental Compile is used:

- **Location**
  Where the cell or port is placed on the device.

- **Delay Type**
  The unisim primitive and the particular timing arc followed by the path. In case of a net, it shows the fanout \( f_o \) and its status. A net can be:
  - Unplaced: The driver and the load are not placed.
  - Estimated: The driver or the load or both are placed. A partially routed net is also reported as estimated.
  - Routed: The driver and the load are both placed, plus the net is fully routed.

- **Incr(ns) (text report) / Delay (IDE report)**
  The value of the incremental delay associated to a unisim primitive timing arc or a net. It can also show a constraint such as input/output delay or clock uncertainty.

- **Path(ns) (text report) / Cumulative (IDE report)**
  The accumulated delay after each segment of the path. On a given line, its value is the accumulated value from the previous + the incremental delay of the current line.

- **Netlist Resource(s) (text report) / Logical Resource (IDE report)**
  The name of the netlist object traversed.

- **Pin Reuse (Incremental Compile only)**
  Indicates whether the path is being reused from the reference run. Applicable values are ROUTING, PLACEMENT, MOVED, and NEW.

Each incremental delay is associated to one of the following edge senses:

- \( r \) (rising)
- \( f \) (falling)

The initial sense of the edge is determined by the launch or capture edge used for the analysis. It can be inverted by any cell along the path, depending on the nature of the timing arc. For example, a rising edge at the input of an inverter becomes a falling edge on the output.

The edge sense can be helpful in identifying that an overly-tight timing path requirement comes from a clock edge inversion along the source or destination clock tree.
Verifying Timing Signoff

Before going into the details of timing analysis, it is important to understand which part of the timing reports indicates that your design is ready to run in hardware.

**IMPORTANT:** Timing signoff is a mandatory step in the analysis of the implementation results, once your design is fully placed and routed.

By default, when using projects in the Vivado Design Suite, the runs automatically generate the text version of Report Timing Summary. You can also generate this report interactively after loading the post-implementation design checkpoint in memory.

**IMPORTANT:** Report Timing Summary does not cover the bus skew constraints. To report the bus skew constraints, you must run the `report_bus_skew` command separately on the command line. There is no GUI support for this command.

For a comprehensive Timing Signoff Verification methodology, see this link in the *UltraFast Design Methodology Guide for the Vivado Design Suite* (UG949) [Ref 6].
Chapter 6

Synthesis Analysis and Closure Techniques

Using the Elaborated View to Optimize the RTL

When analyzing the timing results after any implementation step with `report_timing`, `report_timing_summary` or `report_design_analysis`, you must review the structure of critical paths to understand if they can be mapped to logic primitives more efficiently by modifying the RTL, using synthesis attributes, or using different synthesis options. This is especially important for paths with high number of logic levels, which stress the implementation tools and limit the overall design performance.

Whenever you find a critical path with a high number of logic levels, you must question whether the functionality of the path requires so many logic levels or not. It is usually not easy to determine the optimal number of logic levels because it depends on your knowledge of the design and your knowledge of RTL optimization in general. It is a complex task to look at the post-synthesis optimized netlist and identify where the problem comes from in the RTL and how to improve it.

In project mode, the Vivado IDE helps simplifying the analysis by providing a powerful cross-probing mechanism between the synthesized or implemented design and the elaborated design. Do the following to cross-probe the synthesized/implemented design and the elaborated design:

1. Open both the synthesized/implemented design and the elaborated design in memory.
2. Select the timing path in the synthesized/implemented design view and show its schematics by pressing the F4 key.
3. Select the Elaborated Design in the Flow Navigator pane. The RTL cells that correspond to the timing path are also selected, so that you can open the RTL schematics (by pressing the F4 key) to view the same path in the elaborated view or trace from the endpoint pin back to the startpoint cell.
4. Review the RTL logic traversed by the path, especially the size of the operators or vectors.
Example

In the following example, a user has written a counter as follows:

```vhdl
signal cnt : integer := 0;

process (clk)
begin
  if(clk'event and clk = '1') then
    if(cnt = 16) then
      cnt <= 0;
    else
      cnt <= cnt + 1;
    end if;
    if(cnt = 8) then
dout <= din0;
    else
dout <= din1;
    end if;
  end if;
end process;
```

*Figure 6-1: Simple Counter VHDL Example*

The signal `cnt` counts from 0 to 16, which requires a 5-bit vector to encode. The post-route critical schematics is shown in *Figure 6-2*. The endpoint is the bit 30 of the `cnt` signal.

*Figure 6-2: cnt Counter Post-Route Critical Path Schematic*

After selecting the startpoint and endpoint cells of the critical path, you can visualize the equivalent path in the elaborated view by opening a schematics of the selected cells and expanding the logic from the endpoint pin back to the startpoint, as shown in *Figure 6-3*.

*Figure 6-3: cnt Counter in the Elaborated View*
The elaborated view shows that the adder-input has been sized to 32 bit, because the signal \texttt{cnt} is declared as an integer. In this particular example, the 32-bit operator is retained throughout the synthesis optimizations. The elaborated view gives a good hint of what is happening and you can change the RTL as follows in order to get a better optimized netlist and timing QoR. As the counter increments from 0 to 16, you can define a range for the signal \texttt{cnt} which forces the adder-inputs to be 5 bits wide instead of 32 bits wide.

```
signal cnt : integer range 0 to 16 := 0;

process (clk)
begin
  if(clk'event and clk = '1') then
    if(cnt = 16) then
      cnt <= 0;
    else
      cnt <= cnt + 1;
    end if;
    if(cnt = 8) then
      dout <= din0;
    else
      dout <= din1;
    end if;
  end if;
end process;
```

*Figure 6-4: Simple Counter VHDL example with Integer Range*

The change made to the RTL code will subsequently impact the synthesis optimization, which you can verify using the elaborated view instead of going through the entire compilation flow:

*Figure 6-5: \texttt{cnt} Counter in the Elaborated View after RTL improvement*
Decomposing Deep Memory Configurations for Balanced Power and Performance

In deep memory configurations, the synthesis attribute **RAM_DECOMP** can be used for better memory decomposition and reduced power consumption. This attribute can be set in the RTL. When the **RAM_DECOMP** attribute is applied to a memory, the memory is setup in a wider configuration (of primitives) instead of a deep and narrow configuration.

When the **CASCADE_HEIGHT** attribute is used along with the **RAM_DECOMP** attribute, the synthesis inference has more granular control on cascading thereby providing balanced power and performance. This approach requires additional address decoding logic but reduces the number of block RAMs accessed at any given point in time, which helps reduce power consumption. The memory configuration (32 × 16K) in Figure 6-6 shows an example of how the memory is decomposed when the **RAM_DECOMP** and **CASCADE_HEIGHT** attributes are set.

If the attributes **RAM_DECOMP** = power and **CASCADE_HEIGHT** = 4 are applied, 16 RAMB36E2 are inferred and the memory is decomposed as shown in Figure 6-7.
The base primitive used here is 32 × 1K and four block RAMs are cascaded with a built-in feature to form a 32 × 4K configuration. Four such parallel structures create a 16K deep memory. The outputs are multiplexed to generate the output data.

```verilog
module test
(
    input clk,
    input we,
    input [11:0] addr,
    input [31:0] din,
    output reg [31:0] dout );

    // ram_style = "block", ram_decomp = "power", cascade_height = 4 
reg [31:0] mem[15*1024];
reg [31:0] addr_reg;
reg [31:0] dout_tmp0;
reg [31:0] dout_tmp1;
reg [31:0] din_reg;
reg [31:0] we_reg;
always @(posedge clk)
begin
    addr_reg <= addr;
din_reg <= din;
we_reg <= we;
dout_tmp0 <= mem[addr_reg];
dout_tmp1 <= dout_tmp0;
dout <= dout_tmp1;
if (we_reg)
    mem[addr_reg] <= din_reg;
end
endmodule
```

**Figure 6-7:** Generated Structure for 32 × 16K Memory Configuration using RAM_DECOMP and CASCADE_HEIGHT Attributes

If only the RAM_DECOMP = power attribute is applied, 16 RAMB36E2 are inferred and the memory is decomposed as shown in Figure 6-9.
The base primitive used here is 32 × 1K and eight block RAMs are cascaded with a built-in feature to form a 32 × 8K configuration. Two such parallel structures create a 16K deep memory. The outputs are multiplexed to generate the output data. The multiplexer is a 2:1 MUX.

```
module test
  (input clk,
   input we,
   input [31:0] addr,
   input [31:0] din,
   output reg [31:0] dout);

  (* ram_style = "Block", ram_decomp = "power"*)
  reg [31:0] addr_reg;
  reg [31:0] dout_reg;
  reg [31:0] dout_tmp;
  reg [31:0] din_reg;
  reg we_reg;

  always @(posedge clk)
  begin
    addr_reg <= addr;
    din_reg <= din;
    we_reg <= we;
    dout_tmp <= we[addr_reg];
    dout_reg[31] <= dout_tmp[31];
    dout[31] <= dout_tmp[31];
    if (we_reg)
      addr[31] <= din_reg;
  end

endmodule
```

**Figure 6-9:** Generated Structure for 32 × 16K Memory Configuration using RAM_DECOMP Attribute

The overall power savings are similar for both the memory decomposition examples, shown in Figure 6-7 and Figure 6-9, because only one block RAM is active at any given point in time. However, in terms of performance, a four-level deep cascaded block RAM chain (Figure 6-7) provides better performance than an eight-level deep cascaded block RAM chain (Figure 6-9).
Optimizing RAMB Utilization when Memory Depth is not a Power of 2

The following test case can be used to observe the log file generated by the synthesis tool and see if there is any improvement that can be done to the RTL to guide the tool in a better way. The following code snippet shows a 40K-deep 36-bit wide memory description in VHDL. The address bus requires 16 bits.

```vhdl
library IEEE;
use IEEE STD_LOGIC_1164.ALL;
use IEEE NUMERIC_STD.ALL;

text is
  Port (clk : in STD_LOGIC;
        addr : in STD_LOGIC_VECTOR(15 downto 0);
        din : in STD_LOGIC_VECTOR(35 downto 0);
        we : in STD_LOGIC;
        dout : out STD_LOGIC_VECTOR(35 downto 0));
end test;

architecture rtl of test is
  signal addr_reg : STD_LOGIC_VECTOR(15 downto 0);
type mem_type is array (0 to 40959) of STD_LOGIC_VECTOR(35 downto 0);
  signal mem : mem_type;
begin
  process [clk]
  begin
    if (rising_edge(clk)) then
      addr_reg <= addr;
      if(we='1') then
        mem(to_integer(unsigned(addr_reg))) <= din;
      end if;
      dout <= mem(to_integer(unsigned(addr_reg)));
    end if;
  end process;
end rtl;
```

*Figure 6-11: 40K x 36 bits Memory RTL Example*

Using the `report_utilization` command post-synthesis, you can see that 72 block RAMs (BRAMs) are generated by the synthesis tool, as shown in *Figure 6-12*.

<table>
<thead>
<tr>
<th>Site Type</th>
<th>Used</th>
<th>Fixed</th>
<th>Available</th>
<th>Util%</th>
</tr>
</thead>
<tbody>
<tr>
<td>Block RAM Tile</td>
<td>72</td>
<td>0</td>
<td>1630</td>
<td>6.99</td>
</tr>
<tr>
<td>RAMB36/FIFO*</td>
<td>72</td>
<td>0</td>
<td>1630</td>
<td>6.99</td>
</tr>
<tr>
<td>RAMB36E1 only</td>
<td>72</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RAMB18</td>
<td>0</td>
<td>0</td>
<td>2660</td>
<td>0.80</td>
</tr>
</tbody>
</table>

*Figure 6-12: Number of Block RAMs Generated by Synthesis in the Utilization Report*
If you calculate the number of BRAMs that are supposed to be inferred for the 40K x 36 configuration, you would end up with fewer BRAMs than the synthesis tool generated.

The following shows the manual calculation for this memory configuration:

- 40K x 36 can be broken in two memories: (32K x 36) and (8K x 36)
- An address decoder based on the MSB address bits is required to enable one or the other memory for read and write operations, and select the proper output data.
- The 32K x 36 memory can be implemented with 32 RAMBs: 4 * 8 * (4K x 9)
- The 8K x 36 memory can be implemented with 8 RAMBs: 8 * (1K x 36)
- In total, 40 RAMBs are required to optimally implement the 40K x 36 memory.

To verify that the optimal number of RAMBs have been inferred, the synthesis log file includes a section that details how each memory is configured and mapped to FPGA primitives. As shown in the following figure, memory depth is treated as 64K, which gives a clue that non-power of 2 depths are not handled in an optimal way.

---

**Start ROM, RAM, DSP and Shift Register Reporting**

<table>
<thead>
<tr>
<th>Block RAM:</th>
</tr>
</thead>
</table>

<table>
<thead>
<tr>
<th>Module Name</th>
<th>RTL Object</th>
<th>PORT A (Depth x Width)</th>
<th>W</th>
<th>R</th>
<th>PORT B (Depth x Width)</th>
<th>M</th>
<th>R</th>
<th>OUT_REG</th>
<th>RAMB18</th>
<th>RAMB36</th>
<th>Hierarchical Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>test</td>
<td>mem.reg</td>
<td>64 K x 36 (READ_FIRST)</td>
<td>W</td>
<td>R</td>
<td>Port A</td>
<td>B</td>
<td>72</td>
<td>test/extra.2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*Figure 6-13: RAM Configuration and Mapping Section in the Synthesis Log*

The synthesis tool has used 64K x 1 (2 BRAMs with cascade feature), 36 such structures because of 36-bit data. So in total, you have 36 * 2 = 72 BRAMs. The following figure shows the code snippet that forces synthesis to infer the optimal number of RAMBs.
architecture rtl of test is
  signal addr_reg : std_logic_vector(15 downto 0);
  type ram_type_0 is array (0 to 32767) of std_logic_vector(35 downto 0);
  type ram_type_1 is array (0 to 8191) of std_logic_vector(35 downto 0);
  signal RAM_0 : ram_type_0;
  signal RAM_1 : ram_type_1;
  signal dout_0 : std_logic_vector(35 downto 0);
  signal dout_1 : std_logic_vector(35 downto 0);
begin
  process (clk)
  begin
    if clk'event and clk = '1' then
      addr_reg <= addr;
      if we = '1' and addr_reg(15) = '0' then
        RAM_0(to_integer(unsigned(addr_reg(14 downto 0)))) <= din;
      end if;
      dout_0 <= RAM_0(to_integer(unsigned(addr_reg(14 downto 0))));
    end if;
  end process;
  process (clk)
  begin
    if clk'event and clk = '1' then
      if we = '1' and addr_reg(15) = '1' then
        RAM_1(to_integer(unsigned(addr_reg(12 downto 0)))) <= din;
      end if;
      dout_1 <= RAM_1(to_integer(unsigned(addr_reg(12 downto 0))));
    end if;
  end process;
  dout <= dout_1 when addr_reg(15) = '1' else dout_0;
end rtl;

Figure 6-14: Optimized 40 K x 36 bits Memory RTL Example
Optimizing RAMB Input Logic to Allow Output Register Inference

The following RTL code snippet generates a critical path from block RAM (actually it is a ROM) with multiple logic levels ending at a flip-flop (FF). The RAMB cell has been inferred without the optional output registers (DOA-0), which adds over 1 ns extra delay penalty to the RAMB output path.

```verilog
module test (input clk, input [3:0] addr, output reg dout, dout_shift);
(+ rom_style = 'block' *) reg [15:0] mem [0:15];
reg [3:0] addr_reg0;
reg [3:0] addr_reg1;
reg [3:0] addr_reg2;
reg [3:0] addr_reg3;
reg [15:0] dout_mem;
initial
begin
    $readmem("init.txt",mem);
end
always@ (posedge clk)
begin
    addr_reg0 <= addr;
    addr_reg1 <= addr_reg0;
    addr_reg2 <= addr_reg1;
    addr_reg3 <= addr_reg2;
end
always@ (posedge clk)
begin
    dout_mem <= mem[addr_reg3];
    dout <= dout_mem;
    dout_shift <= addr_reg3;
end
endmodule
```

*Figure 6-15: Memory RTL Code Without Inferred RAMB Output Register*

The critical path for the above RTL code is shown by the tool, such as in *Figure 6-16.*
It is good practice to review the critical paths after synthesis and after each implementation step in order to identify which groups of logic need to be improved. For long paths or any paths that do not take advantage of the FPGA hardware features optimally, go back to the RTL description, try to understand why the synthesized logic is not optimal, and modify the code to help the synthesis tool improve the netlist.

Vivado has a powerful embedded debugging mechanism that you can use to start off with elaborated view. The elaborated view helps to identify where the problem could be, instead of manually searching through the RTL code. See the elaborated view shown in the following figure for the above RTL code snippet.

The elaborated view gives a good hint about the inefficient structure for the given test case. In this case, the problem comes from the address register fanout (addr_reg3_reg), which drives the memory address as well as some glue-logic, highlighted in blue.
RAMB inference by the synthesis tool requires a dedicated address register in the RTL code, which is not compatible with the current address register fanout. As a consequence, the synthesis tool re-times the output register in order to allow the RAMB inference instead of using it to enable the RAMB optional output register.

By replicating the address register in the RTL code so that the memory address and the glue logic are driven by separate registers, the RAMB will be inferred with the output registers enabled.

The RTL code and elaborated view after manual replication are shown in the following figures:

```verilog
module test (input clk, input [3:0] addr, output reg dout, dout_shift);

(* rom_style = "block" *) reg [15:0] mem [0:15];

reg [3:0] addr_reg0;
reg [3:0] addr_reg1;
reg [3:0] addr_reg2;
reg [3:0] addr_reg3;

/* KEEP = "true" *) reg [3:0] addr_reg3_dup;

reg [15:0] dout_mem;

initial
begin
    $readmem("init.txt",mem);
end

always@(posedge clk)
begin
    addr_reg0 <= addr;
    addr_reg1 <= addr_reg0;
    addr_reg2 <= addr_reg1;
    addr_reg3 <= addr_reg2;
    addr_reg3_dup <= addr_reg2;
end

always@(posedge clk)
begin
    dout_mem <= mem[addr_reg3];
    dout <= [dout_mem;
    dout_shift <= [dout_reg3_dup;
end
endmodule
```

*Figure 6-18:  RTL Code with the Replicated Address Register*
The critical path for the modified RTL code can be seen in the following figure. Notice the following:

- The `addr_reg2_reg` register is connected to the address pin of the block RAM.
- The `addr_reg3_reg` register has been absorbed in the Block RAM.
- The RAMB output register is enabled, which significantly reduces the datapath delay on the RAMB outputs.
Chapter 6: Synthesis Analysis and Closure Techniques

Improving Critical Logic on RAMB Outputs

The following test case highlights about improving critical paths through restructuring, such as when pushing macro (BRAM) closer to the destination register.

The following figure shows a 16x1 Multiplexer with only one input to the Multiplexer coming from BRAM and the rest of the inputs being fed by registers.

Critical path: BRAM -> 2 Logic levels -> FF.

![Figure 6-21: 16x1 Multiplexer Connected to Block RAM Outputs](Image)

Select=4'b0101 has ram-output
Figure 6-22 shows the critical path where the BRAM to FF path is highlighted in red. There are 2 logic levels from BRAM->FF as well as FF->FF. Because BRAM CLK->Q delay is higher for BRAM, BRAM->FF is critical.
Next, look at the RTL code snippet shown in Figure 6-23 to see whether there is a way to restructure the logic.

```vhdl
ram_sdp ram_sdp_inst (.clk(clk), .we(we), .addr(addr), .din(din_reg[15]), .dout(dout_from_ram));
always@(posedge clk)
begin
    sel_reg <= sel;
    din_reg <= din;
    case(sel_reg)
        4'd0: dout <= din_reg[0];
        4'd1: dout <= din_reg[1];
        4'd2: dout <= din_reg[2];
        4'd3: dout <= din_reg[3];
        4'd4: dout <= din_reg[4];
        4'd5: dout <= din_reg[5];
        4'd6: dout <= din_reg[6];
        4'd7: dout <= din_reg[7];
        4'd8: dout <= din_reg[8];
        4'd9: dout <= din_reg[9];
        4'd10: dout <= din_reg[10];
        4'd11: dout <= din_reg[11];
        4'd12: dout <= din_reg[12];
        4'd13: dout <= din_reg[13];
        4'd14: dout <= din_reg[14];
        4'd15: dout <= din_reg[15];
    endcase
end
```

**Figure 6-23: RTL Code Snippet**

The optimal way to restructure the logic is to rewrite the above code snippet by breaking the 16x1 Multiplexer into two multiplexers. You can exempt the condition of select value 4'd5 and use it as an enabling condition for the 2x1 Multiplexer as shown in Figure 6-24, creating this cascade Multiplexer structure results in FF->FF with 3 logic levels, but BRAM->FF is reduced to 1 logic level. This way, the BRAM->FF path has been improved, which helps the downstream tools for better placement because RAMB placement is more challenging than LUT and FF placement. In general, fewer long paths around Macro primitives such RAMB, FIFO, and DSP will yield better QoR for any given design.
Chapter 6: Synthesis Analysis and Closure Techniques

Figure 6-24: Cascade Multiplexer Structure to Reduce RAMB Output Logic Levels

```verilog
always @(*)
begin
  dout_nxt <= dout;
  case (sel_reg)
  4'd0: dout_nxt <= din_reg[0];
  4'd1: dout_nxt <= din_reg[1];
  4'd2: dout_nxt <= din_reg[2];
  4'd3: dout_nxt <= din_reg[3];
  4'd4: dout_nxt <= din_reg[4];
  4'd5: dout_nxt <= din_reg[5];
  4'd6: dout_nxt <= din_reg[6];
  4'd7: dout_nxt <= din_reg[7];
  4'd8: dout_nxt <= din_reg[8];
  4'd9: dout_nxt <= din_reg[9];
  4'd10: dout_nxt <= din_reg[10];
  4'd11: dout_nxt <= din_reg[11];
  4'd12: dout_nxt <= din_reg[12];
  4'd13: dout_nxt <= din_reg[13];
  4'd14: dout_nxt <= din_reg[14];
  4'd15: dout_nxt <= din_reg[15];
  endcase
end

always @(posedge clk)
begin
  sel_reg <= sel;
  din_reg <= din;
  if (sel_reg == 4'd0)
    dout <= dout_from_ramb;
  else
    dout <= dout_nxt;
end
```

Design Analysis and Closure Techniques
UG906 (v2017.1) April 28, 2017 www.xilinx.com
Implementation Analysis and Closure Techniques

Using the report_design_analysis Command

When timing closure is difficult to achieve or when you are trying to improve the overall performance of your application, you must review the main characteristics of your design after running synthesis and after any step of the implementation flow. It is relatively easy to gather the high-level metrics such as timing summary numbers (WNS/TNS/WHS/THS) (report_timing_summary) or various resource utilization numbers (report_utilization, report_clock_utilization, report_high_fanout_nets and report_control_sets). But it is more difficult to analyze and identify which particular aspect of your design is impacting a specific timing path and consequently the overall Quality of Result (QoR). The QoR analysis usually requires you to look at several global and local characteristics at the same time to figure out what is suboptimal in the design and the constraints, or which logic structure is not suitable for the target device architecture and implementation tools. The report_design_analysis command gathers logical, timing and physical characteristics in a few tables that can simplify the QoR root cause analysis.

Note: The report_design_analysis command does not report on the completeness and correctness of timing constraints. To verify your timing constraints, you must use the check_timing and report_exceptions commands, as well as the XDC and TIMING methodology DRCs. For more information on how to run these commands, see the corresponding sections:

- Report Timing Summary, page 22
- Report Exceptions, page 61

Two main categories of QoR problems are usually encountered:

- Timing Violations
- Congestion
Timing Violations

While analyzing and fixing the worst timing violation usually helps the overall QoR improvement, you must also review the other critical paths as they often contribute to the timing closure challenge. You can use the following command to report the 50 worst setup timing paths:

```
report_design_analysis -max_paths 50 -setup
```

Figure 7-1 shows an example of the Setup Path Characteristics table generated by this command.

<table>
<thead>
<tr>
<th>Paths</th>
<th>Requirement</th>
<th>Path Delay</th>
<th>Logic Delay</th>
<th>Net Delay</th>
<th>Clock skew</th>
<th>Skew</th>
<th>Clock Relationship</th>
<th>Logic Levels</th>
<th>Routes</th>
<th>Logical Path</th>
</tr>
</thead>
<tbody>
<tr>
<td>Path #1</td>
<td>10.000</td>
<td>9.022</td>
<td>6.223(34)</td>
<td>0.799(97)</td>
<td>-0.090</td>
<td>0.985</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #2</td>
<td>10.000</td>
<td>6.079</td>
<td>6.223(34)</td>
<td>0.856(97)</td>
<td>-0.458</td>
<td>0.370</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #3</td>
<td>10.000</td>
<td>9.079</td>
<td>6.223(34)</td>
<td>0.505(97)</td>
<td>-0.096</td>
<td>0.970</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #4</td>
<td>10.000</td>
<td>9.159</td>
<td>6.223(34)</td>
<td>0.969(97)</td>
<td>-0.385</td>
<td>0.970</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #5</td>
<td>10.000</td>
<td>9.198</td>
<td>6.223(34)</td>
<td>0.966(97)</td>
<td>-0.385</td>
<td>0.970</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #6</td>
<td>10.000</td>
<td>9.156</td>
<td>6.223(34)</td>
<td>0.282(97)</td>
<td>-0.385</td>
<td>0.970</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #7</td>
<td>10.000</td>
<td>9.154</td>
<td>6.223(34)</td>
<td>1.933(97)</td>
<td>-0.165</td>
<td>0.970</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #8</td>
<td>10.000</td>
<td>8.921</td>
<td>6.223(34)</td>
<td>6.699(97)</td>
<td>-0.525</td>
<td>0.971</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #9</td>
<td>10.000</td>
<td>8.199</td>
<td>6.223(34)</td>
<td>6.976(97)</td>
<td>-0.524</td>
<td>0.971</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #10</td>
<td>10.000</td>
<td>8.098</td>
<td>6.223(34)</td>
<td>6.478(97)</td>
<td>-0.524</td>
<td>0.971</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #11</td>
<td>10.000</td>
<td>6.036</td>
<td>6.223(34)</td>
<td>1.713(97)</td>
<td>-0.510</td>
<td>0.972</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #12</td>
<td>10.000</td>
<td>6.036</td>
<td>6.223(34)</td>
<td>0.713(97)</td>
<td>-0.510</td>
<td>0.972</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #13</td>
<td>10.000</td>
<td>8.082</td>
<td>6.223(34)</td>
<td>0.759(97)</td>
<td>-0.440</td>
<td>0.972</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
<tr>
<td>Path #14</td>
<td>10.000</td>
<td>9.019</td>
<td>6.223(34)</td>
<td>1.792(97)</td>
<td>-0.499</td>
<td>0.972</td>
<td>Safely Timed</td>
<td>0</td>
<td>1</td>
<td>TRUE DOES</td>
</tr>
</tbody>
</table>

Figure 7-1: Setup Path Characteristics

From the table, you can isolate which characteristics are introducing the timing violation for each path:

- **High logic delay percentage (Logic Delay)**
  - Are there many levels of logic? (Logic Levels)
  - Are there any constraints or attributes that prevent logic optimization? (Don’t Touch, Mark Debug)
  - Does the path include a cell with high logic delay such as RAMB or DSP?
  - Is the path requirement too tight for the current path topology? (Requirement)
- **High net delay percentage (Net Delay)**
  - Are there any high fanout nets in the path? (High Fanout, Cumulative Fanout)
  - Are the cells assigned to several Pblocks that can be placed far apart? (PBlocks)
  - Are the cells placed far apart? (Bounding Box Size, Clock Region Distance)
  - For SSI devices, are there nets crossing SLR boundaries? (SLR Crossings)
  - Are one or several net delay values a lot higher than expected while the placement seems correct? See the section on Congestion, page 206.
Chapter 7: Implementation Analysis and Closure Techniques

- Missing pipeline register in a RAMB or DSP cell (when present in the path)
  - See the Comb DSP, MREG, PREG, DOA_REG and DOA_REG values
- High skew (<-0.5 ns for setup and >0.5 ns for hold) (Clock Skew)
  - Is it a clock domain crossing path? (Start Point Clock, End Point Clock)
  - Are the clocks synchronous or asynchronous? (Clock Relationship)
  - Is the path crossing I/O columns? (IO Crossings)

For visualizing the details of the timing paths and their placement/routing in the Xilinx® Vivado® IDE, you must use the following command:

```bash
report_timing -max_paths 50 -setup -input_pins -name worstSetupPaths
```

The paths are sorted by slack and appear in the same order as in the Setup Path Characteristics table (shown in Figure 7-1).

The `report_design_analysis` command also generates a Logic Level Distribution table for the worst 1000 paths that you can use to identify the presence of longer paths in the design. The longest paths are usually optimized first by the placer in order to meet timing, which will potentially degrade the placement quality of shorter paths. You must always try to eliminate the longer paths to improve the overall QoR. Figure 7-2 shows an example of the Logic Level Distribution for a design with only one clock.

![Logic Level Distribution Table](image)

*Columns represent the logic levels per end point clock  
**Distribution is for top worst 1000 paths

**Figure 7-2: Logic Level Distribution Table**

Based on what you find, you can improve the netlist by changing the RTL or using different synthesis options, or you can modify the timing and physical constraints.
Design Analysis and Closure Techniques

Chapter 7: Implementation Analysis and Closure Techniques

Congestion

The `report_design_analysis` command reports several congestion tables which show the congested area seen by the placer and router algorithms, as well as the estimated congestion. You can generate these tables using the following command in the same Vivado tools session where the placer and router were run:

```
report_design_analysis -congestion
```

Figure 7-3 shows an example of the estimated congestion tables which are equivalent to the Vertical and Horizontal Routing congestion per CLB metrics available in the Vivado IDE. In this example, the congestion is low.

<table>
<thead>
<tr>
<th>Tile Name</th>
<th>RGM Grid Column</th>
<th>RGM Grid Row</th>
<th>Congestion in Window</th>
<th>Cell Names</th>
<th>Placer Max Overlap</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLAIM_1.X169102</td>
<td>44</td>
<td>109</td>
<td>6%</td>
<td>usbEngine1(100%)</td>
<td>Y</td>
</tr>
<tr>
<td>CLAIM_1.X169102</td>
<td>43</td>
<td>101</td>
<td>6%</td>
<td>usbEngine1(100%)</td>
<td>N</td>
</tr>
<tr>
<td>CLAIM_1.X169101</td>
<td>44</td>
<td>102</td>
<td>6%</td>
<td>usbEngine1(100%)</td>
<td>N</td>
</tr>
<tr>
<td>CLAIM_1.X169100</td>
<td>44</td>
<td>109</td>
<td>5%</td>
<td>usbEngine1(100%)</td>
<td>Y</td>
</tr>
<tr>
<td>CLAIM_1.X169100</td>
<td>44</td>
<td>103</td>
<td>5%</td>
<td>usbEngine1(100%)</td>
<td>N</td>
</tr>
<tr>
<td>CLAIM_1.X387160</td>
<td>88</td>
<td>41</td>
<td>5%</td>
<td>fftEngine(100%)</td>
<td>N</td>
</tr>
<tr>
<td>CLAIM_1.X169101</td>
<td>43</td>
<td>102</td>
<td>5%</td>
<td>usbEngine1(100%)</td>
<td>N</td>
</tr>
<tr>
<td>CLAIM_1.X169106</td>
<td>44</td>
<td>114</td>
<td>5%</td>
<td>usbEngine1(100%)</td>
<td>N</td>
</tr>
<tr>
<td>CLAIM_1.X169104</td>
<td>43</td>
<td>99</td>
<td>5%</td>
<td>usbEngine1(100%)</td>
<td>N</td>
</tr>
</tbody>
</table>

Figure 7-3: Estimated Congestion Tables

The names provided for the Module Names correspond to the hierarchical cells present in each reported Tile. You can retrieve the complete name using the following command:

```
get_cells -hier <moduleName>
```

Once the hierarchical cells present in the congested area are identified, you can use congestion alleviating techniques to try reducing the overall design congestion.
Identifying the Longest Logic Delay Paths in the Design

Timing paths correspond to logical paths in the design. Their delay is the accumulation of cell delays and net delays. The Vivado synthesis and implementation tools are timing-driven and work on optimizing the worst violating paths of your design throughout the compilation flow. If accumulated cell delay for a path is equal to or higher than the timing requirement (for example, usually the clock period of the path), the design is unlikely to meet timing after implementation. Analyzing the logic delay is better than simply counting logic levels, because it shows what the worst paths are before estimated or routed net delays become a factor. The result of this analysis is a list of the worst timing paths before placement and routing, and without net delay.

It is important to identify the paths that are the worst in terms of timing and not necessarily levels of logic. For example, unregistered block RAM have very large clock to out delay, while a series of carry chains may have multiple levels of levels of logic, each with a small delay. You must analyze these paths carefully before implementation. There are three typical categories for these long delay paths:

- block RAMs that do not take advantage of the embedded output register
- DSP48s that are not pipelined
- Long logic paths

The most efficient method of identifying these long paths is to run a timing report post synthesis with the routing estimates set to none. This can be done by changing the Interconnect model to none in the Timer Settings tab of the Vivado IDE Timing Report dialog box, or by using the following Tcl command in the Tcl console or shell:

```
set_delay_model -interconnect none
```

Review the timing results to identify any failing paths. If there are paths that fail to meet timing without any routing delay, these paths will be impossible to meet timing with actual routing. These paths MUST be addressed immediately. Typically, these would have to be fixed in RTL, but the violations could also be due to missing synthesis attributes, or incorrect timing constraints. After implementing the changes, the design will have sufficient slack as shown in Figure 7-4.
Identifying High Fanout Net Drivers

High fanout nets often lead to implementation issues. As die sizes increase with each FPGA family, fanout problems also increase. It is often difficult to meet timing on nets that have many thousands of endpoints, especially if there is additional logic on the paths, or if they are driven from non-sequential cells, such as LUTs or distributed RAMs.

Many times, designers address the high fanout nets in RTL or synthesis by using a global fanout limit or a \texttt{MAX\_FANOUT} attribute on a specific net. Physical optimization (\texttt{phys\_opt\_design}) automatically replicates the high fanout net drivers based on slack and placement information, and usually significantly improves timing. Xilinx recommends that you drive high fanout nets with a fabric register (FD*), which is easier to replicate and relocate during physical optimization. It is important to look at the list of high fanout signals post synthesis as well as post physical optimization. The command to identify these nets is \texttt{report\_high\_fanout\_nets}.

Once the report has been generated, the timing through the high fanout nets and corresponding schematic can be reviewed. This report does not list clocks as the high fanout driver. If a BUFG is in the Driver Type column, this BUFG is driving logic and possibly also clock pins.

\begin{verbatim}
### Report the high fanout net
report_high_fanout_nets -load_types -max_nets 100
### Report timing through specific high fanout net
report_timing -through [get_nets I\_GLOBAL\_RST\_N\_i] -name high_fanout_1
\end{verbatim}

Following is an example of a design in which \texttt{phys\_opt\_design} was able to reduce the fanout:

\textbf{Post Place Checkpoint: report\_high\_fanout\_nets}
The Timing Report for that net post physical optimization is:

TIP: Use of -timing and -load_types option with the report_high_fanout_nets command also shows the delay and the various types of loads for the high-fanout nets.

The fanout on that particular net was reduced from 2945 down to 464. More importantly, the reduction in fanout improved the timing (on this particular path the improvement was over 1 ns).

The FLAT_PIN_COUNT property of each net indicates the number of leaf cells connected to this net throughout the design hierarchy. Use the get_property command to extract the FLAT_PIN_COUNT property:

```
get_property FLAT_PIN_COUNT [get_nets my_hfn]
```

TIP: You can use Tcl scripting to create additional reports for the paths that propagate through any particular high fanout net.
Determining if Hold-Fixing is Negatively Impacting the Design

The Vivado Design Suite router prioritizes fixing hold over setup. This is because your design may work in the lab if you are failing setup by a small amount. There is always the option of lowering the clock frequency. If you have hold violations, the design will most likely not work.

In most cases, the router can meet the hold timing without affecting the setup. In some cases (mostly due to errors in the design or the constraints), the setup time will be significantly affected. Improper hold checks are often caused by improper set_multicycle_path constraints in which the -hold was not specified. In other cases, large hold requirements are due to excessive clock skew. In this case, Xilinx recommends that you review the clocking architecture for that particular circuit. For more information, see this link in the UltraFast Design Methodology Guide for the Vivado Design Suite (UG949) [Ref 6].

This may occur if your design meets setup timing post placement, but fails setup post route.

_TIP:_ Analyze the estimated hold timing post place and identify any unusually large hold violations (over 500ps).

If you suspect that hold fixing is affecting timing closure, you can use one of the following to determine if this is the case:

- **Method 1:** Routing without hold fixing
- **Method 2:** Run report_timing -min on Worst Failing Setup Path

**Method 1: Routing without hold fixing**

1. Read the post-placed checkpoint into Vivado Design Suite.
2. Add a constraint to disable all hold checking:
   ```
   set_false_path -hold -to [all_clocks]
   ```
   **CAUTION!** This constraint is for test purposes only. Never do this for designs that will be put into production or delivered to another designer. You must remove this constraint before the production design.
3. Run route_design and report_timing_summary.

If there is a significant difference between the WNS with and without the hold checks, the hold violations might be too large, and the setup paths are being affected.
Method 2: Run report_timing -min on Worst Failing Setup Path

To determine whether the worst failing setup path is due to hold fixing, review the hold timing of that path. In the Vivado IDE, right click and report timing on source to destination. As opposed to doing the setup timing analysis, it is important to look at the hold timing. Once you have the hold report, verify the requirement and ensure that additional delay was not added on the path to be able to meet hold.

Figure 7-6: Running Timing Report on Specific Paths
Quickly Analyzing All Failing Paths

The `report_timing_summary` command is a powerful tool for determining all the timing information for your design. Sometimes it is beneficial to simply look at all of the failing paths in a single report. The command below works from the command line or from within the IDE.

```
report_timing -max_paths 100 -slack_less_than 0 -name worse_100_setup
```

**TIP:** When using the IDE, you can export the timing results to a spreadsheet to do more comprehensive analysis of the failing paths.

The command above reports the top 100 failing paths. If there are less than 100 failing paths, only the failing paths are reported because of the `-slack_less_than 0` option. Reviewing the failing paths in a single list helps to quickly identify the order of magnitude differences among the failing paths.

For example, the WNS could be -3 ns, which affects a few paths, but then the next WNS in the list could be at -300 ps or better.

By default, when you analyze timing failures, you see the single worst timing path per endpoint. There are generally many similar paths for the common failing endpoint.

To review all worst paths for a single endpoint, use the `-nworst` option with the `report_timing` command. For example, run the following command to see all paths leading to the worst case failing endpoint (assuming there are less than 100):

```
report_timing -max_paths 100 -nworst 100
```

Reviewing all the worst paths may yield considerable data. To minimize the amount of data to analyze, you can review only the unique portions of paths by using the `-unique_pins` option with the `report_timing` command. This provides a single path for each unique combination of pins through the timing path. For example:

```
report_timing -max_paths 100 -nworst 100 -unique_pins
```
Floorplanning

This section discusses Floorplanning and includes:

- About Floorplanning
- Understanding Floorplanning Basics
- Using Pblock-Based Floorplanning
- Locking Specific Logic to Device Sites
- Floorplanning With Stacked Silicon Interconnect (SSI) Devices

About Floorplanning

Floorplanning can help a design meet timing. Xilinx recommends that you floorplan when a design does not meet timing consistently, or has never met timing. Floorplanning is also helpful when you are working with design teams, and consistency is most important.

Floorplanning can improve the setup slack (TNS, WNS) by reducing the average route delay. During implementation, the timing engine works on resolving the worst setup violations and all the hold violations. Floorplanning can only improve setup slack.

Manual floorplanning is easiest when the netlist has hierarchy. Design analysis is much slower when synthesis flattens the entire netlist. Set up synthesis to generate a hierarchical netlist. For Vivado synthesis use:

- synth_design -flatten_hierarchy rebuilt
  
  or

- The Vivado Synthesis Defaults strategy

Large hierarchical blocks with intertwined logical paths can be difficult to analyze. It is easier to analyze a design in which separate logical structures are in lower sub-hierarchies. Consider registering all the outputs of a hierarchical module. It is difficult to analyze the placement of paths that trace through multiple hierarchical blocks.
Understanding Floorplanning Basics

Not every design will always meet timing. You may have to guide the tools to a solution. Floorplanning allows you to guide the tools, either through high-level hierarchy layout, or through detailed gate placement.

You will achieve the greatest improvements by fixing the worst problems or the most common problems. For example if there are outlier paths that have significantly worse slack, or high levels of logic, fix those paths first. The Tools > Timing > Create Slack Histogram command can provide a view of outlier paths. Alternatively, if the same timing endpoint appears in several negative slack paths, improving one of the paths might result in similar improvements for the other paths on that endpoint.

Consider floorplanning to increase performance by reducing route delay or increasing logic density on a non-critical block. Logic density is a measure of how tightly the logic is packed onto the chip.

Floorplanning can help you meet a higher clock frequency and improve consistency in the results. There are multiple approaches to floorplanning, each with its advantages and disadvantages.

Detailed Gate-Level Floorplanning

Detailed gate-level floorplanning involves placing individual leaf cells in specific sites on the device.

Advantages of Detailed Gate-Level Floorplanning

- Detailed gate-level floorplanning works with hand routing nets.
- Detailed gate-level floorplanning can extract the most performance out of the device.

Disadvantages of Detailed Gate-Level Floorplanning

- Detailed gate-level floorplanning is time consuming.
- Detailed gate-level floorplanning requires extensive knowledge of the device and design.
- Detailed gate-level floorplanning may need to be redone if the netlist changes.

RECOMMENDED: Use detailed gate-level floorplanning as a last resort.
Information Reuse

Reuse information from a design that met timing. Use this flow if the design does not consistently meet timing. To reuse information:

1. Open two implementation runs:
   a. One for a run that is meeting timing.
   b. One for a run that is not meeting timing.

   **TIP:** On a computer with multiple monitors, select Open Implementation in New Window to open a design in a new window.

2. Look for the differences between the two designs.
   a. Identify some failing timing paths from report_timing_summary.
   b. On the design that is meeting timing, run report_timing in min_max mode to time those same paths on the design that meets timing.

3. Compare the timing results:
   a. Clock skew
   b. Datapath delay
   c. Placement
   d. Route delays

4. If there are differences in the amount of logic delay between path end points, revisit the synthesis runs.

Review I/O and Cell Placement

Review the placement of the cells in the design. Compare two I/O reports to review the I/O placement and I/O standards. Make sure all the I/Os are placed. A simple search finds all I/Os without fixed placement as shown in the following figure.
If clock skew has changed between the runs, consider re-using the clock primitive placement from the run that met timing. The Clock Utilization Report lists the placement of the clock tree drivers, as shown in the following figure.

**Figure 7-7: I/O Is Not Fixed**

**Figure 7-8: Clock Locations**
The LOC constraints can easily be copied into your XDC constraints file.

Many designs have met timing by reusing the placement of the Block RAMs and DSPs. Select **Edit > Find** to list the instances.

**Figure 7-9: DSP or RAM**

### Adding Placement Constraints

Fix the logic to add the placement constraints to your XDC.

1. Select the macros from the find results.
2. Right click and select **Fix Cells** (shown in the following figure).
RECOMMENDED: Analyze the placement based on hierarchy name and highlight before fixing the placement.

Reusing Placement

It is fairly easy to reuse the placement of I/Os, Global Clock Resources, BlockRAM macros, and DSP macros. Re-using this placement helps to reduce the variability in results from one netlist revision to the next. These primitives generally have stable names. The placement is usually easy to maintain.

TIP: Do not reuse the placement of general slice logic. Do not reuse the placement for sections of the design that are likely to change.

Reusing Placement with Incremental Compile

Incremental Compile allows reuse of place and route data from a previous run. To set it up, simply reference an existing placed or routed DSP before place_design. It is possible to reuse a full design, a hierarchy level, or a cell type like DSPs or BRAMs. Incremental Compile also automatically handles changes made to parts of a design.
For more information, see the Vivado Design Suite User Guide: Implementation (UG904) [Ref 7].

Floorplanning Techniques

Consider gate-level floorplanning for a design that has never met timing, and in which changing the netlist or the constraints are not good options.

**RECOMMENDED:** Try hierarchical floorplanning before considering gate level floorplanning.

**Hierarchical Floorplanning**

Hierarchical floorplanning allows you to place one or more levels of hierarchy in a region on the chip. This region provides guidance to the placer at a global level, and the placer does the detailed placement. Hierarchical floorplanning has the following advantages over gate-level floorplanning:

- Hierarchical floorplan creation is fast compared to gate-level floorplanning. A good floorplan can improve timing. The floorplan is resistant to design change.
- The level of hierarchy acts as a container for all the gates. It will generally work if the netlist changes.

In hierarchical floorplanning:

- Identify the lower levels of hierarchy that contain the critical path.
- Use the top level floorplan to identify where to place them.
- Implementation places individual cells.
- Has comprehensive knowledge of the cells and timing paths.
- Generally does a good job of fine grain placement.

**Manual Cell Placement**

Manual cell placement can obtain the best performance from a device. When using this technique, designers generally use it only on a small block of the design. They may hand place a small amount of logic around a high speed I/O interface, or hand place Block RAMs and DSPs. Manual placement can be slow.

All floorplanning techniques can require significant engineering time. They might require floorplan iterations. If any of the cell names change, the floorplan constraints must be updated.

When floorplanning, you should have an idea of final pinout. It is useful to have the I/Os fixed. The I/Os can provide anchor points for starting the floorplan. Logic that communicates to I/Os migrates towards the fixed pins.
TIP: Place blocks that communicate with I/Os near their I/Os. If the pinout is pulling a block apart, consider pinout or RTL modification.

The floorplan shown in Figure 7-11 might not help timing. Consider splitting the block apart, changing the source code, or constraining only the Block RAMs and DSPs. Also consider unplacing I/O registers if external timing requirements allow.
The Pblock mentioned in this section is represented by the XDC constraints:

```plaintext
create_pblock Pblock_usbEngine
add_cells_to_pblock [get_pblocks Pblock_usbEngine] [get_cells -quiet [list usbEngine1]]
resize_pblock [get_pblocks Pblock_usbEngine] -add {SLICE_X8Y105:SLICE_X23Y149}
resize_pblock [get_pblocks Pblock_usbEngine] -add {DSP48_X0Y42:DSP48_X1Y59}
resize_pblock [get_pblocks Pblock_usbEngine] -add {RAMB18_X0Y42:RAMB18_X1Y59}
resize_pblock [get_pblocks Pblock_usbEngine] -add {RAMB36_X0Y21:RAMB36_X1Y29}
```

The first line creates the Pblock. The second line (`add_cells_to_pblock`) assigns the level of hierarchy to the Pblock. There are four resource types (SLICE, DSP48, RAMB18, RAMB36) each with its own grid. Logic that is not constrained by a grid can go anywhere in the device. To constrain just the Block RAMs in the level of hierarchy, disable the other Pblock grids.

The resulting XDC commands define the simplified Pblock:

```plaintext
create_pblock Pblock_usbEngine
add_cells_to_pblock [get_pblocks Pblock_usbEngine] [get_cells -quiet [list usbEngine1]]
resize_pblock [get_pblocks Pblock_usbEngine] -add {RAMB18_X0Y42:RAMB18_X1Y59}
resize_pblock [get_pblocks Pblock_usbEngine] -add {RAMB36_X0Y21:RAMB36_X1Y29}
```

The Block RAMs are constrained in the device, but the slice logic is free to be placed anywhere on the device.

**TIP:** When placing Pblocks, be careful not to floorplan hierarchy in such a manner that it crosses the central config block.
Using Pblock-Based Floorplanning

When you integrate RTL into a design, it helps to visualize the design inside the device. Graphically seeing how the blocks interconnect between themselves and the I/O pinout after synthesis helps you to understand your design.

To view the interconnect, generate a top level floorplan using Pblocks on upper levels of hierarchy. To break apart the top level RTL into Pblocks, select **Tools > Floorplanning > Auto Create Pblocks**.

To place the blocks in the device, select **Tools > Floorplanning > Place Pblocks**. The tool sizes the Pblocks based on the slice count and target utilization.

Pblocks can be more than one hundred percent full during analysis, but not during implementation. Overfilling the Pblock makes them smaller on the device. This is a useful technique for getting an overview of the relative size of your design top-level blocks, and how they will occupy the device.
Chapter 7: Implementation Analysis and Closure Techniques

Top-Level Floorplan

The top-level floorplan shows which blocks communicate with I/Os (green lines). Nets connecting two Pblocks are bundled together. The bundles change size and color based on the number of shared nets. Two top-level floorplans are shown in Figure 7-15 and Figure 7-16.

The Data Path Top Level Floorplan shows how the data flows between the top-level blocks of the design. Each block communicates only with two neighbors. The green lines show well-placed I/Os that communicate with a single block.
The Control Path Floorplan displays a design in which all the blocks communicate with a central block. The largest connection is between the central block and the block in the bottom right. The central block must spread out around the design to communicate with all the other loads.

Figure 7-15: **Data Path Top Level Floorplan**
Chapter 7: Implementation Analysis and Closure Techniques

Reviewing the Floorplan

Consider device resources when reviewing the floorplan. The Pblock sizing does not take into account specialized device resources such as:

- Block RAM
- DSP48s
- MGTs
- ClockBuffers

**TIP: Review the blocks with the floorplan and utilization in mind.**
Locking Specific Logic to Device Sites

You can place cells on specific locations on the FPGA device, such as placing all the I/O ports on a Xilinx 7 series FPGA design. Xilinx recommends that you place the I/Os before attempting to close timing.

The I/O placement can impact the cell placement in the FPGA fabric. Hand placing other cells in the fabric can help provide some consistency to clock logic and macro placement, with the goal of more consistent implementation runs.

<table>
<thead>
<tr>
<th>Table 7-1: Constraints Used to Place Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Constraint</strong></td>
</tr>
<tr>
<td>LOC</td>
</tr>
<tr>
<td>BEL</td>
</tr>
</tbody>
</table>

Fixed and Unfixed Cells

Fixed and Unfixed apply to placed cells. They describe the way in which the Vivado tools view placed cells in the design.

For more information about Fixed and Unfixed Cells, refer to this link in the Vivado Design Suite User Guide: Implementation (UG904) [Ref 7].

**RECOMMENDED:** After the I/Os are placed, use a hierarchical Pblock floorplan as a starting point for user-controlled placement. Hand placing logic should be used when Pblocks have been found not to work.

Floorplanning With Stacked Silicon Interconnect (SSI) Devices

There are extra considerations for Stacked Silicon Interconnect (SSI) parts. The SSI parts are made of multiple Super Logic Regions (SLRs), joined by an interposer. The interposer connections are called Super Long Lines (SLLs). There is some delay penalty when crossing from one SLR to another.

Keep the SLRs in mind when structuring the design, generating a pinout, and floorplanning. Minimize SLL crossings by keeping logic cells of critical timing paths inside a single SLR.
The I/Os must be placed in the same SLR as the relevant I/O interface circuitry. You must also carefully consider clock placement when laying out logic for SSI parts.

**RECOMMENDED:** Let the placer try an automatic placement of the logic into the SSI parts before doing extensive partitioning. Analyzing the automatic placement may suggest floorplanning approaches you were not considering.

*Figure 7-17: Minimize SLR Crossings*
Timing Methodology Checks

TIMING-1: Invalid Clock Waveform on Clock Modifying Block

Invalid clock waveform for clock `<CLOCK_NAME>` specified at a `<CELL_TYPE>` output `<PIN_NAME>` that does not match the Clock Modifying Block (CMB) settings. The waveform of the clock is `<VALUE>`. The expected waveform is `<VALUE>`.

Description

The Xilinx® Vivado® Design Suite automatically derives clocks on the output of a CMB based on the CMB settings and the characteristics of the incoming master clock. If the user defines a generated clock on the output of the CMB, Vivado does not auto-derive a generated clock on the same definition point (net or pin). The DRC warning is reporting that the user-defined generated clock does not match the expected auto-derived clock that Vivado would automatically create. This could lead to hardware failures because the timing constraints for the design do not match what happens on the device.

Resolution

If the user-defined generated clock is unnecessary, remove the constraint and use the auto-derived clock instead. If constraint is necessary, verify that the generated clock constraint matches the auto-derived clock waveform or modify the CMB properties to match the expected clock waveform. If the intention is to force the name of the auto-derived clock, the recommendation is to use the `create_generated_clock` constraint with only the `-name` option defined and the name of the object where the clock is defined (typically output pin of CMB). See the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5] for additional information about creating generated clocks and restrictions of the auto-derived clocks renaming constraint.
Example

In the following figure, a `create_generated_clock` constraint was defined on the MMCM instance pin `CLKOUT0`, but doesn't match the auto-derived waveform generated by Vivado from the MMCM attribute settings.

To just rename the auto-derived clock, use the following constraint right after the master clock definition in your constraint files:

```plaintext
create_generated_clock -name clkName [get_pins clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT0]
```

*Figure A-1: Invalid Clock Waveform on Clock Modifying Block*
TIMING-2: Invalid Primary Clock on Internal Pin

A primary clock `<CLOCK_NAME>` is created on an inappropriate pin `<PIN_NAME>`. It is recommended to create a primary clock only on a proper clock root (input port or primitive output pin with no timing arc).

**Description**

A primary clock must be defined on the source of the clock tree. For example, this would be the input port of the design. When a primary clock is defined in the middle of a logic path, timing analysis can become inaccurate because it ignores the insertion delay prior to the primary clock source point, which prevents proper skew computation. Therefore, a primary clock created on an internal driver pin should be discouraged. The consequence could be a failure in hardware.

**Resolution**

Modify the `create_clock` constraint to use the actual clock tree source.

**Example**

In the following figure, the primary clock definition, `create_clock` constraint, was placed on the output pin of the `IBUFCTRL` instance. If the clock `clk_pin_p` is used to time an input or output port path, the slack will be inaccurate because part of the clock tree insertion delay will be missing. The primary clock definition for the differential input buffer should be placed on the top-level port `clk_pin_p`.

![Figure A-2: Invalid Primary Clock on Internal Pin](image)
TIMING-3: Invalid Primary Clock on Clock Modifying Block

A primary clock <CLOCK_NAME> is created on the output pin or net <PIN/NET_NAME> of a Clock Modifying Block.

Description

Vivado automatically derives clocks on the output of a CMB based on the CMB settings and the characteristics of the incoming master clock. If the user defines a primary clock on the output of the CMB, Vivado does not auto-derive a clock on the same output. This DRC is reporting that a primary clock was created on the output of the CMB, which breaks the relationship with the incoming clock and prevents proper clock insertion delay computation. This is not recommended because it can lead to inaccurate timing analysis and incorrect hardware behavior.

Resolution

Modify the constraints to remove the create_clock constraint on the output of the CMB. If the intention is to force the name of the auto-generated clock, Xilinx recommends using the create_generated_clock constraint with only the -name option and the CMB output pin. See the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5] for additional information about creating generated clocks.

Example

In the following figure, a create_clock constraint was defined on the MMCM instance pin CLKOUT0. This overrides the automatically derived clock created by Vivado and loses any relationship with the incoming clock.

To just rename the auto-derived clock, use the following constraint right after the master clock definition in your constraint files:

```
create_generated_clock -name clkName [get_pins clk_gen_i0/clk_core_i0/inst/mmcme3_adv_inst/CLKOUT0]
```
Appendix A: Timing Methodology Checks

Figure A-3: Invalid Primary Clock on Clock Modifying Block
TIMING-4: Invalid Primary Clock Redefinition on a Clock Tree

Invalid clock redefinition on a clock tree. The primary clock `<CLOCK_NAME>` is defined downstream of clock `<CLOCK_NAME>` and overrides its insertion delay and/or waveform definition.

**Description**

A primary clock must be defined on the source of the clock tree. For example, this would be the input port of the design. When a primary clock is defined downstream that overrides the incoming clock definition, timing analysis can become inaccurate because it ignores the insertion delay prior to the redefined primary clock source point, which prevents proper skew computation. It is not recommended as the consequence could be incorrect timing analysis which might lead to a failure in hardware.

**Resolution**

Remove the `create_clock` constraint on the downstream object and allow the propagation of the upstream clock or create a generated clock referencing the upstream primary clock.

**Example**

In the following figure, the primary clock was correctly defined on the top-level port `clk_pin_p`. However, a `create_clock` constraint was used to redefine the primary clock on the output of the `IBUFCTRL` output. This new clock will ignore all delays prior to the `IBUFCTRL`.

![Figure A-4: Invalid Primary Clock Redefinition on a Clock Tree](image-url)
TIMING-5: Invalid Waveform Redefinition on a Clock Tree

Invalid inverted waveform on a clock tree. The generated clock `<CLOCK_NAME>` is defined downstream of clock `<CLOCK_NAME>` and has an inverted waveform definition compare to the incoming clock.

**Description**

A generated clock should be defined in relation to the incoming clock. The DRC warning is reporting that the generated clock has an invalid definition, such as a different period, phase shift, or inversion compared to the incoming clock.

**Resolution**

Modify the `create_generated_clock` constraint to define a proper waveform definition that matches the incoming clock definition. For more details about creating a proper generated clock constraint, refer to the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 5].

**Example**

In the following figure, a `create_generated_clock` was created on the output of the LUT1 inverter, but the `-invert` switch was not applied.

![Invalid waveform redefinition on clock tree](image)

*Figure A-5: Invalid Waveform Redefinition on a Clock Tree*
TIMING-6: No Common Primary Clock Between Related Clocks

The clocks `<CLOCK_NAME1>` and `<CLOCK_NAME2>` are related (timed together) but they have no common primary clock. The design could fail in hardware even if timing is met. To find a timing path between these clocks, run the following command: `report_timing -from [get_clocks `<CLOCK_NAME1>`] -to [get_clocks `<CLOCK_NAME2>`].`

**Description**

The two clocks reported are considered related and timed as synchronous by default even if they are not derived from a common primary clock and do not have a known phase relationship. The DRC warning is reporting that the timing engine cannot guarantee that these clocks are synchronous.

**Resolution**

The resolution depends on whether the two clock domains are asynchronous or synchronous. In the case of the clocks being asynchronous, the paths between the two domains should be covered by a timing exception (such as `set_max_delay -datapath_only`, `set_clock_groups`, or `set_false_path`). The DRC will be resolved once all the paths between these two domains have full exception coverage.

**Example**

In the case of the clocks being synchronous, you can define one timing clock on both clock source objects if originally both clocks have the same waveform (see the first example below).

**Example 1:**
```
create_clock -period 10 -name clk1 [get_ports <clock-1-source> <clock-2-source>]
```

If the two clocks have different waveforms, you can define the first clock as a primary clock and the second clock as a generated clock, with the first clock specified as the master clock (see Example 2 below).

**Example 2:**
```
create_clock -period 10 -name clk1 [get_ports <clock-1-source>]
```

If the clocks are related, but have a clock period ratio of 2, the solution is to create a primary clock on the one source, and create a generated clock on the second source:
```
create_generated_clock -source [get_ports <clock-1-source>] -name clk2 -divide_by 2 [get_ports <clock-2-source>]
```
TIMING-7: No Common Node Between Related Clocks

The clocks <CLOCK_NAME1> and <CLOCK_NAME2> are related (timed together) but they have no common node. The design could fail in hardware. To find a timing path between these clocks, run the following command: report_timing -from [get_clocks <CLOCK_NAME1>] -to [get_clocks <CLOCK_NAME2>].

Description

The two clocks reported are considered related and timed as synchronous by default. The DRC warning is reporting that the timing engine cannot guarantee that these clocks are synchronous in hardware, since it could not determine a common node between the two clock trees.

Resolution

The resolution depends on whether the two clock domains are asynchronous or synchronous. In the case of the clocks being asynchronous, the paths between the two domains should be covered by a timing exception (such as set_max_delay -datapath_only, set_clock_groups, or set_false_path).

In the case of the clocks being synchronous, this DRC warning can be waived.

Example

In the following figure, a synchronous clock domain crossing (CDC) exists between the clk1 and clk2 domains. Both clk1 and clk2 are determined to be synchronous in Vivado by default. However, since clk1 and clk2 are input ports, there is no common node relationship between the two clocks. For this case, Vivado cannot guarantee that the two clocks are synchronous.
TIMING-8: No Common Period Between Related Clocks

The clocks `<CLOCK_NAME1>` and `<CLOCK_NAME2>` are found related (timed together) but have no common (expandable) period.

**Description**

The two clocks reported are considered related and timed as synchronous by default. However, the timing engine was unable to determine a common period after expanding the waveform of both clocks over 1000 cycles. In such a case, the worst setup relationship over these 1000 cycles is used for timing analysis. However, the timing engine cannot ensure this is the most pessimistic case. This typically occurs with clocks with an odd fractional period ratio.

**Resolution**

As the waveforms do not allow safe timing analysis between the two clocks, it is recommended to treat these clocks as asynchronous. Therefore, the paths between the two clock domains should be covered by a timing exception (such as `set_max_delay -datapath_only`, `set_false_path`, or `set_clock_groups`).
TIMING-9: Unknown CDC Logic

An asynchronous Clock Domain Crossing has been detected between clock <CLOCK_NAME1> and clock <CLOCK_NAME2> through a set_false_path or a set_clock_groups or a set_max_delay -datapath_only constraint but no safe CDC logic has been identified (crossing pin <PIN_NAME>).

Description

The purpose of the DRC is to ensure that inter-clock domains constrained with timing exceptions have been designed with safe asynchronous clock domain crossing circuitry. For more details on recognized safe topologies, see Report Clock Domain Crossings, page 69.

Resolution

The recommendation is to make the appropriate design to have a proper synchronization for the inter-clock paths. To do this, add, at minimum, a double-register logic synchronizer. In the case a FIFO or higher-level protocol is already defined on the path, this DRC can be safely ignored.

Example

In the following figure, an asynchronous clock domain exists between clk1 and clk2. However, the clk2 capture domain doesn't contain a double register logic synchronizer to synchronize the data.

![Figure A-7: Missing Synchronizer](X15526-111715)
TIMING-10: Missing Property on Synchronizer

A logic synchronizer with `<CELL_NAME1>` and `<CELL_NAME2>` has been detected between clock `<CLOCK_NAME1>` and clock `<CLOCK_NAME2>` but the synchronizer does not have the property `ASYNC_REG=TRUE` on both registers.

Description

Synchronizer registers must have their `ASYNC_REG` property set to `TRUE` in order to preserve the cells through any logic optimization during synthesis and implementation, and to optimize their placement for the best mean time between failure (MTBF) statistics.

Resolution

The solution is to add the `ASYNC_REG` constraint to each stage of the logic synchronizer. To find out more information on the `ASYNC_REG` constraint, refer to the *Vivado Design Suite Properties Reference Guide* (UG912) [Ref 10].

Example

In the following figure, an asynchronous clock domain exists between `clk1` and `clk2` and is properly synchronized with a double register logic synchronizer. However, each register of the synchronizer needs to have the `ASYNC_REG` property applied to increase the timing slack and lower MTBF.

![Missing double register logic synchronizer on the capture domain](image)

![Clock domain crossing](image)

*Figure A-8: Missing Property on Synchronizer*
TIMING-11: Inappropriate Max Delay with Datapath Only Option

A max delay constraint with -datapath_only has been applied between <PIN_NAME> and <PIN_NAME>. The startpoint(s) and endpoint(s) either belong to the same clock domain or belong to two clock domains that can safely be timed together. It is only recommended to use the -datapath_only option on paths between clocks that do not have a known phase relationship. This DRC is waived when a synchronizer is found on the path endpoint.

Description

The set_max_delay with the -datapath_only option is used to remove the clock skew from the setup slack computation and to ignore hold timing. The set_max_delay -datapath_only command is used to constrain asynchronous signals timing paths that: (1) do not have a clock relationship; but which (2) require maximum delay. It is not recommended to use this constraint on synchronous paths.

Resolution

The solution is to modify the set_max_delay -datapath_only constraint such that it does not cover synchronous timing paths. Refer to the startpoint and endpoint cells listed in the message to find the associated set_max_delay constraint.
TIMING-12: Clock Reconvergence Pessimism Removal Disabled

Description
The Clock Reconvergence Pessimism Removal (CRPR) mode has been disabled. It is not recommended to perform timing analysis in this mode as over-pessimistic clock tree delays could result in impossible timing closure.

The CRPR feature is used to remove artificially induced pessimism that is derived from the usage of the maximum and minimum delay along the common portion of the clock network. If the CRPR is disabled, it might be difficult to close timing.

Resolution
The recommendation is to enable the CRPR analysis to ensure the design has accurate timing information. The Tcl command to enable the CRPR analysis is `config_timing_pessimism -enable`.

TIMING-13: Timing Paths Ignored Due to Path Segmentation

Some timing paths are not reported due to path segmentation on pin(s) `<PIN_NAME>`. To prevent path segmentation, all the Min and Max delay constraints should be defined with a list of valid startpoints and endpoints.

Description
Path segmentation occurs when a timing path is broken into a smaller path to be timed. When max and min delay constraints are defined on pins that are invalid startpoints (and respectively, endpoints), the timing engine breaks the timing arcs going through the node so that the node becomes a valid startpoint (and respectively, endpoint). It is highly recommended to avoid path segmentation as it might have unexpected consequences. This might result in incorrect timing analysis and hardware failures.

Resolution
Avoid path segmentation whenever possible by carefully choosing valid startpoints and endpoints in the `set_max_delay` and `set_min_delay` constraints. For additional information on path segmentation and using the Min/Max delay constraints, refer to the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5].
TIMING-14: LUT on the Clock Tree

The LUT `<CELL_NAME>` has been found on the clock tree. It is not recommended to have LUT cells on the clock path.

Description

A LUT on the clock path might cause excess skew because the clock must be routed on general routing resources through the fabric. In addition to excess skew, these paths are more susceptible to PVT variations. It is highly recommended to avoid local clocks whenever possible.

Resolution

The solution is to change the design to remove the LUT located on the clock tree. Synthesis can create this situation in many cases such as clock gating and inversion. In the case of an inversion LUT1 cell, the LUT might be absorbed into the downstream SLICE after `opt_design`. Investigate the case to ensure that the situation is still valid after `opt_design` is complete.

Example

In the following figure, a LUT is used to gate the clock with a clock enable signal. The LUT on the path can cause excess skew, which is undesirable.

![LUT on the Clock Tree](X15530-111715)

*Figure A-9: LUT on the Clock Tree*
TIMING-15: Large Hold Violation on Inter-Clock Path

There is a large inter-clock skew of <VALUE> ns between <CELL_NAME> (clocked by <CLOCK_NAME>) and <CELL_NAME> (clocked by <CLOCK_NAME>) that results in large hold timing violation(s) of <VALUE> ns. Fixing large hold violations during routing might impact setup slack and result in more difficult timing closure.

Description

The DRC warning is reporting that the large hold violation due to the inter-clock skew will most likely be difficult to close timing during implementation. It is recommended to investigate the large inter-clock skew greater than 1.0 ns to ensure proper constraints or design topology.

Resolution

Investigate whether the large inter-clock skew on the timing path should be timed or is related to non-optimal timing constraints. If the large skew occurs due to an unconstrained CDC path, add the necessary timing exception. If the violation occurs due to a logic associated with the clock tree, investigate the topology of path for improvements to more easily close timing.
TIMING-16: Large Setup Violation

There is a large setup violation of <VALUE> ns between <CELL_NAME> (clocked by <CLOCK_NAME>) and <CELL_NAME> (clocked by <CLOCK_NAME>). Large setup violations at the end of those stages might be difficult to fix during the post-placement implementation flow and could be the result of non-optimal XDC constraints or non-optimal design architecture.

Description

This DRC warning reports setup violations that will most likely be difficult to close timing during implementation. It is recommended to investigate setup violations greater than 1.0 ns to ensure proper constraints or design topologies.

Resolution

Investigate whether the large setup violation is a timing path that should be timed or is related to non-optimal timing constraints. If the setup violation occurs due to an unconstrained CDC path, add the necessary timing exception. If the violation occurs due to a significant amount of combinational logic, investigate the topology of the path for improvements to more easily close timing.
TIMING-17: Non-Clocked Sequential Cell

The clock pin <PIN_NAME> is not reached by a timing clock.

Description

The DRC reports the list of sequential cells unconstrained by a timing clock which affect the resulting timing analysis for the reported cells. It is highly recommended that all clocks be properly defined in order to get the maximum timing path coverage with the best accuracy. The consequence could be missing timing analysis, which might lead to hardware failures.

Resolution

The resolution is to create the missing primary or generated clock on the clock tree driving the unconstrained sequential cells.

TIMING-18: Missing Input or Output Delay

An <INPUT/OUTPUT> delay is missing on <PORT_NAME> relative to clock(s) <CLOCK_NAME>.

Description

IO timing is in reference to a timing path that includes an external device. The input and output delays specify the paths delay of the ports relative to a clock edge at the interface of the design. It is highly recommended to add input/output delay constraints to ensure that the FPGA interface can meet the timing of the external devices.

Resolution

Add the required input and output delay constraints in correspondence with required board application.
TIMING-19: Inverted Generated Clock Waveform on ODDR

The waveform of the generated clock `<CLOCK_NAME>` is inverted compared to the waveform of the incoming clock `<CLOCK_NAME>`.

Description

A generated clock on a forwarded clock port should be defined in relation to the incoming clock. The DRC warning is reporting that the generated clock on the forwarding clock port has an invalid waveform, such as an inversion, compared to the incoming source clock. This might lead to hardware failures as the timing analysis of the ports associated with the forwarded clock do not match what happens on the device.

Resolution

Modify the `create_generated_clock` constraint to define a proper waveform that matches the incoming clock definition. For more details about creating a proper generated clock constraint, refer to the *Vivado Design Suite User Guide: Using Constraints* (UG903) [Ref 5].

TIMING-20: Non-Clocked Latch

The latch `<CELL_NAME>` cannot be properly analyzed because its control pin `<PIN_NAME>` is not reached by a timing clock.

Description

This DRC is reporting the list of latch cells not constrained by a timing clock which affect the resulting timing analysis. It is highly recommended that all clocks be properly defined in order to get the maximum timing path coverage with the best accuracy. The consequence could be incomplete timing analysis coverage, which might lead to hardware failures.

Resolution

The resolution is to create the primary or generated clock on the source of the clock tree driving the unconstrained control pins on the latch cells.
TIMING-21: Invalid COMPENSATION Property on MMCM

The MMCM <CELL_NAME> has an invalid COMPENSATION property value relative to the connection of its feedback loop. If the feedback loop goes outside the FPGA, the property should be set to EXTERNAL. If the feedback loop is internal to the FPGA, the property should be set to ZHOLD.

**Description**

MMCM compensation modes define how the MMCM feedback is configured for delay compensation of the output clocks. Depending on the MMCM use case, the feedback path should match a specific topology. This DRC warning is reporting that the topology of the MMCM use case doesn't match the COMPENSATION property value. This might lead to unintended behavior in hardware because the timing analysis does not match.

**Resolution**

The recommendation is to leave the default value of AUTO to the COMPENSATION property of the MMCM in the design. The Vivado Integrated Design Environment (IDE) will automatically select the appropriate compensation value based on the circuit topology. For additional information on the compensation property and the input delay compensation, refer to the Clocking Resources User Guide for your specific architecture.
TIMING-22: Missing External Delay on MMCM

The MMCM <CELL_NAME> has an external feedback loop but no external delay has been specified between FBOUT and FBIN. It is recommended to specify an external delay with set_external_delay between the two ports connected to the pins FBOUT and FBIN with an external feedback loop.

Description

The MMCM can be configured for external deskew where the feedback board trace matches the trace to the external components. The external delay value is used in the calculation of the MMCM compensation delay. This could lead to hardware failures, especially on the IO paths, because the timing analysis of the MMCM compensation does not match what happens on the device.

Resolution

Add a set_external_delay constraint between the external feedback input and output port for the defined external trace delay. For additional information on the set_external_delay command, refer to the Vivado Design Suite Tcl Command Reference Guide (UG835) [Ref 3].

Example

set_external_delay -from <output_port> -to <input_port> <external_delay_value>
Appendix A: Timing Methodology Checks

### TIMING-23: Combinatorial Loop Found

A timing loop has been detected on a combinational path. A timing arc has been disabled between `<CELL_NAME1>` and `<CELL_NAME2>` to break the timing loop.

**Description**

Combinatorial timing loops are created when the output of combinatorial logic is fed back to its input, resulting in a timing loop. This loop unnecessarily increases the number of cycles by infinitely going around the same path and cannot be timed. To resolve the timing loop, the Vivado IDE disables the timing arc on the cell in the loop.

**Resolution**

If you didn’t intend to create a combinatorial feedback loop, correct the issue by modifying the design source files (RTL). But because the timing loop is expected, use the `set_disable_timing` command to break the timing loop where it makes the most sense (usually the feedback path) instead of letting Vivado Timing break it at a random location.

### TIMING-24: Overridden Max Delay Datapath Only

A `set_clock_groups` or a `set_false_path` between clocks `<CLOCK_NAME1>` and `<CLOCK_NAME2>` overrides a `set_max_delay -datapath_only` (see constraint position `<#>` in the Timing Constraints window in the Vivado IDE). It is not recommended to override a `set_max_delay -datapath_only` constraint. Replace the `set_clock_groups` or `set_false_path` between clocks with point-to-point `set_false_path` constraints.

**Description**

The DRC warning only occurs when a `set_max_delay -datapath_only` constraint is overridden by a `set_clock_groups` or `set_false_path` constraint between clocks. If a point-to-point `set_false_path` overrides a `set_max_delay -datapath_only`, the DRC will not be reported.

**Resolution**

The solution is to replace the `set_clock_groups` or `set_false_path` between clocks with point-to-point false path constraints to avoid incorrectly overriding a `set_max_delay -datapath_only` constraint.
TIMING-25: Invalid Clock Waveform on Gigabit Transceiver (GT)

The waveform of the clock `<CLOCK_NAME>` defined on the transceiver output pin `<PIN_NAME>` or on the net connected to that pin is not consistent with the transceiver settings or the reference clock definition is missing. The auto-derived clock period is `<PERIOD>` and the user-defined clock period is `<PERIOD>`.

Description

For UltraScale™ devices, Vivado automatically derives clocks on the output of a GT based on the GT settings and the characteristics of the incoming master clock. For 7 series devices, Vivado does not automatically derive the GT clocks; it is your responsibility to create the appropriate primary clocks on the GT's output pins. The DRC warning is reporting that the user-defined clock does not match the expected auto-derived clock that Vivado would automatically create. This could lead to hardware failures as the timing constraints for the design do not match what happens on the device.

Resolution

If the user-defined generated clock is unnecessary, remove the constraint and use the auto-derived clock instead. If constraint is necessary, verify that the generated clock constraint matches the auto-derived clock waveform or modify the GT properties to match the expected clock waveform. If the intention is to force the name of the auto-derived clock, the recommendation is to use the `create_generated_clock` constraint with only the `-name` option defined and the name of the object where the clock is defined (typically output pin of GT). See the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5] for additional information about creating generated clocks and restrictions of the auto-derived clocks renaming constraint.
TIMING-26: Missing Clock on Gigabit Transceiver (GT)

The output clock pin <PIN_NAME> does not have clock defined. Create a primary clock on the <PORT_NAME> input port in order to let Vivado auto-derive the missing GT clocks.

Description

For UltraScale devices, Vivado automatically derives clocks on the output of a GT based on the GT settings and the characteristics of the incoming master clock. The DRC warning is reporting that Vivado is unable to auto-derive the output clock of the GT due to the missing primary clock on the input port. The consequence is that the downstream logic connected to the GT related clocks will not be timed.

Resolution

Create a primary clock on the recommended input port to the GT.

TIMING-27: Invalid Primary Clock on Hierarchical Pin

A primary clock <CLOCK_NAME> is created on an inappropriate internal pin <PIN_NAME>. It is not recommended to create a primary clock on a hierarchical pin when its driver pin has a fanout connected to multiple clock pins.

Description

If the driver is traversed by a clock and a new clock is defined downstream on a hierarchical pin, the cells downstream of the hierarchal pin will have different timing analysis compared to the cells on the fanout of the driver pin. If any synchronous paths exist between the driver clock and the hierarchical pin clock, skew will be inaccurate and timing signoff will be invalid. This situation can result in hardware failure.

Resolution

Remove the primary clock definition on the hierarchical pin, or if the downstream clock is absolutely needed, use a generated clock constraint with the driver clock specified as master clock instead.
TIMING-28: Auto-Derived Clock Referenced by a Timing Constraint

The auto-derived clock `<CLOCK_NAME>` is referenced by name inside timing constraint (see constraint position `<#>` in the Timing Constraint window in the Vivado IDE). It is recommended to reference an auto-derived clock by the pin name attached to the clock:

`get_clocks -of_objects [get_pins <PIN_NAME>]`.

Description

An auto-derived clock should be referenced by the source pin object. The auto-derived clock name might change during development due to modifications to the netlist or constraints. Referencing an auto-derived clock by name should be discouraged, because the consequence could be invalidated constraints in subsequent runs after the design has been modified.

Resolution

Modify the constraint to reference the auto-derived clock by the pin name attached to the clock using `get_clocks -of_objects [get_pins <PIN_NAME>]`. Alternatively, use the `create_generated_clock` constraint to force the name of the auto-derived clock. For more details about using a generated clock constraint to force a clock name, refer to the `Vivado Design Suite User Guide: Using Constraints` (UG903) [Ref 5].
TIMING-29: Inconsistent Pair of Multicycle Paths

Setup and hold multicycle path constraints should typically reference the same -start pair for SLOW-to-FAST synchronous clocks or -end pair for FAST-to-SLOW synchronous clocks (see constraint positions <#>, <#> in the Timing Constraint window in Vivado IDE).

Description

By default, the set_multicycle_path constraint is used to modify the path requirement multipliers with respect to the source clock for hold or the destination clock for setup. For certain use cases, the path requirement must be multiplied with respect to a specific clock edge.

Resolution

For both setup and hold, modify the set_multicycle_path constraints to reference the destination clock (-end) for SLOW-to-FAST synchronous clocks and the source clock (-start) for FAST-to-SLOW synchronous clocks. See the Vivado Design Suite User Guide: Using Constraints (UG903) [Ref 5] for additional information about properly setting multicycle paths between clocks.
TIMING-30: Sub-Optimal Master Source Pin Selection for Generated Clock

The generated clock `<CLOCK_NAME>` has a sub-optimal master source pin selection, timing can be pessimistic.

**Description**

A generated clock should reference the clock that is propagating in its direct fanin, although the `create_generated_clock` command lets you specify any reference clock. This DRC warning is reporting that the generated clock is associated to a master clock defined farther upstream than the incoming master clock. In this situation, timing analysis can be more pessimistic and apply additional clock uncertainty on the paths between the master clock and the generated clock. This can lead to slightly more difficult timing closure. It is recommended to associate the generated clock to the master clock source pin that the generated clock is derived.

**Resolution**

Modify the `create_generated_clock` constraint to reference the master clock source pin from which the generated clock is directly derived in the design.
Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Solution Centers

See the Xilinx Solution Centers for support on devices, software tools, and intellectual property at all stages of the design cycle. Topics include design assistance, advisories, and troubleshooting tips.

Documentation Navigator and Design Hubs

Xilinx Documentation Navigator provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open the Xilinx Documentation Navigator (DocNav):

- From the Vivado IDE, select Help > Documentation and Tutorials.
- On Windows, select Start > All Programs > Xilinx Design Tools > DocNav.
- At the Linux command prompt, enter docnav.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In the Xilinx Documentation Navigator, click the Design Hubs View tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on Documentation Navigator, see the Documentation Navigator page on the Xilinx website.
References

The following Xilinx® Vivado® Design Suite documents provide supplemental material useful with this guide.

9. 7 Series FPGAs Clocking Resources User Guide (UG472)
11. All Vivado Design Suite Documentation

Training Resources

Xilinx provides a variety of training courses and QuickTake videos to help you learn more about the concepts presented in this document. Use these links to explore related training resources:

2. Vivado Design Suite QuickTake Video: Using the Vivado Timing Constraint Wizard
3. Vivado Design Suite QuickTake Video: Advanced Clock Constraints and Analysis
4. Vivado Design Suite QuickTake Video: Analyzing Implementation Results
5. Vivado Design Suite QuickTake Video: Running Design Rule Checks (DRCs) in Vivado
6. Vivado Design Suite QuickTake Video: Timing Analysis Controls
8. Vivado Design Suite QuickTake Video: Cross Clock Domain Checking - CDC Analysis
9. Vivado Design Suite QuickTake Video: Design Analysis and Floorplanning with Vivado
10. Vivado Design Suite QuickTake Video Tutorials

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