**INTRODUCTION**

The UltraFast™ Design Methodology is a set of best practices recommended by Xilinx to maximize productivity and reduce design iterations of complex systems, including embedded processor subsystems, analog and digital processing, high-speed connectivity, and network processing. See the [UltraFast Design Methodology Guide for the Vivado Design Suite (UG949)](https://www.xilinx.com/support/documentation/ug1231.pdf) for more information.

The UltraFast Design Methodology Checklist (KTP301) includes common questions that highlight typical areas where design decisions have downstream consequences and draws attention to potential problems that are often unknown or ignored. It provides easy access to related collateral. The checklist is available within the Xilinx Documentation Navigator tool (DocNav).

This quick reference guide highlights key design methodology steps to achieve quicker system integration and design implementation and to derive the greatest value from Xilinx® devices and tools. Pointers to related collateral are also provided. The main design tasks covered in this guide include:

- Board and Device Planning
- Design Entry and Implementation
- Top-Level Design Validation
- Design Analysis
- Design Closure

Refer to the UltraFast Design Methodology – System-Level Design Flow available within the Xilinx Documentation Navigator tool (DocNav) for pointers to all design hubs and specific collateral.

---

### PCB Designer

<table>
<thead>
<tr>
<th>PCB Designer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Examine Key Interfaces</strong></td>
</tr>
<tr>
<td>• Validate part orientation and key interfaces</td>
</tr>
<tr>
<td><strong>Examine the PCB Layout</strong></td>
</tr>
<tr>
<td>• Perform the Memory Interface and Transceiver Checklists</td>
</tr>
<tr>
<td>• Follow PCB layout recommendations</td>
</tr>
<tr>
<td>• Ensure final FPGA pinout is signed off by FPGA designer</td>
</tr>
<tr>
<td><strong>Review the Schematic</strong></td>
</tr>
<tr>
<td>• Complete PCB Checklist review</td>
</tr>
<tr>
<td>• Check PDS, configuration, and power supplies</td>
</tr>
<tr>
<td>• Validate I/O state before, during, and after configuration</td>
</tr>
<tr>
<td><strong>Manufacture and Test</strong></td>
</tr>
<tr>
<td>• Verify the configuration sequence, power supplies, and I/O performance with the test I/O project</td>
</tr>
</tbody>
</table>

### FPGA Designer

<table>
<thead>
<tr>
<th>FPGA Designer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Analyze Device for Pinout</strong></td>
</tr>
<tr>
<td>• Examine transceiver and bonded I/O locations</td>
</tr>
<tr>
<td>• Examine SSI technology I/O planning</td>
</tr>
<tr>
<td>• Validate part orientation and key interfaces</td>
</tr>
<tr>
<td><strong>Define I/O Pinouts for Key Interfaces</strong></td>
</tr>
<tr>
<td>• Create I/O planning projects</td>
</tr>
<tr>
<td>• Define and validate memory controllers, GTS, and PCI Express® technology locations</td>
</tr>
<tr>
<td>• Establish a clocking skeleton</td>
</tr>
<tr>
<td>• Minimize floorplan distance between connected IP</td>
</tr>
<tr>
<td><strong>Define Final Pinout</strong></td>
</tr>
<tr>
<td>• Merge interface projects into a final I/O project</td>
</tr>
<tr>
<td>• Validate DRCs and SSN analysis</td>
</tr>
<tr>
<td>• Implement design to check clocking and I/O rules</td>
</tr>
<tr>
<td>• Use the final I/O project for production test</td>
</tr>
</tbody>
</table>

### Design Entry and Implementation

<table>
<thead>
<tr>
<th>Logic Designer</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Define a Good Design Hierarchy</strong></td>
</tr>
<tr>
<td>• Define relevant hierarchies to help global placement and floorplanning</td>
</tr>
<tr>
<td>• Insert I/O and clock components near the top level</td>
</tr>
<tr>
<td>• Add registers at main hierarchical boundaries</td>
</tr>
<tr>
<td>• Generate IP and review target device utilization</td>
</tr>
<tr>
<td><strong>Build and Validate RTL Submodules</strong></td>
</tr>
<tr>
<td>• Ensure design adheres to RTL coding guidelines</td>
</tr>
<tr>
<td>• Add sufficient registers around DSP and memories</td>
</tr>
<tr>
<td>• Use control signals only when absolutely necessary</td>
</tr>
<tr>
<td>• Use synthesis attributes to control final logic mapping</td>
</tr>
<tr>
<td>• Create simple timing constraints to review estimated timing and address paths with too many logic levels</td>
</tr>
<tr>
<td>• Review synthesis log files, utilization report, and elaborated view to identify sub-optimal mapping</td>
</tr>
<tr>
<td>• Run Methodology and RTL checks and review issues</td>
</tr>
<tr>
<td>• Implement the submodule in out-of-context (OOC) mode to validate implemented performance</td>
</tr>
<tr>
<td>• Review utilization and power against original budget</td>
</tr>
<tr>
<td>• Simulate the design to validate functionality</td>
</tr>
</tbody>
</table>

### Board and Device Planning

See Also:
- [UG949: Board and Device Planning PCB Design Checklist](https://www.xilinx.com/support/documentation/ug949.html)
- [Memory Interface IP Design Checklists](https://www.xilinx.com/support/documentation/ug1231.html)
- [Schematic Design Checklists](https://www.xilinx.com/support/documentation/ug1231.html)

### Design Entry and Implementation

See Also:
- [UG949: Design Creation and Implementation](https://www.xilinx.com/support/documentation/ug949.html)
- [Designing with IP Design Hub](https://www.xilinx.com/support/documentation/ug949.html)
- [Using IP Integrator Design Hub](https://www.xilinx.com/support/documentation/ug949.html)
- [Logic Synthesis Design Hub](https://www.xilinx.com/support/documentation/ug949.html)
- [Applying Design Constraints Design Hub](https://www.xilinx.com/support/documentation/ug949.html)
- [Implementation Design Hub](https://www.xilinx.com/support/documentation/ug949.html)
TOP-LEVEL CONSTRAINTS VALIDATION

**Baseline the Design**
- Validate timing closure feasibility early in the design process after most blocks and key IP are available
- Specify essential constraints only:
  - Use all IP constraints
  - Define realistic primary and generated clocks
  - Define all clock domain crossing constraints
  - Add multiphase paths where required
  - Do not use I/O constraints at this stage
  - Ensure path requirements are reasonable
- Validate WNS = 0.0 ns using report_timing_summary at each stage of the flow:
  - After synthesis
  - Before placement
  - Before and after routing
- Address timing violations early in the flow
- Fix GoI issues in RTL and synthesis for the biggest impact

**Validate Timing Constraints**
- Run report_timing_summary or check_timing to ensure all clocks are defined and all registers, input ports, and output ports are constrained
- Run report_methodology and address all TIMING* and XDC* issues
- Run report_clock_interaction to ensure each clock pair is safely timed with reasonable path requirements
- Run report_cdc to verify all asynchronous clock domain crossing paths are properly constrained and use safe synchronization circuitry
- Run report_exceptions to identify timing exceptions that overlap, are ignored, or are inefficient
- Ensure all Critical Warnings are resolved when the design is loaded and constraints are applied

---

**Design Analysis and Closure**

**Identify Timing Violation Root Causes**
- Try report_gsr_suggestions for automated analysis and timing closure recommendations
- Use report_timing_summary or report_design_analysis to find the root cause
- For setup paths, check for high datapath delay due to:
  - Large cell delay (7 series > 25%, UltraScale devices > 50%)
  - Large net delay (7 series > 75%, UltraScale devices > 50%)
- For hold paths, check for hold requirement > 0 ns
- Check for high clock skew (> 500 ps), high clock uncertainty (> 200 ps), or logical issues

**Reduce Logic Delay**
- Modify RTL to use parallel or efficient operators
- Add pipeline registers and use synthesis retiming
- Add registers on DSP or block RAM outputs
- Pull registers out of the SRL on the SRL input, output, or both
- Remove KEEP/DONT_TOUCH/MARK_DEBUG to allow all optimizations

**Reduce Net Delay**
- Review and adjust floorplan constraints
- Optimize high fanout nets
- Address congestion if level > 4 is reported in:
  - report_design_analysis placer congestion table
  - initial estimated router congestion in log file

**Reduce Clock Skew**
- Use parallel buffers instead of cascaded buffers
- Use CLOCK_DELAY_GROUP between synchronous clocks originating from the same input or PLL
- Add timing exceptions between asynchronous clocks

**Reduce Clock Uncertainty**
- Optimize MMCM settings
- Divide clocks with BUFGCE_DIV in UltraScale™ devices

---

**Reduce Control Sets**
- Avoid MAX_FANOUT on control signals
- Increase synthesis control set threshold
- Merge equivalent control signals with opt_design

**Optimize High Fanout Nets**
- Use hierarchy-based register replication in RTL
- Use opt_design -hier_fanout_limit and place_design -fanout_opt for replication
- Promote to global clocking if not critical
- Force replication with phys_opt_design

**Address Congestion**
- Lower device utilization and balance SLR utilization
- Try placer directives AltSpreadLogic* or SSI_Spread*
- Identify congested modules with report_design_analysis -complexity -congestion
- For congested modules, try the AlternateRouting block-level synthesis strategy or reduce MUXF*/CARRY* with opt_design
- Use global clocking for high fanout nets in congested regions
- Reuse DSP and block RAM placement from previous implementations with low congestion

**Tune the Compilation Flow**
- Try several place_design directives
- Use block-level synthesis strategies for an optimal netlist
- Overconstrain critical clocks during placement and physical optimization with net_clock_uncertainty
- Use incremental compile after minor design modifications to preserve QoR and improve runtime

**Analyze and Optimize Power**
- Constrain activity, environment, and process
- Try power_opt to reduce power consumption
- Maximize use of block RAM cascading

---

See Also:
- UG949: Design Closure
- Implementing and Design Closure
- UG949: Implementation and Design Closure
- Analyzing and Resolving Timing Violations
- Applying Common Timing Closure Techniques
- Implementation Design Hub
- Timing Closure and Design Analysis Design Hub

---

SeeAlso:
- UG949: Design Closure
- Understanding Timing Reports
- Identifying Timing Violations Root Cause
- UG949: Baseline The Design
- Timing Closure and Design Analysis Design Hub