What’s New in PlanAhead Software 13.1

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/01/2011	13.1	Initial release for 13.1 PlanAhead software.
03/23/2011	13.1	Fixed broken links.

Table of Contents

What's New in PlanAhead Software 13.1

This document provides an overview of the PlanAhead™ software 13 release. See the related chapters in the *PlanAhead User Guide (UG632),* for more information.

ISE Simulator Integration

PlanAhead release 13 has integrated the Xilinx® ISE Simulator (ISim) into the design flow. This new integration enables development and verification of designs completely within the PlanAhead user interface. PlanAhead now has support for simulation-only sources added to the project, which is performed either in the new project wizard or in the add sources dialog. The Flow Navigator provides access to ISE Simulator.

You can invoke ISim:

- After RTL Design for behavioral simulation
- After Implementation for timing simulation

Hierarchical Design Methodology Support

PlanAhead release 13 supports the Hierarchical Design features as described in the following subsections.

- Incremental XST flow in RTL projects
- Importing a partition into a different hierarchy than the one in which the partition was created
- AREA_GROUPS within partitions
- Black box support in Synthesis and Implementation
- Boundary optimization for constants and unconnected inputs and outputs on partition ports
- Defining partitions for Design Preservation in Netlist-based projects

Team-Based Design Support

PlanAhead 13 adds support for new team-based design methodology. Team based design supports multiple engineers implementing at a module level within a design to work in parallel. The flow then supports assembling the module level runs by a team leader at the top level with support for preservation levels to control the placement and routing information that is kept during import.

See the *Hierarchical Design Methodology Guide (UG748)* and Chapter 13, Hierarchical Design Techniques, in the *PlanAhead User Guide (UG632)* for more information.

Design Preservation RTL Support

PlanAhead 13 enhances support for design preservation flows by adding incremental compilation for RTL synthesis of partitions with XST. The design preservation flow allows a designer to mark portions of a design to be preserved in subsequent iterations and enabled incremental compilation. In prior releases, design preservation was only supported post synthesis. RTL-level control was added to provide designers an easier to use flow to control partitions throughout the design flow from synthesis through implementation within the PlanAhead user interface.

See the *Hierarchical Design Methodology Guide (UG748)* and Chapter 13, Hierarchical Design Techniques, in the *PlanAhead User Guide (UG632)* for more information.

Partial Reconfiguration Support

PlanAhead provides an interface to Partial Reconfiguration with appropriate licensing.

See the *Partial Reconfiguration User Guide (UG702)*, for more information.

Project Navigator Project File (.xise) Support

The New Project wizard lets you specify an ISE project file without requiring the specification of all project sources. The PlanAhead software:

- Parses the XISE project file
- Adds RTL and simulation sources, including CORE Generator™ cores and Block Memory Model (BMM) file

PlanAhead can now also determine relevant run options for Synthesis and Implementation tools and can configure the default run to match based on settings in the XISE project file.

New and Modified Project Management Features

The following subsections describe the new and modified features in PlanAhead 13 projects. In PlanAhead 13, you can:

- Import sources from Project Navigator
- Order source files automatically or manually for proper compilation by XST
- Discover the top-module name automatically
- Support 'include statements inside HDL more robustly
- Support Xilinx Synsthesis Technology (XST) XCF constraint files
- Identify unused source files
- Launch Runs without copying sources to the Run directory
- Archive projects
- Customize the Text Editor font

Graphical User Interface Enhancements

The PlanAhead software for release 13 has further enhanced the "layered complexity" of the Graphical User Interface (GUI) to provide an intuitive environment for both new and advanced users.

The left-side panel of the interface is a "Flow Navigator," which exposes a push-button flow from Project Management, through RTL Design, Netlist Design, Implemented Design, to Device Programming and Debugging. The new integration with ISim provides timing and behavioral simulation, which are exposed where appropriate for use in the Flow Navigator menu options. A new information window and an enhanced Tcl Console and Messaging window are also available.

The following subsections describe the new features and enhancements in the PlanAhead software release 13 in the ISE® Design Suite.

Main Menu Enhancements

Workspace Views

The PlanAhead workspace views are redesigned with an auto-fit selection. A dropdown in the Main toolbar lets you select applicable views for the open Project. The workspace views now contain dock/undock, float, minimize/maximize, and restore buttons.

Search Option

PlanAhead has added a search text box on the main menu to search through all the menu options for the specified text.

Export Options

A new option in the PlanAhead **File >Export > Export IBIS Model** is available in an open design. The Input/Output Buffer Information Specification (IBIS) is used analyze the design. The IBIS model exported from PlanAhead is compliant with the IBIS version 4.2, and uses the defaults of that specification.

Single Click Implementation

PlanAhead now allows you to click on the Implementation button in the flow navigator and the tool will launch a dialog prompting if you want to launch synthesis first if you have an RTL project, and the synthesis run is out of date. This allows you to do a "single-click" implementation of RTL. This feature requires that you have PlanAhead in GUI mode: if you close the project, only the currently running Synthesis run completes: the Implementation run does not launch.

Source View Enhancements

The PlanAhead release 13 provides enhanced views for source file structures and editing.

Third Party Text Editor Support

PlanAhead now allows the ability to use third party editors for editing source code files.

Message Manager

A new Messages view consolidates error, critical warning, warning, and informational messages from PlanAhead and ISE point tools into a single view. Messages are linked to the source code to allow for quick exploration and resolution of any errors or warnings.

Netlist View Additions and Modifications

The following subsections describe the additions and modifications to the PlanAhead Netlist view.

Clocking Resource View

The new Clocking Resource view available in the PlanAhead GUI aids in the visualization and assignment of clocking-related sites and physical resources within the FPGA.

Folders for Component Switching Limits

There are new folders in the timing results view imported from TRACE that better organize the component pin switching limit violations with setup and hold violations. The violations are sorted and the worst violation is displayed first within a constraint.

Enhanced Slack Histogram Report

PlanAhead release 13 contains an improved slack histogram feature which creates a graphical bar chart corresponding to collections of paths within ranges from most negative to most positive.

Device View Enhancements

PlanAhead Release 13 contains the following enhancements.

Device Resource Details

The Device view in PlanAhead has been enhanced to provide more detail for device resources such as pins on slices and BEL-level pins for Virtex®-6 and Virtex-7 devices, and the Timing Path provides annotation on pins upon full placement.

Multiple Instance Drag and Drop

PlanAhead now allows moving multiple instances in the device view at the same time. This allows users to move instances that are already placed in a group and all location constraints are translated together.

Schematic View Enhancements

PlanAhead supports tracing logic between two selected objects in the schematic view. Any two objects can be selected, and the PlanAhead software will trace and draw any intermediate logic connections between them within a schematic.

XPA Integration

PlanAhead Release 13 has added the ability to launch Xilinx Power Analyzer (XPA) to analyze power on implemented designs. To launch XPA click the XPower Analyzer icon after opening an implemented design.

RTL Design Additions and Modifications

Text Editor Options

PlanAhead release 13 allows for customization of fonts for comments, and keywords, supports integration of third party text editors, and allows for easier use of Xilinx Language Templates. See *PlanAhead User Guide (UG632)*, Chapter 5, RTL Design.

IP Catalog

The PlanAhead release 13 enhancements in the IP Catalog are:

- The CORE Generator™ IP catalog now supports migration of older superseded cores to the currently supported version.
- PlanAhead now supports canceling IP generation tasks that block other operations in the GUI.

Source File Exploration

PlanAhead can determine the top-module in an RTL design automatically, or give you the ability to define it manually.

You can reorder source files, either automatically or manually, for compilation and synthesis, and automatically or manually enable or disable RTL source files as required by the top-level module.

Power Estimation Enhancements

PlanAhead release 13 has Power Estimation available on Virtex-5, Virtex-6, and Spartan®-6 device families.

Partitions Control

PlanAhead release 13 provides control of partitions at the RTL level in synthesis with XST.

Additional ChipScope Features

The PlanAhead software release 13 added the ability within the ChipScope™ Pro Debug Analyzer to tag RTL nets using a new HDL Debug Probe feature that supports the following HDL debug flows:

- PlanAhead and Xilinx Synthesis Technology (XST)
- PlanAhead and Synplify and Synplify Pro from Synopsys®, Inc.
- PlanAhead and Precision RTL Synthesis from Mentor® Graphics, Inc.

See Chapter 12, Programming and Debugging the Design, in the *PlanAhead User Guide (UG632).*

Pin Planning Changes

The following subsections describe the PlanAhead 13 changes to the Pin Planning features.

Package View Legend and Spreadsheet Manipulation

A new legend to the Device and Package view allows you to view or hide specific layers and objects, and provides a legend for layer colors and pin shapes.

The spreadsheet-like Package Pins view can be edited, sorted, flattened, and filtered for better visibility on multifunction pins.

Alternate Part Definition

PlanAhead release 13 has the ability to define alternative parts to a design (for Virtex-5, Virtex-6, and Spartan-6 devices only). Some restrictions apply to Spartan-6 LX25 and LX25T devices, which is detailed in:

http://www.xilinx.com/support/answers/34885.htm.

New Pin Assignment and Banking Rules

The new pin assignment and banking rules are documented in Appendix B, DRCs, of the *PlanAhead User Guide (UG632)*, and include VCCaux reporting for Virtex-6 and newer devices.

Write I/O STANDARDs to Exported UCF

PlanAhead now has the option to write out all I/O STANDARD constraints to an exported UCF file with the **File > Export > Export I/O Ports** command.

New and Modified Design Rule Checks

The following is a list of the new and modified Design Rule Check (DRCs) in PlanAhead release 13.

Attribute DRCs

- AVAL—Checks for invalid attribute values on Netlist instances.
- ADEF—Checks for undefined attribute values on Netlist instances.

Bank DCI Cascade DRC

- DCICIOSTD—Checks that the DCI Cascade constraint is legal.

Bank I/O Standard DRC

- VCCAUX2—Warns of any requirements on LVPECL_33 and TMDS_33.

ChipScope DRCs

- CSUC—Checks for unconnected channels on ILA cores.
- CSCL—Checks for non-clock nets that are clocking the capture of probed nets.
- CSBR—Checks if device block RAM resources exceeded.

DSP48 DRCs

- DPCA—Checks the DSP48 cascade to ensure it is feasible based on Netlist connectivity.
- DPREG—Checks for DSP48 asynchronous feedback.

FIFO DRC

- FSYN—Checks for synchronous FIFO.

IOB DRC

- IOPCSLR—Checks for part compatibility between monolithic and multi-die devices.

Placer DRCs

- PLCR—Checks that the number of global clocks in a region is less than the value allowed by the device.
  PLCK—Checks all clock placement rules run during the placer.
- PLDL—Placement constraint for I/Os that checks whether all I/O are locked and whether all members of a bus are locked.
- PLVP—Checks for non-place-able instances due to resource conflicts or limitations.

RAMB DRC

- RAMB—Checks for clock restrictions for `READ_FIRST` mode.

Required Pin DRC

- REQP—Checks for required pins that are not connected on instances in the netlist.

Implementation Enhancements

PlanAhead 13 contains the following Implementation enhancements:

- Ease of file ordering for Implementation Runs.
- Ability to store Run-specific constraints in a specified UCF file.
  Once you implement a design, PlanAhead automatically loads/stores the constraints from that Run in a run-specific UCF.

Reference Documents

This document references the following web locations and documents:

PlanAhead release 13 capabilities are further described in following new documents:

- ***PlanAhead Tcl Command Reference**, (UG789)*

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ug789_tcl_commands.pdf

- ***Power Methodology Guide**, (UG786)*

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/ug786_PowerMethodology.pdf

The following documentation is available for PlanAhead Release 13:

- ***ISE Design Suite: Installation and Licensing Guide** (UG798)*:

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/iil.pdf

- ***ISE Design Suite 13: Release Note Guide** (UG631)*:

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/irn.pdf

- ***ISim User Guide** (UG660)*:

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/plugin_ism.pdf

- ***PlanAhead User Guide*** (UG632):

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/PlanAhead_UserGuide.pdf

- ***Floorplanning Methodology Guide** (UG633)*

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/Floorplanning_Methodology_Guide.pdf

- ***Hierarchical Design Methodology Guide** (UG748)*

  http://www.xilinx.com/support/documentation/sw_manuals/xilinx13_1/Hierarchical_Design_Methodology_Guide.pdf

- ***Partial Reconfiguration User Guide** (UG702):*

  http://www.xilinx.com/tools/partial-reconfiguration.htm

PlanAhead Tutorials are available at:

http://www.xilinx.com/support/documentation/dt_planahead_planahead13-1_tutorials.htm

User licenses are available at:
http://www.xilinx.com/getproduct.htm

Known Issues

A list of known issues is compiled in the Answer Record (AR) link at:

http://www.xilinx.com/support/answers/40512.htm