ISE Design Suite 10.1 Install Release Notes Known Issues

XTP026 (v1.1) March 24, 2008

The ISE Design Suite 10.1 Release Notes and Installation Guide found at the following URL contains installation instructions, system requirements, and other general information about ISE Design Suite 10.1:

http://toolbox.xilinx.com/docsan/xilinx10/books/docs/irn/irn.pdf (English)

http://toolbox.xilinx.com/docsan/xilinx10j/books/docs/irn/irn.pdf (Japanese)

This Known Issues document is a supplement to the Release Notes and Installation Guide and contains links to Answer Records that contain information on known issues in the ISE Design Suite. Xilinx Technical Support recommends that you apply the first service pack, to be released in late April 2008, as soon as it is available to avoid many of these Known Issues.

For IP-specific release note information related to IP Core Updates shipped in the ISE Design Suite 10.1 software release, as well as updates shipped in earlier ISE releases, refer to the IP Release Notes Guide at the following URL: http://www.xilinx.com/support/documentation/user_guides/xtp025.pdf

ISE General

30356	10.1 xilperl - "error while loading shared libraries: libdb-4.1.so" on Suse Linux Enterprise 10 64-bit
30372	10.1 Install - 32-bit cable drivers do not work on a 64-bit operating system
30374	10.1 Schematic - RAMB36 initial values are all set to zero; behavioral simulation fails
30376	10.1 ISE - "ERROR:ProjectMgmt:387 - TOE: ITclInterp::ExecuteCmd gave Tcl result..."
30382	Install - System experiences kernel panic when installing cable drivers on Linux
30383	10.1 Install - Issues when installing both Standalone Programming Tools and ISE
30384	ISE - Conflict in /usr/lib64/kde3/plugins/styles/, Plugin uses incompatible Qt library
30385	10.1 ISE Install - An install that utilized "setXenv.bat" does not allow updates
30386	10.1 Install - Canceling a WebInstall causes a segmentation fault
30387	10.1 Install - Select Installation Options (Environment Variables) is not displayed
30481	10.1 ISE - What is SecureIp and when is it supported?

ChipScope Pro

30223 10.1 ChipScope Pro - Release Notes and Known Issues

Constraints

30065 10.1 Constraint Editor - Comment line does not work correctly

30357 10.1 Constraints Editor/Floorplan Editor - Launching Floorplan Editor after Constraints Editor is Up causes Project Navigator to crash, "ConstraintSystem:151"

30363 10.1 Constraints System - Segmentation fault when converting from 9.2i to 10.1

30364 10.1 Constraints Editor - Unable to create constraints for EDIF project

30365 10.1 Constraint Editor - Comment line does not work correctly

30367 10.1 Constraints Editor - DDR OFFSET IN/OUT Wizard uses FALLING keyword for both rising and falling edge elements, and the pad timegrp name includes extra letters

30370 10.1 Constraints Editor - OFFSET IN (Clock to Setup Wizard does not provide "ns" as valid values

30369 10.1 Constraints System - Lack of error numbers and UCF line numbers for constraint syntax issues

CORE Generator

30196 10.1 CORE Generator - “ERROR:sim - NgdBuild:15 - Missing "-p" option and no target architecture available!"

30291 10.1 CORE Generator - Known Issues for CORE Generator 10.1

EDK

29852 10.1 EDK, MPMC v4.00.a - Memory details in MPMC GUI are not updating on CUSTOM part choice

30132 10.1 EDK, MPMC v4.00.a - mpmc_ecc_example.c:318: error: InterruptController undeclared

30133 10.1 EDK, MPMC v4.00.a - NPI PIM_RdFifo_Empty signal incorrectly goes Low when PIM_RdFifo_Flush is asserted

30194 10.1 EDK - "WARNING:MDT - This flow has been removed from the tools. Please update your scripts to remove this command"

30216 10.1 EDK - Why is it that XMD cannot connect to the FPU in my PPC design?

30224 10.1 EDK - "ncvhdl_p: *W,DLCILIB: Library name 'xilinxcorelib' not found, defaulting to 'XilinxCoreLib'. Please see nchelp on this error."

30225 10.1 EDK - libgen gives me errors in _profile_timer_hw.c when I try to profile for the PPC440

30274 10.1 EDK - Downloading a VxWorks image for PPC440 does not work

30292 10.1 EDK - "ERROR:MDT - IPNAME:xps_iic HW_VER:1.00.a - Can not find valid MPD..."

30298 10.1 EDK - After running compedklib to create simulation libraries for NCSim, I cannot run simulations

30299 10.1 EDK - Can I use CSUM offload with the xps_ll_fifo?

30303 10.1 EDK - How do I upgrade MicroBlaze from v7.00 to v7.10 in EDK?

30334 10.1 EDK, MPMC v4.00.a - Cannot find MIG /mig21/user_design/rtl/mig21.v for Virtex-5 DDR2 design

30381 10.1 EDK Install - settings32.sh and settings32.csh created even when no 32-bit applications exist on Linux 64-bit

Floorplanning

30278 10.1 Floorplanner - S3AN200 FT256 pin locations shown incorrectly in Floorplan View

30285 10.1 Floorplan Editor - Cannot delete constraints in New Source Wizard

30359 10.1 Floorplanner/Automotive Spartan-3A - Unable to view place BRAM

30360 10.1 Floorplanner - Crashes when the cursor is placed over an assigned pin

30361 10.1 Floorplan Editor - Unable to change the I/OStandard

30366 10.1 Floorplan Editor - Unable to see all Vref pins and right side I/O pins for Spartan-3, Spartan-3A,Spartan-3AN, and Spartan-3A DSP devices

30371 10.1 Floorplan Editor - Area Group ranges are written incorrectly

iMPACT

30307 10.1 iMPACT - Release Notes and Known Issues

IP

29767 10.1 IP Update #0 - Release Notes and Known Issues for CORE Generator ISE 10.1 IP Update 0 (10_IP0)

ISim

30331 10.1 ISim - ISE Simulator Known Issues

30332 10.1 ISim (ISE Simulator) - "FATAL_ERROR:Simulator:Fuse.cpp:419:$Id: Fuse.cpp.v"

MAP

30064 10.1 MAP - "FATAL_ERROR:MapLib:basmmtswrap.c:79:1.25- Failed to build TS database: 1 error(s)"

30112 10.1 MAP - Net SAVE property behavior has changed and may lead to DRC failures

30404 10.1 MAP/PAR - Placement phases do not produce same results on different OS platforms

NGDBuild

30333 10.1 NGDBUILD - Problems with constraint precedence

PACE

30362 10.1 PACE - Unable to load Spartan-2 or Spartan-3 device with -4Q speed grade

PAR

30355 10.1 PAR - Overview of new behavior where XIL_PLACE_ALLOW_LOCAL_BUFG_ROUTING variable is replaced by the CLOCK_DEDICATED_ROUTE constraint

PlanAhead

30513 10.1 PlanAhead - Can not launch PlanAhead on Linux

Project Navigator

30290 10.1 ISE - Known Issues for Project Navigator 10.1

30368 10.1 Project Navigator - Creating a new I/O pin assignment with the New Source Wizard causes a crash

30375 10.1 ISE - When opening PinAhead, error occurs: "FATAL_ERROR:GuiUtilities:Gq_Application.c:590:1.20 .."

Synthesis

30273 Synplify - Does Synplify support the use of unimacros in ISE 10.1?

30477 10.1 XST - "ERROR:MapLib:979 - LUT2 symbol <instance name> has an equation that uses input pin I1"

State Diagram Editor

12053 10.1 State Diagram Editor - The state diagram (.dia) cannot be saved without Administrator privileges in Windows 2000/NT

15589 10.1 State Diagram Editor - State Assignments variables set to "Node" cause synthesis errors such as "ERROR: HDLParsers:3312 - Undefined symbol 'state0'"

16616 10.1 State Diagram Editor - Blocking/Non-blocking statements are not used optimally in Verilog State Machine code

System Generator

17966 System Generator for DSP - Which versions of System Generator for DSP are compatible with which versions of ISE and MATLAB? Which versions of MATLAB and other dependent tools are supported by each release of System Generator?

23614 System Generator for DSP - Why does my design fail to generate when using a FIFO block, From FIFO block, or To FIFO block, in my design, and when my target path is more than 160 characters?

29595 System Generator for DSP - Release Notes and Known Issues

30282 10.1.00 System Generator for DSP - Release Notes/README and Known Issues List

30297 10.1.00 System Generator for DSP Installer - Why do I receive the message "An error occurred while installing the Microsoft Network Monitor driver (NetMon) during installation of WinPcap?"

30308 10.1.00, System Generator for DSP - My simulation does not use the automatically generated Verilog testbench and stimulus files. Why?

30310 10.1.00 - System Generator for DSP - Why do I get "Error 0001: Multiple Clock Support Design Rule Check Failed" when I select DCM for my "Multirate implementation" in my model containing a FIR Compiler block?

30312 10.1.00 - System Generator for DSP - I am able to generate my model using the DCM option for "Multirate Implementation" despite having blocks in my design that are listed as unsupported for the DCM

30313 10.1.00, System Generator for DSP - Why do I receive the message "MATLAB is not installed" when I try to launch my System Generator project from ISE?

30316 10.1.00 - System Generator for DSP - Why do I get mismatches in my post-translate, post-map, or post-par simulation if I use the DCM for my "Multirate Implementation"?

30317 10.1.00 - System Generator for DSP - If my design does not use the full rate system clock and the DCM option is used for "Multirate Implementation," I get mismatches in my behavioral simulation

30512 10.1.00 System Generator for DSP - When I try to run System Generator for DSP, TrendMicro's virus scanner flags "PPEthernetCosimEngine.dll" as a virus

Text Editor

30321 10.1 ISE Text Editor - Asian language characters in ISE Text Editor might appear corrupted when a file is closed and reopened

Timing

29382 10.1 Timing Analyzer - "FATAL_ERROR:GuiUtilites:WinApp.c:710:$Revision - This application has discovered an exceptional condition from which it cannot recover"

30017 10.1 Floorplan Editor/Timing Analyzer Crossprobing - The Clock and Data Paths for an OFFSET constraint do not connect

30033 10.1 Timing Analyzer Crossprobing - Extra connections shown through RAM during crossprobe to schematic

30335 10.1 Timing Analyzer/ Constraints Editor/Floorplan Editor/PACE - Launching via command line causes multiple issues (crashes to incorrect files)

30358 10.1 Timing Constraints - OFFSET OUT without a requirement causes "ERROR:Pack:1653"

30460 10.1 Timing Analyzer/Floorplan Editor -Crossprobing with non-updated NCD shows incorrect path

XPower Analyzer (XPA)

30479 10.1 XPower Analyzer (XPA) - Known Issues for XPA

XST

30328 10.1 XST - Known Issues List

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/17/08	1.0	Initial Xilinx release.
03/24/08	1.1	Added additional Answer Records; minor typographical updates.