



# Training Curriculum Paths

Wondering which Xilinx course is right for you? Use our curriculum paths to choose by design specialization: Hardware (Embedded or FPGA), Software, System, FPGA, SoC (Hardware Design or Software Development), Connectivity, DSP, or Languages. You can start with any optional or prerequisite courses or go straight to a course that is required.

Level 1 indicates core knowledge, skills, and techniques required to become proficient with Xilinx products.

Level 2 indicates advanced knowledge, skills, and techniques required for better optimization of Xilinx products.

Level 3 Indicates mastered knowledge, skills, and techniques required for best optimization and performance of Xilinx products.

Level 4 Indicates expert knowledge, skills, and techniques required to innovate with Xilinx products.

Just click any of the following to get started:

- [Embedded Hardware](#)
- [FPGA Hardware](#)
- [Software: Software Development](#)
- [Software: SDx SDSoC Development Environment](#)
- [Software: SDX SDAccel Development Environment](#)
- [System Courses](#)
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Embedded Hardware

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
Embedded Hardware	Course Name		Required / Optional	Products		Length	In Class / Online	Level
	Essentials of Microprocessors		Optional	SDK		8 hours	Both	1
	C Language Programming with SDK		Optional	SDK		16 hours	Both	1
	Introduction to the Zynq All Programmable SoC Architecture	or Zynq UltraScale+ MPSoC for the Hardware Designer	Optional	Zynq®-7000 AP SoC, Vivado® System Edition	or Zynq UltraScale+™ MPSoC, Vivado System Edition	8 hours	Both	3
	Embedded Systems Design		Required	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze™ Processor, SDK, Vivado System Edition		16 Hours	Both	3
	C-based Design: High-Level Synthesis with the Vivado HLx Tool		Optional	Zynq-7000 AP SoC, Vivado System Edition, SDSoC™ Development Environment, 7 Series		16 Hours	Both	3
	C-based HLS Coding for Hardware Designers		Optional	Zynq-7000 AP SoC, Vivado System Edition		4 hours	Both	3
	Advanced Features and Techniques of Embedded Systems Design		Required	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK, Vivado System Edition		16 Hours	Both	4

FPGA Hardware

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
FPGA Hardware	Course Name		Required / Optional	Products		Length	In Class / Online	Level
FPGA Core Design	<a href="#">Prerequisite: Languages &gt; Core HDL</a>		Optional	Vivado System Edition		24 hours	Both	1
	<a href="#">Designing FPGAs Using the Vivado Design Suite 1</a>		Required	Vivado System Edition, 7 Series, UltraScale™, UltraScale+ Families		16 hours	Both	1
	<a href="#">Designing FPGAs Using the Vivado Design Suite 2</a>		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families		16 hours	Both	2
	<a href="#">Designing FPGAs Using the Vivado Design Suite 3</a>		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families		16 Hours	Both	3
FPGA Advanced Design	<a href="#">Designing FPGAs Using the Vivado Design Suite 4</a>		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families		16 Hours	Both	4
	<a href="#">Xilinx Partial Reconfiguration Tools &amp; Techniques</a>		Optional	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families		16 Hours	Both	4

## Software Courses

Software course categories include:

- General-purpose Software Development
- SDx SDSoC Development Environment
- SDx SDAccel Development Environment

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
Software Courses	Course Name		Required / Optional	Products		Length	In Class / Online	Level
Software Development	<a href="#">Essentials of Microprocessors</a>		Optional	SDK		8 hours	Both	1
	<a href="#">C Language Programming with SDK</a>		Optional	SDK		16 hours	Both	1
	<a href="#">Embedded Systems Software Design</a>		Required	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK		16 hours	Both	3
	<a href="#">Zynq UltraScale+ MPSoC for the Software Developer</a>		Optional	Zynq UltraScale+ MPSoC, SDK		16 hours	Both	3
	<a href="#">Embedded Design with PetaLinux Tools</a>		Optional	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK, Vivado System Edition		16 Hours	Both	4
	<a href="#">Advanced Features and Techniques of Embedded Systems Software Design</a>		Optional	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, SDK		8 Hours	Both	4

**Software Courses: SDx SDSoC Development Environment**

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
Software Courses	Course Name		Required / Optional	Products		Length	In Class / Online	Level
<b>SDx SDSoC Development Environment</b>	<a href="#">Essentials of Microprocessors</a>		Optional	SDK		8 hours	Both	1
	<a href="#">C Language Programming with SDK</a>		Optional	SDK		16 hours	Both	1
	<a href="#">Embedded C/C++ SDSoC Development Environment and Methodology</a>		Required	Zynq-7000 AP SoC, SDx™ Development Environment		16 hours	Both	2
	<a href="#">C-based Design: High-Level Synthesis with the Vivado HLx Tool</a>		Optional	Zynq-7000 AP SoC, 7 Series, Vivado System Edition, SDx Development Environment		16 hours	Both	3
	<a href="#">C-based HLS Coding for Software Designers</a>		Optional	Zynq-7000 AP SoC, 7 Series, Vivado System Edition, SDx Development Environment		4 hours	Both	3

**Software Courses: SDx SDAccel Development Environment**

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
Software Courses	Course Name		Required / Optional	Products		Length	In Class / Online	Level
<b>SDx SDAccel Development Environment</b>	<a href="#">Essentials of Microprocessors</a>		Optional	SDK		8 hours	Both	1
	<a href="#">C Language Programming with SDK</a>		Optional	SDK		16 hours	Both	1
	<a href="#">Developing and Optimizing Applications Using the OpenCL Framework for FPGAs</a>		Required	7 Series, UltraScale, and UltraScale+ Families, SDx Development Environment		16 hours	Both	2
	<a href="#">C-based Design: High-Level Synthesis with the Vivado HLx Tool</a>		Optional	Zynq-7000 AP SoC, 7 Series, Vivado System Edition, SDx Development Environment		16 hours	Both	3
	<a href="#">C-based HLS Coding for Software Designers</a>		Optional	Zynq-7000 AP SoC, 7 Series, Vivado System Edition, SDx Development Environment		4 hours	Both	3

System Courses

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages			
System Courses	Course Name		Required / Optional	Products		Length	In Class / Online	Level		
	Zynq All Programmable SoC System Architecture	or	Zynq UltraScale+ MPSoC for the System Architect	Required	Zynq-7000 AP SoC, Vivado System Edition, SDK	or	Zynq UltraScale+ MPSoC, Vivado System Edition, SDK	16 hours	Both	3

FPGA Courses

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages
FPGA Courses	Course Name		Required / Optional	Products	Length	In Class / Online	Level
FPGA Core Design	Prerequisite: Languages > Core HDL		Optional	Vivado System Edition	24 hours	Both	1
	Designing FPGAs Using the Vivado Design Suite 1		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	16 hours	Both	1
	Designing FPGAs Using the Vivado Design Suite 2		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	16 hours	Both	2
	Designing FPGAs Using the Vivado Design Suite 3		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	16 Hours	Both	3
FPGA Advanced Design	Designing FPGAs Using the Vivado Design Suite 4		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	16 Hours	Both	4
	Xilinx Partial Reconfiguration Tools & Techniques		Optional	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	16 Hours	Both	4
Vivado Design Suite for ISE Design Suite Users	Vivado Design Suite for ISE Software Project Navigator Users		Optional	Vivado System Edition	8 hours	Both	2
	Vivado Design Suite Advanced XDC and Static Timing Analysis for ISE Software Users		Optional	Vivado System Edition	24 hours	Both	3



### SoC Courses

System on a Chip course categories include:

- SoC Hardware Design
- SoC Software Development

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages			
SoC Courses	Course Name		Required / Optional	Products			Length	In Class / Online	Level	
Hardware Design	Essentials of Microprocessors		Optional	SDK			8 hours	Both	1	
	C Language Programming with SDK		Optional	SDK			16 hours	Both	1	
	Introduction to the Zynq All Programmable SoC Architecture	or	Zynq UltraScale+ MPSoC for the Hardware Designer	Optional	Zynq-7000 AP SoC, Vivado System Edition	or	Zynq UltraScale+ MPSoC, Vivado System Edition	8 hours	Both	3
	Embedded Systems Design		Required	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK, Vivado System Edition			16 Hours	Both	3	
	C-based Design: High-Level Synthesis with the Vivado HLx Tool		Optional	Zynq-7000 AP SoC, Vivado System Edition, SDSoC Design Environment, 7 Series			16 Hours	Both	3	
	C-based HLS Coding for Hardware Designers		Optional	Zynq-7000 AP SoC, Vivado System Edition			4 hours	Both	3	
	Advanced Features and Techniques of Embedded Systems Design		Required	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK, Vivado System Edition			16 Hours	Both	4	

SoC Courses: Software Development

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
SoC Courses	Course Name		Required / Optional	Products		Length	In Class / Online	Level
Software Development	Essentials of Microprocessors		Optional	SDK		8 hours	Both	1
	C Language Programming with SDK		Optional	SDK		16 hours	Both	1
	Embedded C/C++ SDSoC Development Environment and Methodology		Optional	Zynq-7000 AP SoC, SDx Development Environment		16 hours	Both	2
	C-based Design: High-Level Synthesis with the Vivado HLx Tool		Optional	Zynq-7000 AP SoC, 7 Series, Vivado System Edition, SDx Development Environment		16 hours	Both	3
	C-based HLS Coding for Software Designers		Optional	Zynq-7000 AP SoC, 7 Series, Vivado System Edition, SDx Development Environment		4 hours	Both	3
	Embedded Systems Software Design		Required	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK,		16 hours	Both	3
	Zynq UltraScale+ MPSoC for the Software Developer		Optional	Zynq UltraScale+ MPSoC, SDK,		16 hours	Both	3
	Embedded Design with PetaLinux Tools		Optional	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, MicroBlaze Processor, SDK, Vivado System Edition		16 Hours	Both	4
	Advanced Features and Techniques of Embedded Systems Software Design		Optional	Zynq-7000 AP SoC, Zynq UltraScale+ MPSoC, SDK		8 Hours	Both	4

Connectivity Courses

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
Connectivity Courses	Course Name		Required / Optional		Products	Length	In Class / Online	Level
PCI Express	Prerequisite: <a href="#">FPGA &gt; FPGA Core Design</a>		Required		Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families			1-3
	<a href="#">PCIe Protocol Overview</a>		Optional		7 Series, UltraScale, UltraScale+ Families	8 hours	Both	2
	<a href="#">Designing an Integrated PCI Express System</a>		Required		Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	16 hours	Both	3
Transceivers	Prerequisite: <a href="#">FPGA &gt; FPGA Core Design</a>		Required		Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families			1-3
	<a href="#">Designing with Multi-Gigabit Serial I/O</a>		Required		Vivado System Edition, 7 Series Families	24 hours	Both	3
	<a href="#">Designing with UltraScale FPGA Transceivers</a>		Required		Vivado System Edition, UltraScale Families	16 hours	Both	3
Memory Interface	Prerequisite: <a href="#">FPGA &gt; FPGA Core Design</a>		Required		Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families			1-3
	<a href="#">How to Design a High-Speed Memory Interface</a>		Required		Vivado System Edition, 7 Series Families	16 hours	Both	3
Ethernet MAC	Prerequisite: <a href="#">FPGA &gt; FPGA Core Design</a>		Required		Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families			1-3
	<a href="#">Designing with Ethernet MAC Controllers</a>		Required		Vivado System Edition, 7 Series, UltraScale Families	16 hours	Both	3
Signal Integrity and Board Design	<a href="#">Signal Integrity and Board Design for Xilinx FPGAs</a>		Required		Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families	24 hours	Online	3

DSP Courses

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
DSP Courses	Course Name		Required / Optional	Products		Length	In Class / Online	Level
DSP Design	Prerequisite: FPGA > FPGA Core Design		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families				1-3
	Essential DSP Implementation Techniques for Xilinx FPGAs		Required	7 Series Families		16 hours	Both	3
	DSP Design Using System Generator		Required	Vivado System Edition, 7 Series, UltraScale, UltraScale+ Families		16 hours	Both	3

Language Courses

Hardware	Software	System	FPGA	SoC	Connectivity	DSP	Languages	
Language Courses	Course Name			Required / Optional	Products	Length	In Class / Online	Level
Core HDL	Designing with Verilog	or	Designing with VHDL	Required	Vivado System Edition	24 hours	Both	1
System Verilog	Designing with SystemVerilog			Required	Vivado System Edition	16 hours	Both	1
	Verification with SystemVerilog			Required	Vivado System Edition	16 hours	Both	1
Advanced VHDL	Advanced VHDL			Required	Vivado System Edition	16 hours	Both	4