



# Vitis design Analysis

Introduction to Vitis



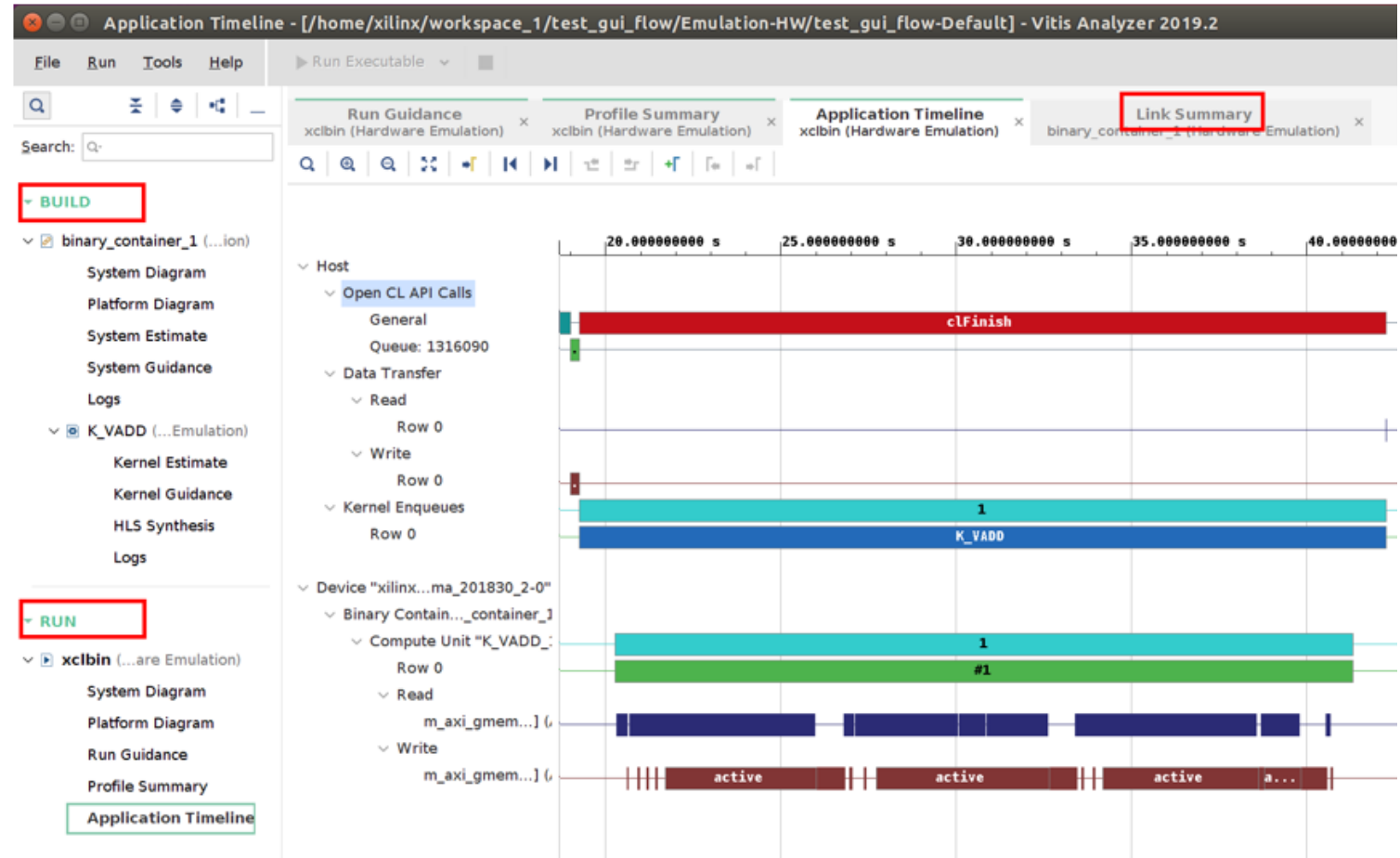
# Profiling: Vitis Analyzer

## ► Vitis analyzer

- To view and analyze the reports
  - Build reports generated by the Vitis compiler
  - Run reports after the application is executed

## ► Design analysis

- System resources and performance
- Kernel and Host optimization
- Data transfer





# Vitis Profiling – System Optimization reports

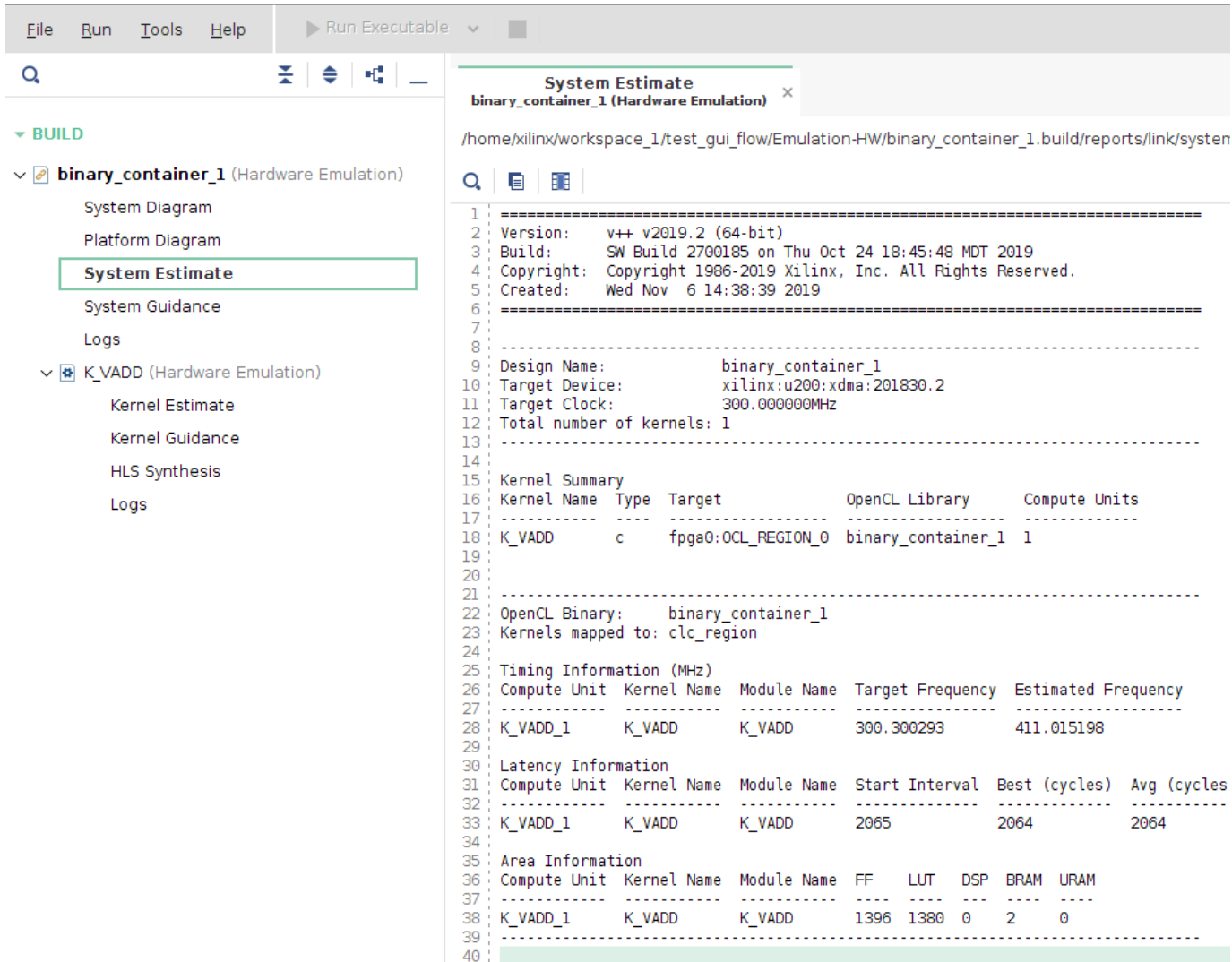
Goal	Report	Information	Operations
System (Host and Kernel) Optimization	Profile Summary Report	Top Operations	Data Transfers
		Kernel & Compute Units	OpenCL APIs
	Application Timeline	Host Events	
		Device Trace Data	



# Vitis Profiling – Kernel Optimization reports

Goal	Report	Information
Kernel Optimization	Guidance	Host & Kernel Data Transfer
	System Estimate Report	Device and Kernel Summary
		Timing and Latency
		Area Estimate
	HLS Report	Performance Estimate
		Utilizations Estimates
		Interface Information
	Waveform View	HLS Process Summary
		Waveform View
		Live View

# System Estimate Report



The screenshot shows the Xilinx IDE interface. On the left, the 'BUILD' tree is expanded, showing 'binary\_container\_1 (Hardware Emulation)' with 'System Estimate' selected. The main window displays the 'System Estimate' report for 'binary\_container\_1 (Hardware Emulation)'. The report path is '/home/xilinx/workspace\_1/test\_gui\_flow/Emulation-HW/binary\_container\_1.build/reports/link/system'. The report content includes version information, design details, a kernel summary table, OpenCL binary information, timing information, latency information, and area information.

```
1 =====
2 Version:      v++ v2019.2 (64-bit)
3 Build:       SW Build 2700185 on Thu Oct 24 18:45:48 MDT 2019
4 Copyright:   Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
5 Created:    Wed Nov  6 14:38:39 2019
6 =====
7
8 -----
9 Design Name:      binary_container_1
10 Target Device:   xilinx:u200:xdma:201830.2
11 Target Clock:    300.000000MHz
12 Total number of kernels: 1
13 -----
14
15 Kernel Summary
16 Kernel Name  Type  Target          OpenCL Library  Compute Units
17 -----
18 K_VADD       c    fpga0:OCL_REGION_0  binary_container_1  1
19
20 -----
21
22 OpenCL Binary:   binary_container_1
23 Kernels mapped to: clc_region
24
25 Timing Information (MHz)
26 Compute Unit  Kernel Name  Module Name  Target Frequency  Estimated Frequency
27 -----
28 K_VADD_1      K_VADD      K_VADD      300.300293       411.015198
29
30 Latency Information
31 Compute Unit  Kernel Name  Module Name  Start Interval  Best (cycles)  Avg (cycles)
32 -----
33 K_VADD_1      K_VADD      K_VADD      2065            2064           2064
34
35 Area Information
36 Compute Unit  Kernel Name  Module Name  FF    LUT    DSP    BRAM    URAM
37 -----
38 K_VADD_1      K_VADD      K_VADD      1396  1380  0      2      0
39
40 =====
```

- ▶ Takes into account the target hardware device and each compute unit
- ▶ Estimates performance from known information
- ▶ Exact performance metric can only be measured by running the application on the FPGA

# System Estimate Report > Device and Kernel Summary

```
=====
Version:      v++ v2019.2 (64-bit)
Build:        SW Build 2700185 on Thu Oct 24 18:45:48 MDT 2019
Copyright:    Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
Created:      Wed Nov  6 14:38:39 2019
=====
```

```
-----
Design Name:      binary_container_1
Target Device:    xilinx:u200:xdma:201830.2
Target Clock:     300.000000MHz
Total number of kernels: 1
-----
```

Design and Target  
Device Summary

```
Kernel Summary
Kernel Name  Type  Target                OpenCL Library        Compute Units
-----
K_VADD       c     fpga0:OCL_REGION_0    binary_container_1     1
```

Kernel Summary  
1 kernel in the XCLBIN

# System Estimate Report > Timing, Latency, and Area

OpenCL Binary:      binary\_container\_1  
Kernels mapped to: clc\_region

Binary Info

Timing Information (MHz)

Compute Unit	Kernel Name	Module Name	Target Frequency	Estimated Frequency
--------------	-------------	-------------	------------------	---------------------

Timing Info

Latency Information

Compute Unit	Kernel Name	Module Name	Start Interval	Best (cycles)	Avg (cycles)
--------------	-------------	-------------	----------------	---------------	--------------

Latency Info

K_VADD_1	K_VADD	K_VADD	2065	2064	2064
----------	--------	--------	------	------	------

Avg (cycles)	Worst (cycles)	Best (absolute)	Avg (absolute)	Worst (absolute)
2064	2064	6.879 us	6.879 us	6.879 us

Area Information

Compute Unit	Kernel Name	Module Name	FF	LUT	DSP	BRAM	URAM
--------------	-------------	-------------	----	-----	-----	------	------

Area Info

K_VADD_1	K_VADD	K_VADD	1396	1380	0	2	0
----------	--------	--------	------	------	---	---	---

## ► Latency info:

- Only calculates *inside* compute unit
- In-system latencies and overheads are not reported

## ► Area Info

- Estimate per compute unit
- May vary with final implementation

# Profile Summary Report

Q

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▼ RUN

▼ xclbin (...ulation)

System Diagr...

Platform Diag...

Run Guidance

Profile Sum...

Application Ti...

Run Summary xclbin (Hardware Emulation) ×

Profile Summary xclbin (Hardware Emulation) ×

Top Operations | Kernels & Compute Units | Data Transfers | OpenCL APIs

▼ Top Data Transfer: Kernels to Global Memory

Device	Compute Unit	Number Of Transfers	Average Bytes per Transfer	Transfer Efficiency
xilinx_u200_xdma_201830_2-0	K_VADD_1	2112	5.818	0.

▼ Top Kernel Execution

Kernel Instance Address	Kernel	Context ID	Command Queue ID	Device	St Ti
0x13420b0	K_VADD	0	0	xilinx_u200_xdma_201830_2-0	

▼ Top Memory Writes: Host to Global Memory

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Wri Rat
0x400000000	0	0	18996.400	N/A	4.096	
0x400001000	0	0	19254.300	N/A	4.096	

▼ Top Memory Reads: Host to Global Memory

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Rea Rat
0x400002000	0	0	42268.900	N/A	4.096	

- ▶ The Vitis runtime library automatically collects profiling data on host applications
- ▶ After the application finishes execution, the profile summary is saved in the solution report directory or working directory



# Profile Summary Report

Run Summary  
xclbin (Hardware Emulation)

Profile Summary  
xclbin (Hardware Emulation)

Top Operations

Kernels & Compute Units

Data Transfers

OpenCL APIs

▼ Top Data Transfer: Kernels to Global Memory

Device	Compute Unit	Number Of Transfers	Average Bytes per Transfer	Transfer Efficiency (%)	Total Data Transfer (MB)	Total Write (MB)	Total Read (MB)	Total Transfer Rate (MB/s)
xilinx_u200_xdma_201830_2-0	K_VADD_1	2112	5.818	0.142	0.012	0.004	0.008	277.674

▼ Top Kernel Execution

Kernel Instance Address	Kernel	Context ID	Command Queue ID	Device	Start Time (ms)	Duration (ms)	Global Work Size	Local Work Size
0x13420b0	K_VADD	0	0	xilinx_u200_xdma_201830_2-0	0.017	0.026	1:1:1	1:1:1

▼ Top Memory Writes: Host to Global Memory

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Writing Rate (MB/s)
0x400000000	0	0	18996.400	N/A	4.096	N/A
0x400001000	0	0	19254.300	N/A	4.096	N/A

▼ Top Memory Reads: Host to Global Memory

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Reading Rate (MB/s)
0x400002000	0	0	42268.900	N/A	4.096	N/A

# Profile Summary Report > OpenCL APIs

Run Summary xclbin (Hardware Emulation) x						
Profile Summary xclbin (Hardware Emulation) x						
Top Operations   Kernels & Compute Units   Data Transfers   OpenCL APIs						
OpenCL API Calls						
API Name	Number Of Calls	Total Time (ms)	Minimum Time (ms)	Average Time (ms)	Maximum Time (ms)	
clCreateProgramWithBinary	1	85750.400	85750.400	85750.400	85750.400	
clFinish	1	26024.300	26024.300	26024.300	26024.300	
clReleaseProgram	1	4085.500	4085.500	4085.500	4085.500	
clCreateBuffer	3	2.436	0.461	0.812	1.307	
clCreateKernel	1	2.198	2.198	2.198	2.198	
clEnqueueTask	1	0.989	0.989	0.989	0.989	
clReleaseMemObject	3	0.423	0.013	0.141	0.397	
clEnqueueMigrateMemObjects	3	0.337	0.043	0.112	0.153	
clSetKernelArg	3	0.060	0.016	0.020	0.022	
clGetPlatformIDs	2	0.050	0.012	0.025	0.038	
clGetDeviceIDs	2	0.034	0.012	0.017	0.022	
clBuildProgram	1	0.030	0.030	0.030	0.030	
clGetDeviceInfo	2	0.027	0.013	0.014	0.014	
clReleaseKernel	1	0.026	0.026	0.026	0.026	
clGetPlatformInfo	2	0.024	0.012	0.012	0.012	
clReleaseDevice	1	0.022	0.022	0.022	0.022	
clReleaseCommandQueue	1	0.020	0.020	0.020	0.020	
clCreateContext	1	0.015	0.015	0.015	0.015	

# HLS Report

- ▶ HLS report is generated by the Vivado HLS tools
- ▶ Includes details on performance and logic usage of kernels
  - Performance estimates
    - Clock speed, throughput, latency
  - Utilization
  - Interfaces
- ▶ Provides insights to guide kernel optimization

The screenshot shows the 'Synthesis Report for 'mmult'' in Vivado. It includes metadata like Date, Version, Project, and Solution. The 'Performance Estimates' section contains tables for Timing (ns) and Latency (clock cycles). The 'Utilization Estimates' section contains a table showing resource usage for various components.

**Synthesis Report for 'mmult'**

Vivado HLS Report for 'mmult'

Date: Sun Sep 15 17:51:50 2019  
Version: 2019.2 (Build 2644986 on Wed Sep 04 21:26:32 MDT 2019)  
Project: mmult  
Solution: solution  
Product family: virtexplus  
Target device: xcu200-fsgd2104-2-e

**Performance Estimates**

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	3.33	2.433	0.90

Latency (clock cycles)

Summary

Latency		Interval		min max	
min	max	min	max	Type	825 828
2.750 (us)	2.760 (us)	825	828	none	

Detail

Instance

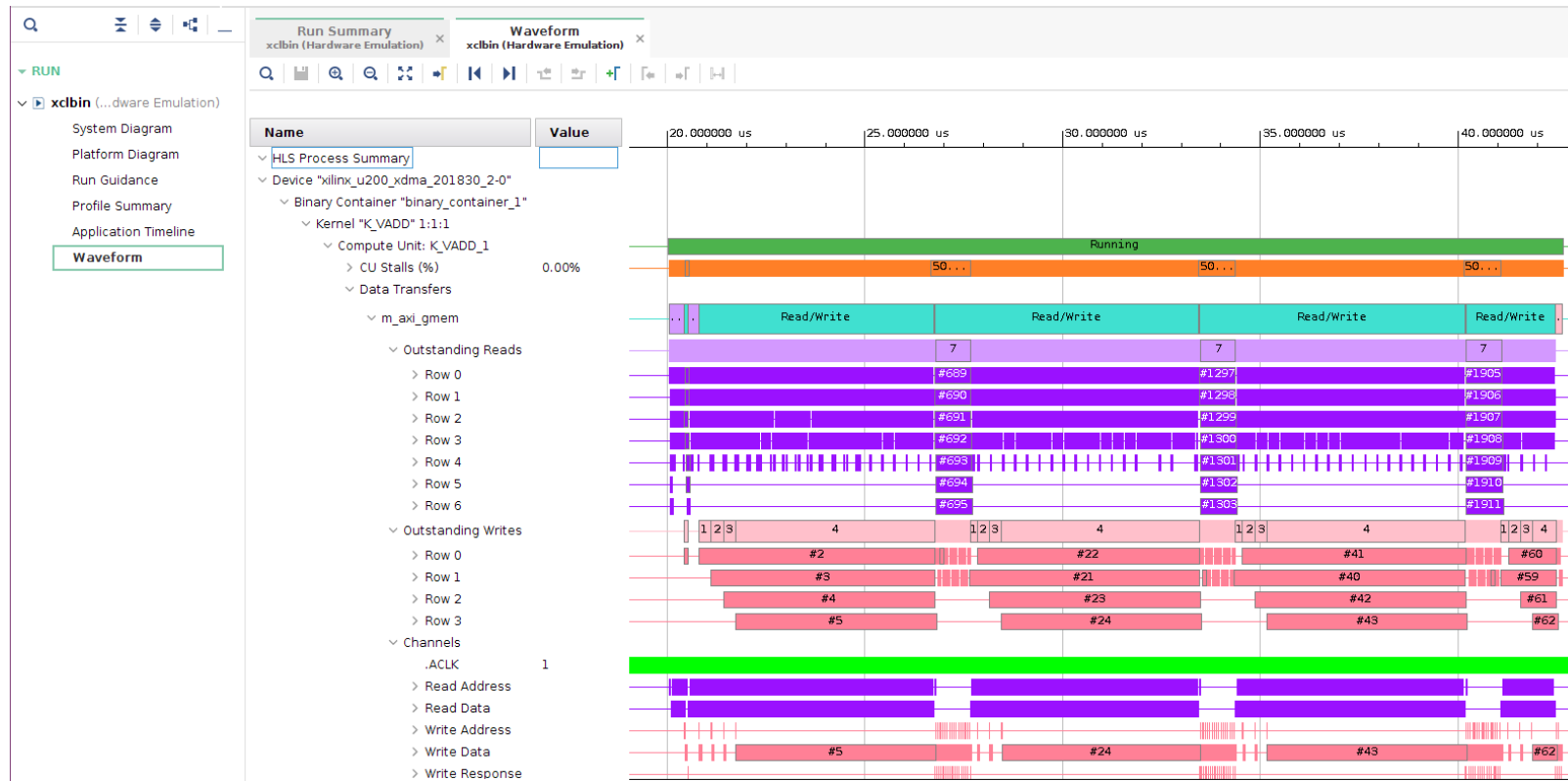
Loop

**Utilization Estimates**

Summary

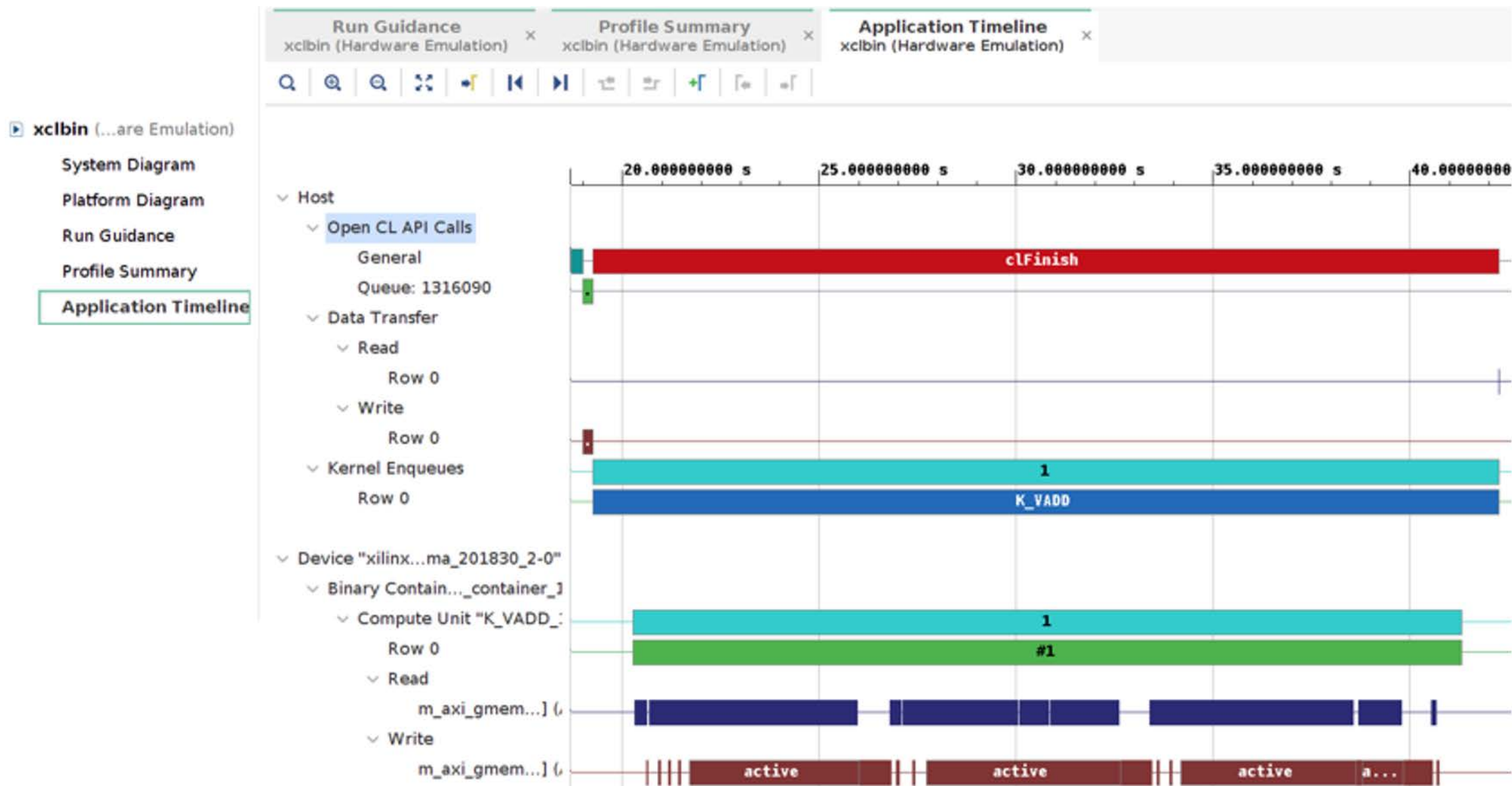
Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	18774	-
FIFO	-	-	-	-	-
Instance	2	1036	60701	15249	-
Memory	0	-	2048	256	0
Multiplexer	-	-	-	914	-

# Waveform View and Live Waveform Viewer



- ▶ Generate a Waveform view and launch a Live Waveform viewer when running hardware emulation
- ▶ Displays in-depth details on the emulation results at the system level, compute unit level, and function level
- ▶ Waveform view and live waveform viewer are not enabled by default
  - Consumes more time and disk space

# Application Timeline





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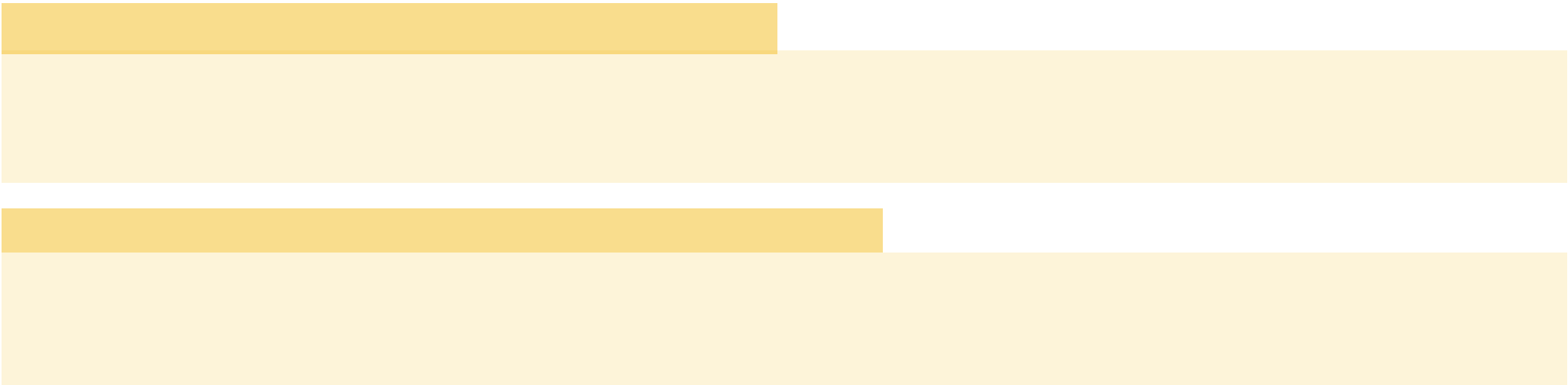
# Thank You



# Appendix



# Profile Summary Report > Kernels & Compute Units



Dataflow Acceleration	Total Time (ms)	Minimum Time (ms)	Average Time (ms)	Maximum Time (ms)	Clock Freq (MHz)	CU Utilization (%)
1.000000x	0.023	0.023	0.023	0.023	300	90.740



# Profile Summary Report > Data Transfers (1)

Run Summary  
xclbin (Hardware Emulation) ×

Profile Summary  
xclbin (Hardware Emulation) ×

Top Operations | Kernels & Compute Units | **Data Transfers** | OpenCL APIs

## ▼ Data Transfer: Host to Global Memory

Context: Number of Devices	Transfer Type	Number Of Buffer Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Buffer Size (KB)	Total Time (ms)	Average Time (ms)
context0:1	READ	1	N/A	N/A	4.096	N/A	N/A
context0:1	WRITE	2	N/A	N/A	4.096	N/A	N/A

## ▼ Data Transfer: Kernels to Global Memory

Device	Compute Unit/ Port Name	Kernel Arguments	Memory Resources	Transfer Type	Number Of Transfers	Transfer Rate (MB/s)
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A B R	DDR[1]	READ	2048	366.478
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A B R	DDR[1]	WRITE	64	187.032

Average Bandwidth Utilization (%)	Average Size (KB)	Average Latency (ns)
3.181	0.004	39.700
1.624	0.064	1159.480

## ► Host and global memory PCIe transfers

- Transfer rate, number of transfers
- Average size of transfer, average bandwidth utilization
- Average time, total time

# Profile Summary Report > Data Transfers (2)

Run Summary  
xclbin (Hardware Emulation)

Profile Summary  
xclbin (Hardware Emulation)

Top Operations

Kernels & Compute Units

Data Transfers

OpenCL APIs

▼ Data Transfer: Host to Global Memory

Context: Number of Devices	Transfer Type	Number Of Buffer Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Buffer Size (KB)	Total Time (ms)	Average Time (ms)	
context0:1	READ	1	N/A	N/A	4.096	N/A	N/A	
context0:1	WRITE	2	N/A	N/A	4.096	N/A	N/A	

▼ Data Transfer: Kernels to Global Memory

Device	Compute Unit/ Port Name	Kernel Arguments	Memory Resources	Transfer Type	Number Of Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Size (KB)	Average Latency (ns)
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A B R	DDR[1]	READ	2048	366.478	3.181	0.004	39.700
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A B R	DDR[1]	WRITE	64	187.032	1.624	0.064	1159.480

## ► Kernels and global memory transfers

- Transfer rate, number of transfers
- Average size of transfer, average bandwidth utilization
- Average time, total time