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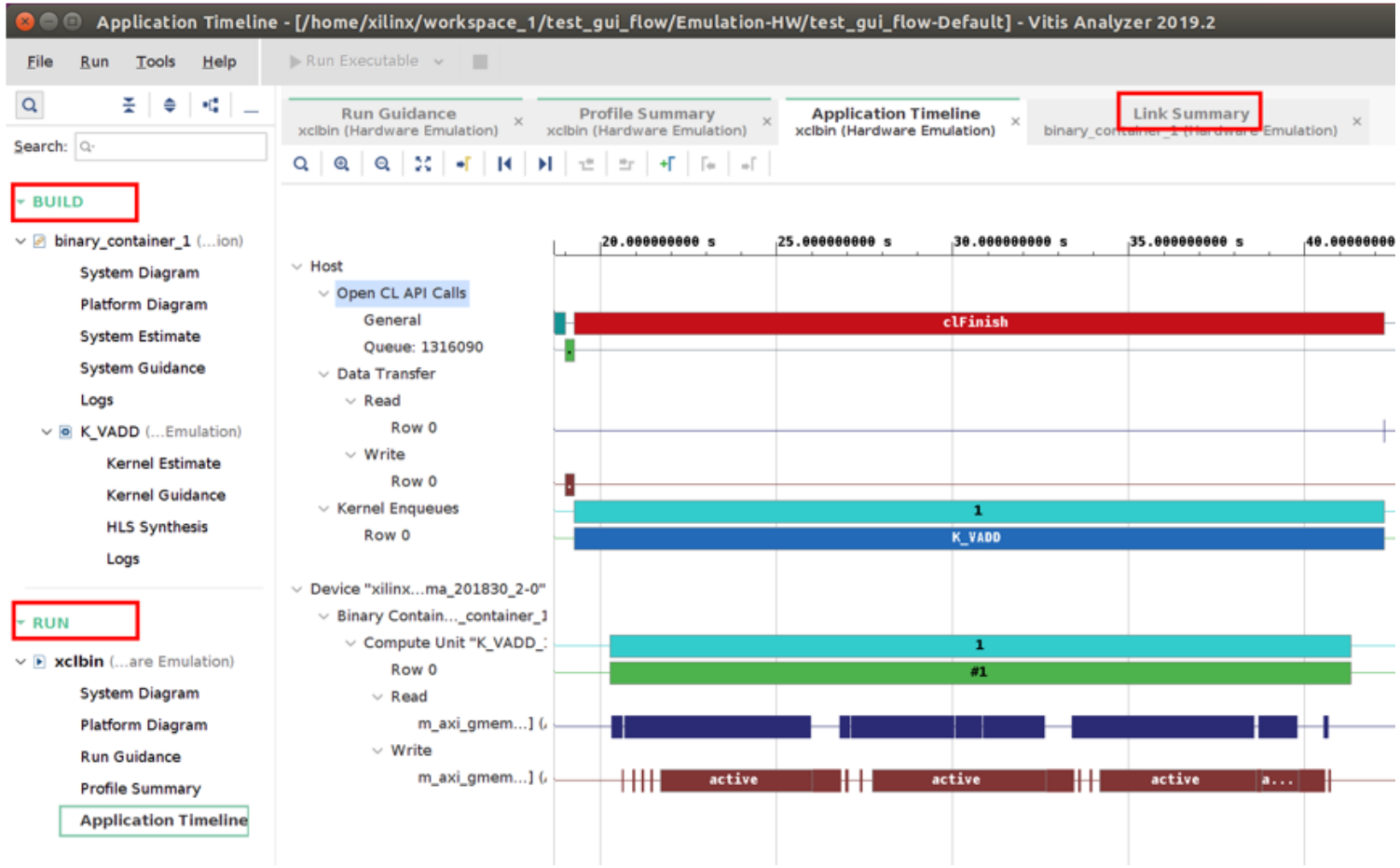
Vitis design Analysis

Introduction to Vitis

Profiling: Vitis Analyzer

- Vitis analyzer
  - To view and analyze the reports
    - Build reports generated by the Vitis compiler
    - Run reports after the application is executed
- Design analysis
  - System resources and performance
  - Kernel and Host optimization
  - Data transfer



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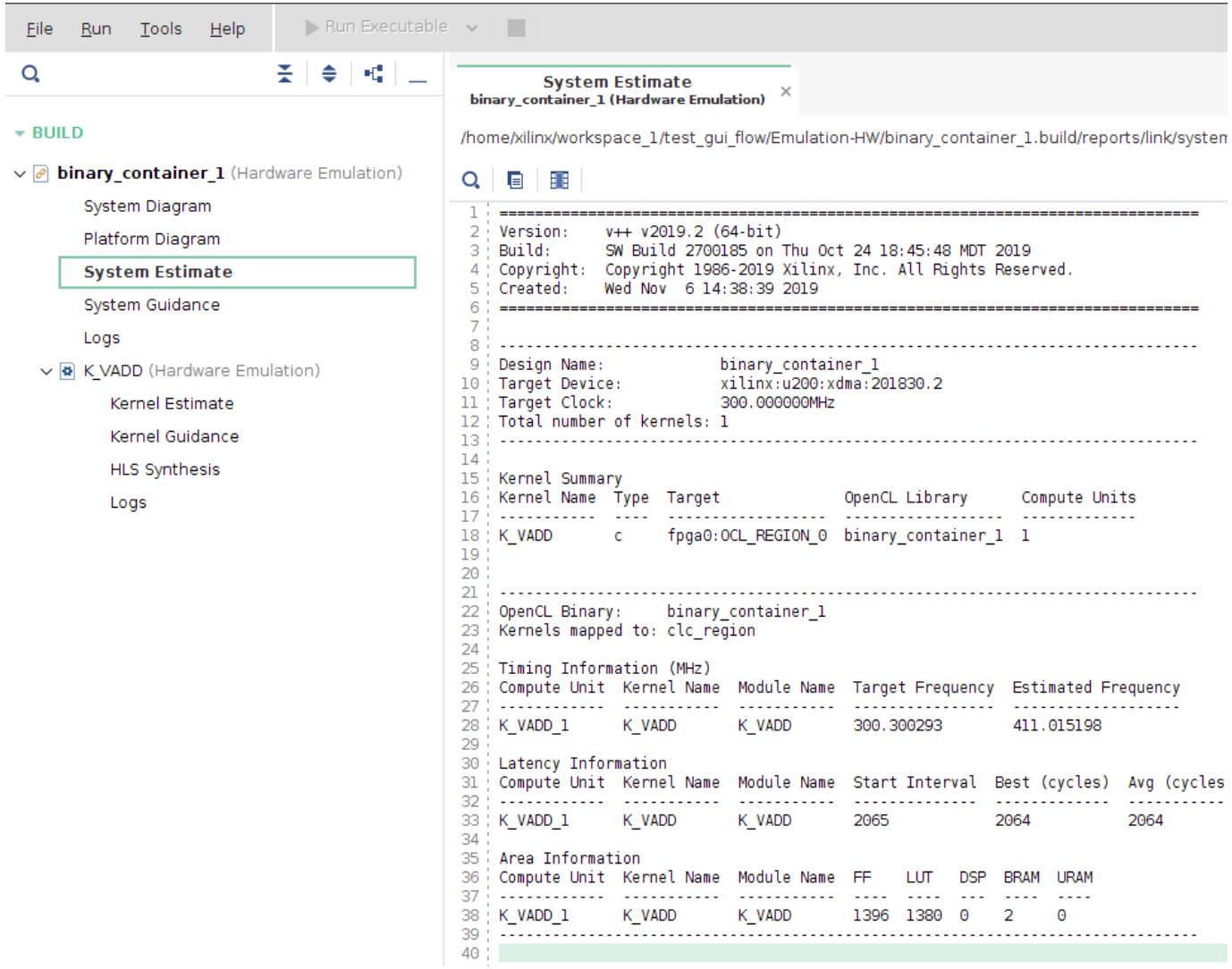
Vitis Profiling – System Optimization reports

Goal	Report	Information	Operations
System (Host and Kernel) Optimization	Profile Summary Report	Top Operations	Data Transfers
		Kernel & Compute Units	OpenCL APIs
	Application Timeline	Host Events	
		Device Trace Data	

Vitis Profiling – Kernel Optimization reports

Goal	Report	Information
Kernel Optimization	Guidance	Host & Kernel Data Transfer
	System Estimate Report	Device and Kernel Summary
		Timing and Latency
		Area Estimate
	HLS Report	Performance Estimate
		Utilizations Estimates
		Interface Information
	Waveform View	HLS Process Summary
		Waveform View
		Live View

System Estimate Report



- Takes into account the target hardware device and each compute unit
- Estimates performance from known information
- Exact performance metric can only be measured by running the application on the FPGA

System Estimate Report > Device and Kernel Summary

```
================================================================================
Version:    v++ v2019.2 (64-bit)
Build:      SW Build 2700185 on Thu Oct 24 18:45:48 MDT 2019
Copyright:  Copyright 1986-2019 Xilinx, Inc. All Rights Reserved.
Created:    Wed Nov  6 14:38:39 2019
================================================================================

--------------------------------------------------------------------------------
Design Name:             binary_container_1
Target Device:           xilinx:u200:xdma:201830.2
Target Clock:            300.000000MHz
Total number of kernels: 1
--------------------------------------------------------------------------------

Kernel Summary
Kernel Name  Type  Target              OpenCL Library      Compute Units
-----------  ----  ------------------  ------------------  -------------
K_VADD       c     fpga0:OCL_REGION_0  binary_container_1  1
```

Design and Target Device Summary

Kernel Summary
1 kernel in the XCLBIN

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System Estimate Report > Timing, Latency, and Area

```
================================================================
OpenCL Binary:     binary_container_1
Kernels mapped to: clc_region
```

Binary Info

```
Timing Information (MHz)
Compute Unit  Kernel Name  Module Name  Target Frequency  Estimated Frequency
------------  -----------  -----------  ----------------  -------------------
```

Timing Info

```
Latency Information
Compute Unit  Kernel Name  Module Name  Start Interval  Best (cycles)  Avg (cycles)
------------  -----------  -----------  --------------  -------------  ------------
K_VADD_1      K_VADD       K_VADD       2065            2064           2064

Avg (cycles)  Worst (cycles)  Best (absolute)  Avg (absolute)  Worst (absolute)
------------  --------------  ---------------  --------------  ----------------
2064          2064            6.879 us         6.879 us        6.879 us
```

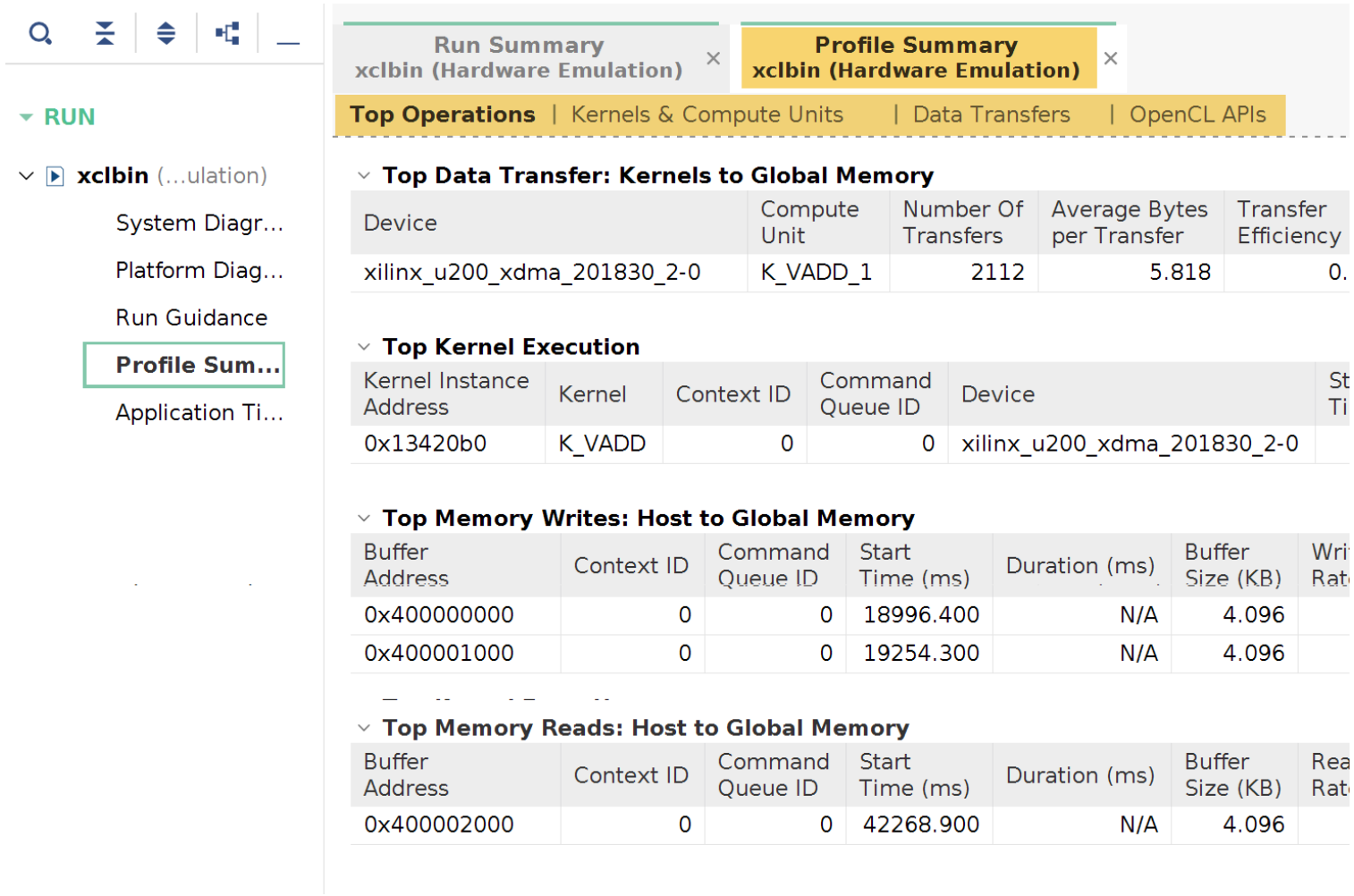
Latency Info

```
Area Information
Compute Unit  Kernel Name  Module Name  FF    LUT   DSP  BRAM  URAM
------------  -----------  -----------  ----  ----  ---  ----  ----
K_VADD_1      K_VADD       K_VADD       1396  1380  0    2     0
```

Area Info

- Latency info:
  - Only calculates *inside* compute unit
  - In-system latencies and overheads are not reported
- Area Info
  - Estimate per compute unit
  - May vary with final implementation

Profile Summary Report



- The Vitis runtime library automatically collects profiling data on host applications
- After the application finishes execution, the profile summary is saved in the solution report directory or working directory

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Profile Summary Report

Run Summary
xclbin (Hardware Emulation)

Profile Summary
xclbin (Hardware Emulation)

Top Operations | Kernels & Compute Units | Data Transfers | OpenCL APIs

Top Data Transfer: Kernels to Global Memory

Device	Compute Unit	Number Of Transfers	Average Bytes per Transfer	Transfer Efficiency (%)	Total Data Transfer (MB)	Total Write (MB)	Total Read (MB)	Total Transfer Rate (MB/s)
xilinx_u200_xdma_201830_2-0	K_VADD_1	2112	5.818	0.142	0.012	0.004	0.008	277.674

Top Kernel Execution

Kernel Instance Address	Kernel	Context ID	Command Queue ID	Device	Start Time (ms)	Duration (ms)	Global Work Size	Local Work Size
0x13420b0	K_VADD	0	0	xilinx_u200_xdma_201830_2-0	0.017	0.026	1:1:1	1:1:1

Top Memory Writes: Host to Global Memory

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Writing Rate (MB/s)
0x400000000	0	0	18996.400	N/A	4.096	N/A
0x400001000	0	0	19254.300	N/A	4.096	N/A

Top Memory Reads: Host to Global Memory

Buffer Address	Context ID	Command Queue ID	Start Time (ms)	Duration (ms)	Buffer Size (KB)	Reading Rate (MB/s)
0x400002000	0	0	42268.900	N/A	4.096	N/A

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Profile Summary Report > OpenCL APIs

Run Summary
xclbin (Hardware Emulation)

Profile Summary
xclbin (Hardware Emulation)

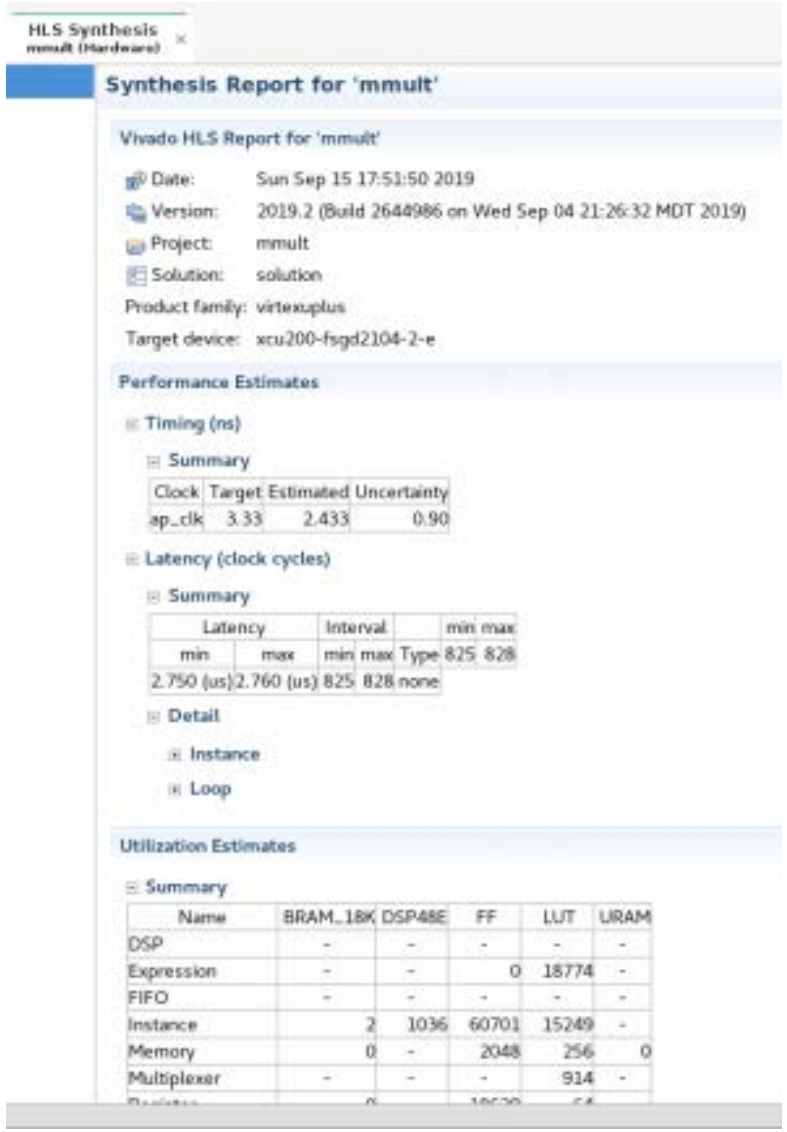
Top Operations | Kernels & Compute Units | Data Transfers | **OpenCL APIs**

OpenCL API Calls

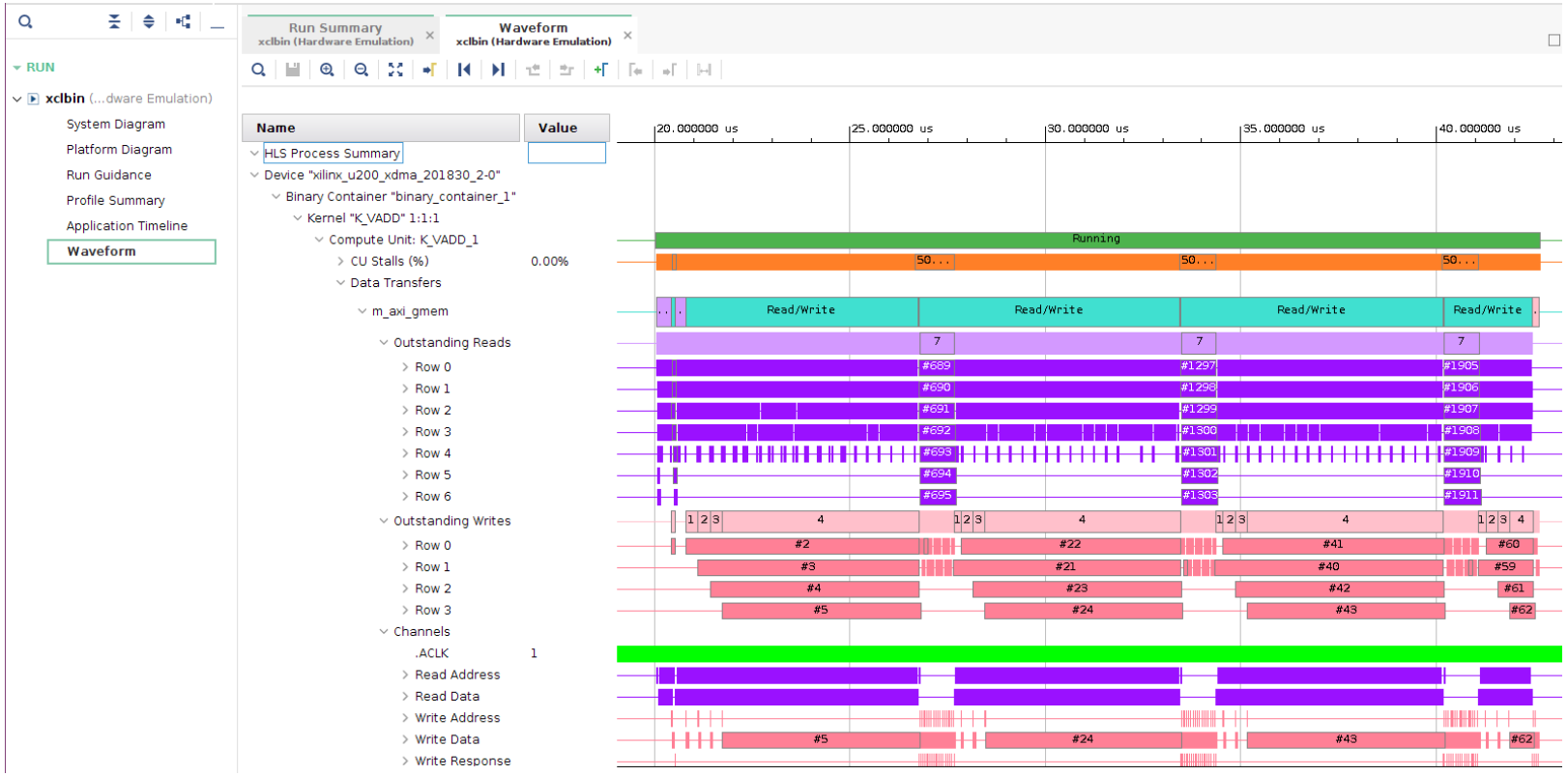
API Name	Number Of Calls	Total Time (ms)	Minimum Time (ms)	Average Time (ms)	Maximum Time (ms)
clCreateProgramWithBinary	1	85750.400	85750.400	85750.400	85750.400
clFinish	1	26024.300	26024.300	26024.300	26024.300
clReleaseProgram	1	4085.500	4085.500	4085.500	4085.500
clCreateBuffer	3	2.436	0.461	0.812	1.307
clCreateKernel	1	2.198	2.198	2.198	2.198
clEnqueueTask	1	0.989	0.989	0.989	0.989
clReleaseMemObject	3	0.423	0.013	0.141	0.397
clEnqueueMigrateMemObjects	3	0.337	0.043	0.112	0.153
clSetKernelArg	3	0.060	0.016	0.020	0.022
clGetPlatformIDs	2	0.050	0.012	0.025	0.038
clGetDeviceIDs	2	0.034	0.012	0.017	0.022
clBuildProgram	1	0.030	0.030	0.030	0.030
clGetDeviceInfo	2	0.027	0.013	0.014	0.014
clReleaseKernel	1	0.026	0.026	0.026	0.026
clGetPlatformInfo	2	0.024	0.012	0.012	0.012
clReleaseDevice	1	0.022	0.022	0.022	0.022
clReleaseCommandQueue	1	0.020	0.020	0.020	0.020
clCreateContext	1	0.015	0.015	0.015	0.015

HLS Report

- HLS report is generated by the Vivado HLS tools
- Includes details on performance and logic usage of kernels
  - Performance estimates
    - Clock speed, throughput, latency
  - Utilization
  - Interfaces
- Provides insights to guide kernel optimization



Waveform View and Live Waveform Viewer



- Generate a Waveform view and launch a Live Waveform viewer when running hardware emulation
- Displays in-depth details on the emulation results at the system level, compute unit level, and function level
- Waveform view and live waveform viewer are not enabled by default
  - Consumes more time and disk space

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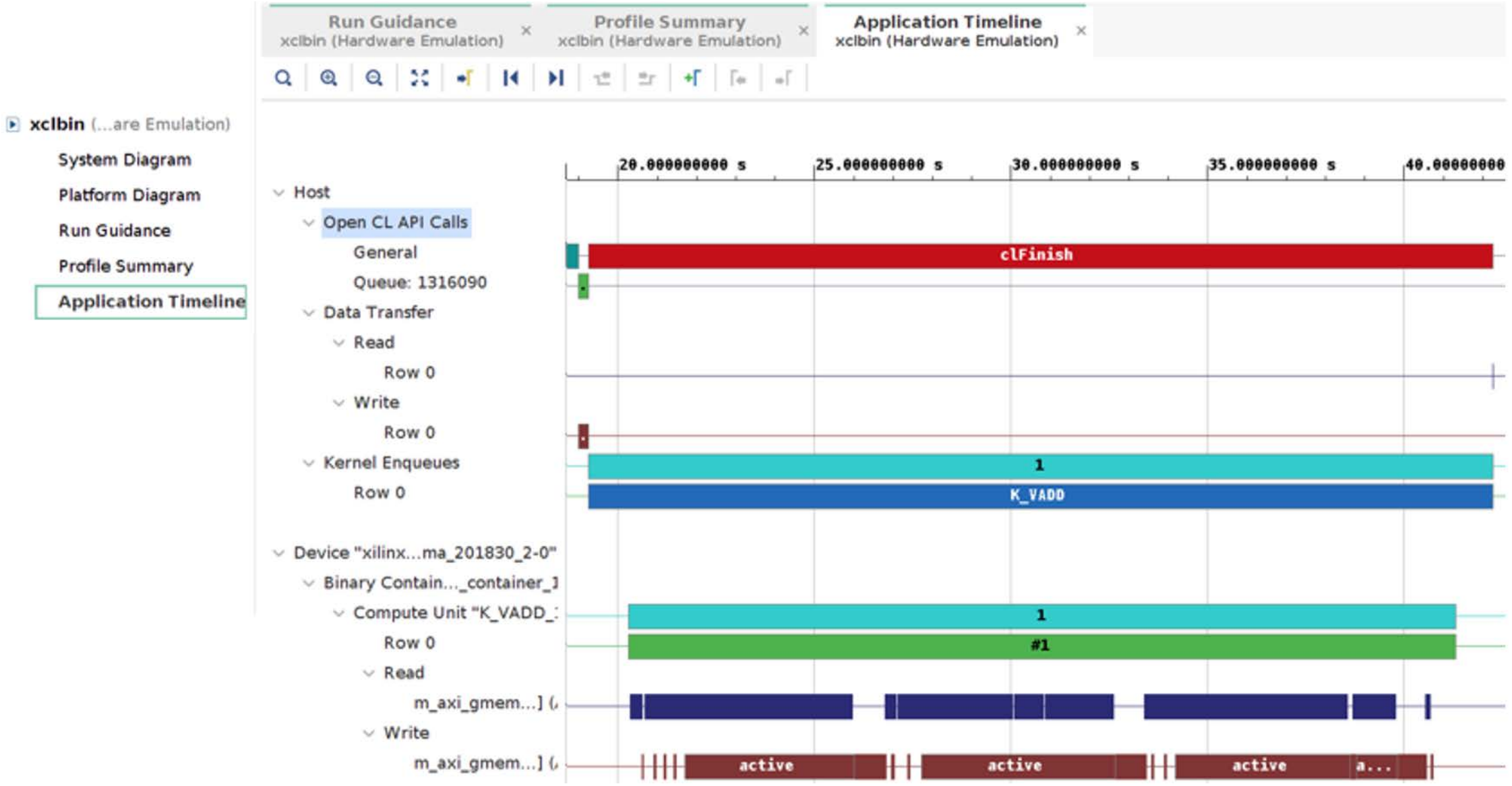
Application Timeline



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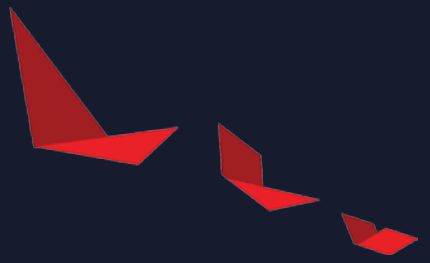
Thank You



Appendix

Profile Summary Report > Kernels & Compute Units

Dataflow Acceleration	Total Time (ms)	Minimum Time (ms)	Average Time (ms)	Maximum Time (ms)	Clock Freq (MHz)	CU Utilization (%)
1.000000x	0.023	0.023	0.023	0.023	300	90.740

Profile Summary Report > Data Transfers (1)

Run Summary
xclbin (Hardware Emulation)

Profile Summary
xclbin (Hardware Emulation)

Top Operations | Kernels & Compute Units | **Data Transfers** | OpenCL APIs

Data Transfer: Host to Global Memory

Context:Number of Devices	Transfer Type	Number Of Buffer Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Buffer Size (KB)	Total Time (ms)	Average Time (ms)
context0:1	READ	1	N/A	N/A	4.096	N/A	N/A
context0:1	WRITE	2	N/A	N/A	4.096	N/A	N/A

Data Transfer: Kernels to Global Memory

Device	Compute Unit/ Port Name	Kernel Arguments	Memory Resources	Transfer Type	Number Of Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Size (KB)	Average Latency (ns)
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A|B|R	DDR[1]	READ	2048	366.478	3.181	0.004	39.700
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A|B|R	DDR[1]	WRITE	64	187.032	1.624	0.064	1159.480

- Host and global memory PCIe transfers
  - Transfer rate, number of transfers
  - Average size of transfer, average bandwidth utilization
  - Average time, total time

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Profile Summary Report > Data Transfers (2)

Run Summary
xclbin (Hardware Emulation)

Profile Summary
xclbin (Hardware Emulation)

Top Operations | Kernels & Compute Units | **Data Transfers** | OpenCL APIs

Data Transfer: Host to Global Memory

Context:Number of Devices	Transfer Type	Number Of Buffer Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Buffer Size (KB)	Total Time (ms)	Average Time (ms)
context0:1	READ	1	N/A	N/A	4.096	N/A	N/A
context0:1	WRITE	2	N/A	N/A	4.096	N/A	N/A

Data Transfer: Kernels to Global Memory

Device	Compute Unit/ Port Name	Kernel Arguments	Memory Resources	Transfer Type	Number Of Transfers	Transfer Rate (MB/s)	Average Bandwidth Utilization (%)	Average Size (KB)	Average Latency (ns)
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A|B|R	DDR[1]	READ	2048	366.478	3.181	0.004	39.700
xilinx_u200_xdma_201830_2-0	K_VADD_1/m_axi_gmem	A|B|R	DDR[1]	WRITE	64	187.032	1.624	0.064	1159.480

- Kernels and global memory transfers
  - Transfer rate, number of transfers
  - Average size of transfer, average bandwidth utilization
  - Average time, total time