

Sri Ramakrishna Engineering College

[Autonomous Institution, ISO 9001-2008 Certified, Approved by AICTE and Affiliated to Anna University, Chennai]

[All eligible courses Accredited by NBA]

Coimbatore-641 022

Two-Day National Workshop on

RF/Wireless System Design Solution from Xilinx

9th & 10th October 2014

REGISTRATION FORM

Name : _____

Designation : _____

Organization : _____

Address : _____

Mobile : _____

E-Mail : _____

Fee Payment Details :

Draft No: _____ Dated : _____

Amount : _____ Bank : _____

(Accommodation is available on chargeable basis if requested)

Signature of
Candidate

Signature of Head of the
Department / Institution

ORGANIZING COMMITTEE

Chief Patrons

Sri.C.Soundararaj – Managing Trustee

Sri.R.VijayaKumhar – Joint Managing Trustee

Patrons

Dr.A.Ebenezer Jeyakumar-Director(Academics)

Dr.N.R.Alamelu- Principal

Convenor

Dr.M.Jagadeeswari, HoD/ECE-PG

Coordinator

Mr.C.S.Manikandababu, AP(Sr.Gr.)/ECE-PG

Co-coordinator

Ms.N.Kirthika, AP/ECE-PG

RESOURCE PERSONS

Ms. Sadiya, National Manager

Mr. Mamidi Nagaraju, Application Engineer, CUP-S

Mr. VidyaSagar M.K., vidyasagar.mk@coreel.com

**University Program, CoreEL Technologies,
Bangalore.** Tel:09972066855.

For further enquiries and communication,

Contact :

The Convenor,

Department of ECE-PG,

**Sri Ramakrishna Engineering College,
Coimbatore – 641 022.**

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Mobile : 99941 58642, 94863 55965

Email id: hod-mevlsi@srec.ac.in

DD Drawn in favor of

The Principal,

Sri Ramakrishna Engineering College,
Payable at Coimbatore.

Important Dates:

Registration form along with D.D should reach us **on or before: 30.09.2014**

Intimation to participant on or before : 04.10.2014



Sri Ramakrishna Engineering
College, Coimbatore-641022.



A Two Day National Workshop

on

RF/Wireless System Design Solution from Xilinx

9th & 10th October 2014



**Organized by
IEEE Student Branch**



&

**Department of Electronics and Communication
Engineering (PG)**

In Association with



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Vattamalaipalayam, NGGO Colony Post, Coimbatore-641022
Tamilnadu, India.

Web: www.srec.ac.in

The Objective

This workshop provides an introduction to the advanced tools you need to design and implement DSP algorithms targeting FPGAs, focuses on learning how to use System Generator for DSP domains, RF and Wireless design flow, IP Core and design implementation tools. Through hands-on exercises, you will be able to Model and Simulate System Generator designs in Simulink Environment and implement RF & Wireless designs from algorithm to Real-time hardware implementation. Emphasis will be provided on real-time processing of models in hardware, Design and Implementation of Filters, ADC / DAC, DUC/DDC, QAM, FFT/DCT, Modulation Techniques and optimize the implementations in FPGA. Design and implementation of OFDM Transceiver for SDR, CDMA, WCDMA and witness the power, ease of use, and design efficiency of Xilinx DSP tools and IP using XUP Virtex-5.

About the Institution

Sri Ramakrishna Engineering College established in the year 1994 by SNR Sons Charitable Trust had grown into an eminent institution in Tamilnadu. The Institution is accredited by National Board of Accreditation (NBA) for all eligible UG & PG courses. The college has been granted Autonomous Status for all UG and PG courses by UGC and Anna University, from 2007. The College campus has an admirable infrastructure with all facilities and state-of-the art laboratories. The college has signed Memorandum of Understanding (MoU), with South Dakota school of Mines and Technology, USA, Kyungpook National University, South Korea for Student and Staff exchange programme. The college has also signed MoU with various reputed industries, to enable the student to be trained in gaining practical knowledge.

About the Department

The Department of ECE (PG) -VLSI Design is recognized as the research center with all computing facilities, State-of-the-art laboratories, and efficient teaching professionals and well stacked department library.

About CoreEL Technologies

CoreEL Technologies (I) Pvt Ltd, CoreEL is a customer Application Specific Products & Solutions company offering Intellectual Property (IP) Hardware, Software & Engineering Services to customers, enabling them to Design Manufacture and Market world class electronic products. The portfolio of offerings include IP cores, Sytem Design, Architecture, Validation, Sustenance, Prototype Manufacturing, Next-Gen products, Semiconductor solutions & Distribution of EDA Tools & COTS products. CoreEL was founded in 1999 and is an ISO 9001:2008 certified headquartered at Bangalore India.

About CoreEL University Program

CoreEL University Program provides eco-system support to Indian Academia in engineering higher education, in the field of embedded systems thereby enabling the delivery of quality education. CoreEL University achieves this by providing state of the art products from XILINX, MENTORGRAPHICS, MATLAB, VxWORKS, Speedgoat, PCB Design Tools, ANALOG Discovery Kit from DIGILENT (Analog Discovery kit can replace the conventional regulated power supply, Function Generator, Oscilloscope with one portable, compact and power effective and low cost solution!) training, update of curriculum, setting up Centers of Excellence in embedded systems arena etc.

Registration Fees

Category	INR
Research Scholars, UG/PG Students & Faculty from Academic Institutions	1000
Participants from Industry / R&D organizations	1500
IEEE Members (Proof for Membership)	800

❖ **No Spot Registration & Registration is restricted to 50 participants only**

Registration fee includes kit, Certificate, Working Lunch, Tea & Snacks.

Course Content

Day I:

Morning Session:

- ✓ The advantages of using FPGAs over traditional processors for DSP designs.
- ✓ Utilize fixed point binary arithmetic and identify how to use this knowledge to create efficient designs in FPGAs.
- ✓ Recognize how both the CLB slices in FPGAs and the more advanced DSP48s are used to implement DSP algorithms.
- ✓ Construct different FIR filter and FFT implementations and how to optimize these implementations in the FPGA.

Afternoon Session:

- ✓ Lab1: Signed Number Conversion, Quantization and Rounding, Adders, subtractors and Accumulation.
- ✓ Lab 2: Filter Implementation, Resource and Performance Estimation.
- ✓ Lab 3: FFT Implementation, Resource and Performance Estimation.

DayII:

Morning Session:

- ✓ Xilinx DSP Design flow and concepts of Hardware co-simulation with Demo design.
- ✓ Construct DUC and QAM Modulation Techniques implementations and how to optimize these implementations in the FPGA.
- ✓ Design & Implementation of OFDM Transceiver for Software Defined Radio (SDR).
- ✓ Design discussions on CDMA, WCDMA and its design Implementation on Hardware.

Afternoon Session:

- ✓ Lab 4: DUC/DDC Design & Implementation using Atlys Sparten6.
- ✓ Lab 5: QAM Design & Implementation on Atlys Sparten6.
- ✓ Lab 6: OFDM Transceiver for Software Defined Radio (SDR) Design & Implementation using XUP Virtex5.