## Registration Form

**Name**

**Department**

**College/University**

**Address for Correspondence**

**Email**

**Phone/Mobile Number**

**Signature**

Dr. Jitendra Kumar Das

Dr. N. K. Rout

S. Padhy

Joy Chowdhury

**Resource Persons:**

Mr. Samik Basu, Zonal Manager-East

Mr. Sharath Kanth, Application Engineer

Mr. Arnob Mallick, Account Manager

**upt@coreel.com**

### Registration Details

Participants are requested to register by filling in the accompanying slip and sending the same/ signed scan copy to the Workshop coordinator in order to reach on or before 19th August, 2015.

### Registration Form to be sent to

Dr. J. K. Das

Associate Professor(I)

School of Electronics Engineering

KIIT University, Bhubaneswar – 751024.

Mobile : +91 9437397714

Email : jkdasfet@kiit.ac.in

**KIIT University,**

**Bhubaneswar-24**

**Two Day Workshop**

**on**

# FPGA Design Flow using Vivado

**21st and 22nd August, 2015**

***Organized by:***

**School of Electronics Engineering**

**In collaboration with**

**Coreel Technologies, Bangalore**

CoreEL Technologies
A CASPS Company

XILINX
ALL PROGRAMMABLE

## Xilinx Vivado Design Flow

### About KIIT University

The KIIT University, Bhubaneswar symbolizes the resurgent Orissa. It is equipped with all modern amenities and has created the environment for the conduct of mega events. Aesthetic campuses of the KIIT University perched in the historic city of Bhubaneswar in idyllic surroundings provide an ambient environment for intellectual pursuit. We at KIIT University are persistently marching ahead to attain excellence both in innovation, quality and quantity of technical and professional education. This University has not only created state-of-the-art infrastructure but also bridges the gap in the area of industry-institute partnership to create a roadmap for the overall development of technical education in India.

### About School of Electronics Engineering

School of electronics Engineering , established in 1998, offers full time four year programs leading to B.Tech degree in Electronics & Telecommunication Engineering, Electronics & Electrical Engineering and Applied Electronics & Instrumentation engineering and two-year program leading to M. Tech Degree in Communication system Engineering, VLSI & Embedded System Engineering and RF and Microwave Engineering. School of Electronics Engineering is equipped with the latest state-of-the-art equipment imparting quality education. It has a term of dynamic and qualified faculty members from elite institutes like IITs, NITs and reputed Universities with proven credentials, which attract quality students from all over the country. The School has a tradition for arranging invited lectures and sponsored projects to bridge the gap between the industry and the Institute.

### About Bhubaneswar

Bhubaneswar, the capital city of Odisha, is also popularly known as the “Temple city of India”. Being the seat of Tribhubaneswar or “Lord Lingaraj “, Bhubaneswar is an important Hindu pilgrimage centre. Hundreds of temples dot the landscape of Old Town, which once boasted of more than 2000 temples. Bhubaneswar is the place where temple building activities of Odishan style flowered from very inception to its fullest culmination extending over a period of over one thousand years. The new Bhubaneswar with its modern buildings and infrastructure perfectly complements its historic surroundings. With facilities to cater to every type of visitors, Bhubaneswar makes an ideal tourist destination.

### About CoreEL Technologies

CoreEL Technologies is a Customer application Specific Product & Solutions (CASPS) company offering innovative solutions from its diverse portfolio of offerings that include Intellectual Property (IP) cores, System Design, Prototype Development, Manufacturing, Sustenance, Next-gen products, Semiconductor solutions, EDA tools, COTS products and Technology Training. CoreEL is a leading developer of advanced electronic system level products and solutions to three primary markets – Aerospace & Defence, Digital Media Broadcast, and Universities & Institutions of higher learning. CoreEL’s products and solutions enable its customers to further add value, create innovative and competitive products for their end users.

### About CoreEL University Program

CoreEL University Program provides Eco-System support to Indian Academia in Engineering Higher Education, in the field of Embedded Systems thereby enabling the delivery of quality education. CoreEL achieves this by providing state of the art products from **XILINX, MENTOR Graphics, MATLAB,** ANSYS, VxWorks, Speedgoat (RCP,HIL simulation & development)**, PCB Design** Tools from Mentor, **VLSI, Embedded Students Training, Faculty Training** etc., with multiyear application engineering support on these products, faculty & student training, providing industry specific inputs to update the curriculum & helping Universities set up Centers of Excellence in Embedded Systems. Arena

### Target Audience

Faculty members and Students from Engineering colleges and Universities

### Important Dates

Last date for Registration : 19/08/2015

### Course Overview:

Day 1:

***7-Series Architecture Overview***

**Lab 1: Vivado Design Flow**

- Use Vivado IDE to create a simple HDL design. Simulate the design using the XSIM HDL simulator available in Vivado design suite. Generate the bitstream and verify in hardware.

***Synthesis Technique***

**Lab 2: Synthesizing a RTL Design**

- Synthesize a design with the default settings as well as other settings changed and observe the effect.
- Implementation and Static Timing Analysis

**Lab 3: Implementing the Design**

- Implement the synthesized design of previous lab, perform timing analysis, generate bitstream, download the bitstream and verify the functionality.

Day 2:

- IP Integrator

**Lab 4: Using the IP Catalog and IP Integrator**

- Use the IP Catalog to generate a clock resource and instantiate in a design. Use IP Integrate to generate a core and instantiate in the design.

- Xilinx Design Constraints

**Lab 5: Xilinx Design Constraints**

- Create a project with I/O Planning type, enter pin locations, and export it to the rtl. Then create the timing constraints and perform the timing analysis.
- Hardware Debugging

**Lab 6: Hardware Debugging**

- Use Mark Debug feature and also available integrated Logic Analyzer(ILA) core (available in IP Catalog) to debug the hardware.