**Advanced Embedded System Design on Zynq Using Vivado Workshop**

**PYNQ-Z1/Z2**

**COURSE DESCRIPTION**

This workshop provides participants the necessary skills to develop complex embedded systems and enable them to improve their designs by using the tools available in Vivado. It also helps developers understand and utilize advanced components of embedded systems design for architecting a complex system in the Zynq™ System on a Chip (SoC).

# Install Xilinx software

Professors may submit the online donation request form at <https://www.xilinx.com/member/forms/registration/xup_donation_request.html> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 10 professional edition.

* Vivado 2018.2 System Edition

1. **Setup hardware**

Connect PYNQ-Z1/Z2

* 1. Set the power supply jumper to USB so the board can be powered up and laboratory assignments can be carried out using single micro-usb cable
  2. Connect micro USB cable between PROG UART port of the board and PC

1. **Install distribution**

Git clone the repository using the following command:

git clone https://github.com/xupgit/Advanced-Embedded-System-Design-Flow-on-Zynq.git

Copy the {board}\_**source** directory in the *c:\xup\adv\_embedded* directory. Create the *c:\xup\adv\_embedded\labs* directory. This is where you will do the labs. The labdocs in markdown format are in the cloned directory. They can also be accessed at <https://github.com/xupgit/Advanced-Embedded-System-Design-Flow-on-Zynq>

1. **For Professors only**

Download the **2018\_2\_zynq\_docs\_source.zip** file using your membership account. Do not distribute them to students or post them on a web site. The **2018\_2\_zynq\_docs\_source.zip** file contains presentations in PowerPoint format for you to use in your classroom

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

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| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| Embedded System Design Review | 11\_embedded\_system\_design\_review.ppt x |
| Lab 1: Building a Complete Embedded System | 11a\_lab1\_intro.pptx  Lab1.docx |
| Advanced Zynq Architecture | 12\_Advanced\_Zynq\_Architecture.pptx |
| System Debugging | 13\_System\_Debugging.pptx |
| Lab 2: Debugging using Vivado Logic Analyzer | 13a\_lab2\_intro.pptx  Lab2.docx |
| Memory Interfacing | 14\_Memory\_Interfacing.pptx |
| Lab 3: Extending Memory Space with Block RAM | 14a\_lab3\_intro.pptx  Lab3.docx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Interrupts | 15\_ Interrupts.pptx |
| Low Latency High Bandwidth | 16\_Low\_Latency\_High\_Bandwidth |
| Lab 4: Direct Memory Access using CDMA | 16a\_lab4\_intro.pptx  Lab4.docx |
| Configuration and Bootloading | 17\_Configuration\_and\_Bootloading.pptx |
| Lab 5: 17\_Configuration\_and\_Bootloading | 17a\_lab5\_into.pptx  Lab5.docx |
| Profiling and Performance Improvement | 18\_Profiling\_and\_Performance\_Improvement.pptx |
| Lab 6: Profiling and Performance Tuning | 18a\_lab6\_intro.pptx  Lab6.docx |

**LAB** **DESCRIPTIONS**

Lab 1 - Create a complete processor system with built-in processor and IP in programmable logic.

Lab 2 - Insert various debug cores to debug/analyze system behavior.

Lab 3 - Instantiate AXI BRAM controller and BRAM to extend address space and run application from it.

Lab 4 - Perform DMA operations between various memories using AXI CDMA controller in polling and interrupt modes.

Lab 5 - Create images to boot off the SD card and QSPI flash. Load previously generated hardware bitstreams and executable and execute desired application.

Lab 6 - Profile an application performing a function both in software and hardware.

1. **Contact XUP**

Send an email to [xup@xilinx.com](mailto:xup@xilinx.com) for questions or comments