Improving Performance Lab

Introduction

This lab introduces various techniques and directives which can be used in Vivado HLS to improve design performance. The design under consideration accepts an image in a (custom) RGB format, converts it to the Y’UV color space, applies a filter to the Y’UV image and converts it back to RGB.

Objectives

After completing this lab, you will be able to:

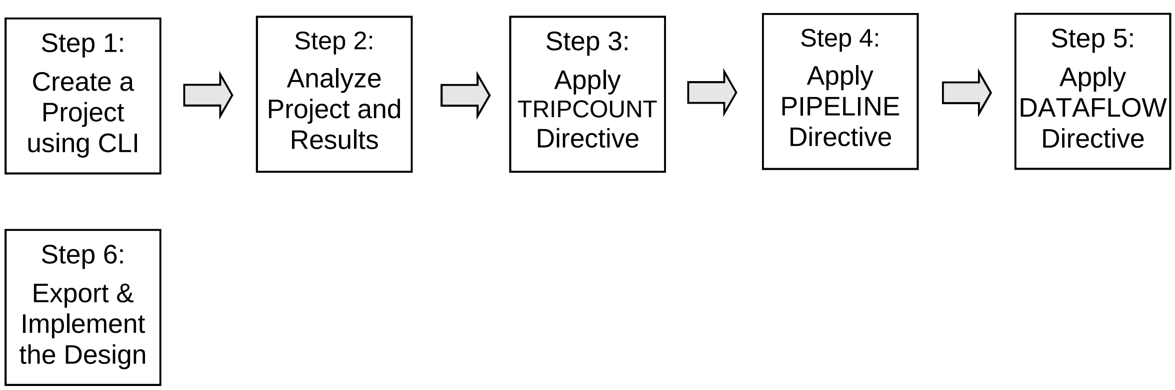
- Add directives in your design
- Understand the effect of INLINE directive
- Improve performance using PIPELINE directive
- Distinguish between DATAFLOW directive and Configuration Command functionality

Procedure

This lab is separated into steps that consist of general overview statements that provide information on the detailed instructions that follow. Follow these detailed instructions to progress through the lab.

This lab comprises 6 primary steps: You will create a new project using Vivado HLS command prompt, analyze the created project and generated solution, turn off inlining and apply the TRIPCOUNT, PIPELINE, and DATAFLOW directives and command configuration, and finally export and implement the design.

General Flow for this Lab



Create a Vivado HLS Project from Command Line Step 1

1-1. Validate your design using Vivado HLS command line window. Create a new Vivado HLS project from the command line.

1-1-1. Launch Vivado HLS: Select **Start > All Programs > Xilinx Design Tools > Vivado 2017.4 > Vivado HLS > Vivado HLS 2017.4 Command Prompt**.

1-1-2. In the Vivado HLS Command Prompt, change directory to **c:\xup\hls\labs\lab2.**

1-1-3. A self-checking program (yuv_filter_test.c) is provided**.** Using that we can validate the design. A Makefile is also provided. Using the Makefile, the necessary source files can be compiled and the compiled program can be executed. You can examine the contents of these files and the project directory. In the Vivado HLS Command Prompt, type **make** to compile and execute the program.

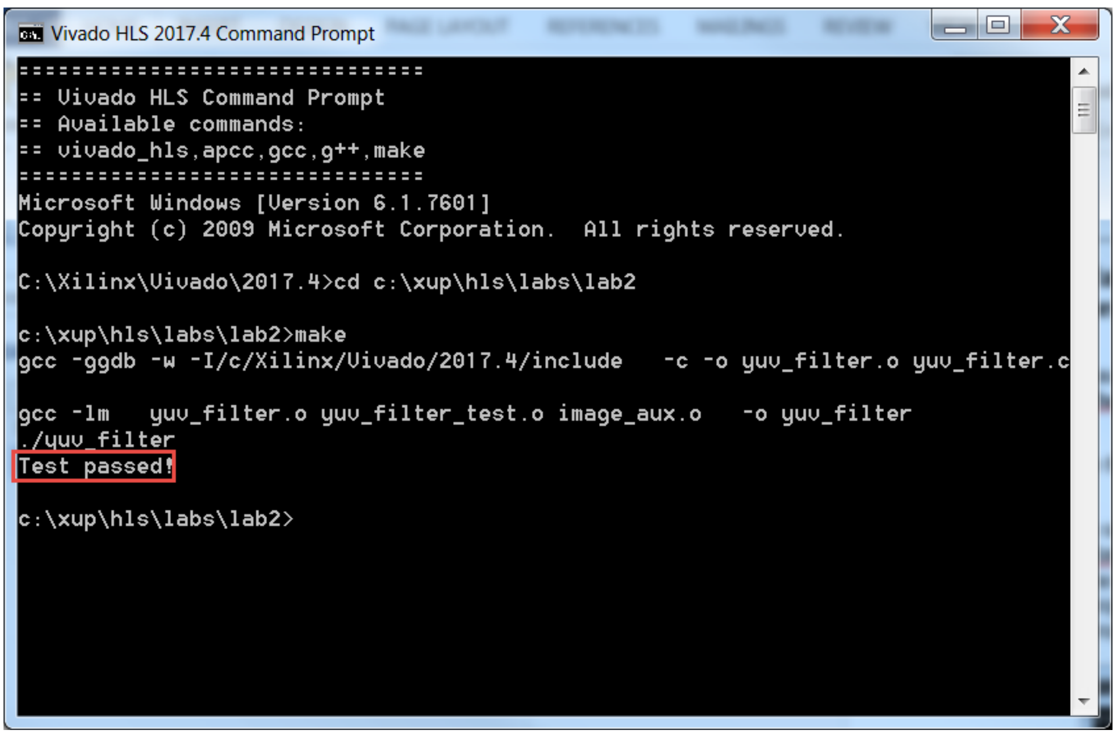


Figure 1. Validating the design

Note that the source files (yuv_filter.c, yuv_filter_test.c, and image_aux.c) were compiled, then yuv_filter executable program was created, and then it was executed. The program tests the design and outputs Test Passed message.

1-1-4. A Vivado HLS tcl script file (yuv_filter.tcl) is provided and can be used to create a Vivado HLS project.

1-1-5. Type **vivado_hls –f zed_yuv_filter.tcl** in the Vivado HLS Command Prompt window to create the project targeting the ZedBoard or type **vivado_hls –f zybo_yuv_filter.tcl** in the Vivado HLS Command Prompt window to create the project targeting the Zybo.

The project will be created and Vivado HLS.log file will be generated.

1-1-6. Open the **vivado_hls.log** file from **c:\xup\hls\labs\lab2** using any text editor and observe the following sections:

- o Creating directory and project called yuv_filter.prj within it, adding design files to the project, setting solution name as solution1, setting target device (Zynq-z020 for ZedBoard or Zynq-z010 for Zybo), setting desired clock period of 10 ns (for ZedBoard) or 8 ns (for Zybo), and importing the design and testbench files (Figure 2).
- o Synthesizing (Generating) the design which involves scheduling and binding of each functions and sub-function (Figure 3).
- o Generating RTL of each function and sub-function in SystemC, Verilog, and VHDL languages (Figure 4).

```

****** Vivado(TM) HLS - High-Level Synthesis from C, C++ and SystemC v2017.4 (64-bit)
  **** SW Build 2086221 on Fri Dec 15 20:55:39 MST 2017
  **** IP Build 2085800 on Fri Dec 15 22:25:07 MST 2017
    ** Copyright 1986-2017 Xilinx, Inc. All Rights Reserved.

source C:/Xilinx/Vivado/2017.4/scripts/vivado_hls/hls.tcl -notrace
INFO: [HLS 200-10] Running 'C:/Xilinx/Vivado/2017.4/bin/unwrapped/win64.o/vivado_hls.exe'
INFO: [HLS 200-10] For user 'parimalp' on host 'xsjparimalp31' (Windows NT_amd64 version 6.1)
INFO: [HLS 200-10] In directory 'C:/xup/hls/labs/lab2'
INFO: [HLS 200-10] Creating and opening project 'C:/xup/hls/labs/lab2/yuv_filter.prj'.
INFO: [HLS 200-10] Adding design file 'yuv_filter.c' to the project
INFO: [HLS 200-10] Adding test bench file 'image_aux.c' to the project
INFO: [HLS 200-10] Adding test bench file 'yuv_filter_test.c' to the project
INFO: [HLS 200-10] Adding test bench file 'test_data' to the project
INFO: [HLS 200-10] Creating and opening solution 'C:/xup/hls/labs/lab2/yuv_filter.prj/solutio
INFO: [HLS 200-10] Cleaning up the solution database.
INFO: [HLS 200-10] Setting target device to 'xc7z020clg484-1'
INFO: [SYN 201-201] Setting up clock 'default' with a period of 10ns.
INFO: [HLS 200-10] Analyzing design file 'yuv_filter.c' ...
INFO: [HLS 200-10] Validating synthesis directives ...
INFO: [HLS 200-111] Finished Checking Pragmas Time (s): cpu = 00:00:01 ; elapsed = 00:00:09 .
INFO: [HLS 200-111] Finished Linking Time (s): cpu = 00:00:01 ; elapsed = 00:00:12 . Memory (
INFO: [HLS 200-10] Starting code transformations ...
```

Figure 2. Creating project and setting up parameters

```
INFO: [HLS 200-10] Starting code transformations ...
INFO: [HLS 200-111] Finished Standard Transforms Time (s): cpu = 00:00:01 ; el
INFO: [HLS 200-10] Checking synthesizability ...
INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:0
INFO: [XFORM 203-602] Inlining function 'yuv_scale' into 'yuv_filter' (yuv_fil
INFO: [XFORM 203-401] Performing if-conversion on hyperblock from (yuv_filter.
INFO: [XFORM 203-11] Balancing expressions in function 'rgb2yuv' (yuv_filter.c
INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:02 ; elapsed
INFO: [HLS 200-111] Finished Architecture Synthesis Time (s): cpu = 00:00:02 ;
INFO: [HLS 200-10] Starting hardware synthesis ...
INFO: [HLS 200-10] Synthesizing 'yuv_filter' ...
INFO: [HLS 200-10] ----------------------------------------------------------
INFO: [HLS 200-42] -- Implementing module 'rgb2yuv'
INFO: [HLS 200-10] ----------------------------------------------------------
INFO: [SCHED 204-11] Starting scheduling ...
WARNING: [SCHED 204-21] Estimated clock period (10.283ns) exceeds the target (
WARNING: [SCHED 204-21] The critical path consists of the following:
    'mul' operation ('tmp_25', yuv_filter.c:57) (3.36 ns)
    'add' operation ('tmp3', yuv_filter.c:57) (3.02 ns)
    'add' operation ('tmp_26', yuv_filter.c:57) (3.9 ns)
INFO: [SCHED 204-11] Finished scheduling.
INFO: [HLS 200-111]  Elapsed time: 15.045 seconds; current allocated memory: 9
INFO: [BIND 205-100] Starting micro-architecture generation ...
INFO: [BIND 205-101] Performing variable lifetime analysis.
INFO: [BIND 205-101] Exploring resource sharing.
INFO: [BIND 205-101] Binding ...
INFO: [BIND 205-100] Finished micro-architecture generation.
INFO: [HLS 200-111]  Elapsed time: 0.105 seconds; current allocated memory: 95
INFO: [HLS 200-10] ----------------------------------------------------------
INFO: [HLS 200-42] -- Implementing module 'yuv2rgb'
INFO: [HLS 200-10] ----------------------------------------------------------
INFO: [SCHED 204-11] Starting scheduling ...
WARNING: [SCHED 204-21] Estimated clock period (10.8454ns) exceeds the target
WARNING: [SCHED 204-21] The critical path consists of the following:
    'mul' operation ('tmp_12', yuv_filter.c:101) (3.36 ns)
    'add' operation ('tmp1', yuv_filter.c:101) (3.02 ns)
    'add' operation ('tmp_14', yuv_filter.c:101) (2.14 ns)
    'icmp' operation ('icmp9', yuv_filter.c:101) (0.959 ns)
    'select' operation ('p_phitmp2', yuv_filter.c:101) (0 ns)
    'select' operation ('G', yuv_filter.c:101) (1.37 ns)
INFO: [SCHED 204-11] Finished scheduling.
```

Figure 3. Synthesizing (Generating) the design

```
INFO: [RTGEN 206-100] Finished creating RTL model for 'yuv_filter'.
INFO: [HLS 200-111]  Elapsed time: 0.623 seconds; current allocated memory: 98.680 MB.
INFO: [RTMG 210-278] Implementing memory 'yuv_filter_p_yuv_hbi_ram (RAM)' using block RAM
INFO: [HLS 200-111] Finished generating all RTL models Time (s): cpu = 00:00:04 ; elapsec
INFO: [SYSC 207-301] Generating SystemC RTL for yuv_filter.
INFO: [VHDL 208-304] Generating VHDL RTL for yuv_filter.
INFO: [VLOG 209-307] Generating Verilog RTL for yuv_filter.
INFO: [HLS 200-112] Total elapsed time: 21.239 seconds; peak allocated memory: 98.680 MB.
INFO: [Common 17-206] Exiting vivado_hls at Tue Feb 13 19:33:43 2018...
```

Figure 4. Generating RTL

1-1-7. Open the created project (in GUI mode) from the Vivado HLS Command Prompt window, by typing **vivado_hls –p yuv_filter.prj**.

The Vivado HLS will open in GUI mode and the project will be opened.

Analyze the Created Project and Results Step 2

2-1. Open the source file and note that three functions are used. Look at the results and observe that the latencies are undefined (represented by ?).

2-1-1. In Vivado HLS GUI, expand the **source** folder in the Explorer view and double-click **yuv_filter.c** to view the content.

- o The design is implemented in 3 functions: `rgb2yuv`, `yuv_scale` and `yuv2rgb`.
- o Each of these filter functions iterates over the entire source image (which has maximum dimensions specified in `image_aux.h`), requiring a single source pixel to produce a pixel in the result image.
- o The scale function simply applies individual scale factors, supplied as top-level arguments to the Y'UV components.
- o Notice that most of the variables are of user-defined (`typedef`) and aggregate (e.g. structure, array) types.
- o Also notice that the original source used `malloc()` to dynamically allocate storage for the internal image buffers. While appropriate for such large data structures in software, `malloc()` is not synthesizable and is not supported by Vivado HLS.
- o A viable workaround is conditionally compiled into the code, leveraging the `__SYNTHESIS__` macro. Vivado HLS automatically defines the `__SYNTHESIS__` macro when reading any code. This ensure the original `malloc()` code is used outside of synthesis but Vivado HLS will use the workaround when synthesizing.

2-1-2. Expand the **syn > report** folder in the Explorer view and double-click **yuv_filter_csynh.rpt** entry to open the synthesis report.

2-1-3. Each of the loops in this design has variable bounds – the width and height are defined by members of input type `image_t`. When variables bounds are present on loops the total latency of the loops cannot be determined: this impacts the ability to perform analysis using reports. Hence, "?" is reported for various latencies.

⊟ **Latency (clock cycles)**

⊟ **Summary**

Latency		Interval		
min	max	min	max	Type
?	?	?	?	none

Figure 5. Latency computation

Apply TRIPCOUNT Pragma Step 3

3-1. Open the source file and uncomment pragma lines, re-synthesize, and observe the resources used as well as estimated latencies. Answer the questions listed in the detailed section of this step.

3-1-1. To assist in providing loop-latency estimates, Vivado HLS provides a TRIPCOUNT directive which allows limits on the variables bounds to be specified by the user. In this design, such directives have been embedded in the source code, in the form of #pragma statements.

3-1-2. Uncomment the #pragma lines (50, 53, 90, 93, 130, 133) to define the loop bounds and save the file.

3-1-3. Synthesize the design by selecting **Solution > Run C Synthesis > Active Solution.** View the synthesis report when the process is completed.

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
841205	51621125	841205	51621125	none

(a) ZedBoard

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
1001205	61451525	1001205	61451525	none

(b) Zybo

Figure 6. Latency computation after applying TRIPCOUNT pragma

3-1-4. Looking at the report, and answer the following question.

Question 1

Estimated clock period: ______________________________

Worst case latency: ______________________________

Number of DSP48E used: ______________________________

Number of BRAMs used: ______________________________

Number of FFs used: ______________________________

Number of LUTs used: ______________________________

3-1-5. Scroll the Console window and note that yuv_scale function is automatically inline into the yuv_filter function.

```
INFO: [HLS 200-10] Checking synthesizability ...
INFO: [HLS 200-111] Finished Checking Synthesizability Time (s): cpu = 00:00:01 ; elapsed = 00:00:11 . Memory (MB): peak = 104.156 ; gain = 47.289
INFO: [XFORM 203-602] Inlining function 'yuv_scale' into 'yuv_filter' (yuv_filter.c:24) automatically.
INFO: [XFORM 203-401] Performing if-conversion on hyperblock from (yuv_filter.c:92:33) to (yuv_filter.c:92:27) in function 'yuv2rgb'... converting 7 basic blocks.
INFO: [XFORM 203-11] Balancing expressions in function 'rgb2yuv' (yuv_filter.c:30)...11 expression(s) balanced.
INFO: [HLS 200-111] Finished Pre-synthesis Time (s): cpu = 00:00:01 ; elapsed = 00:00:12 . Memory (MB): peak = 125.930 ; gain = 69.063
```

Figure 7. Vivado HLS automatically inlining function

3-1-6. Observe that there are three entries – rgb2yuv.rpt, yuv_filter.rpt, and yuv2rgb.rpt under the **syn** report folder in the Explorer view. There is no entry for yuv_scale.rpt since the function was inlined into the yuv_filter function.

You can access lower level module's report by either traversing down in the top-level report under components (under Utilization Estimates > Details > Component) or from the reports container in the project explorer.

3-1-7. Expand the Summary of loop latency and note the latency and trip count numbers for the yuv_scale function. Note that the `YUV_SCALE_LOOP_Y` loop latency is 6X the specified TRIPCOUNT, implying that 6 cycles are used for each of the iteration of the loop.

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
841205	51621125	841205	51621125	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- YUV_SCALE_LOOP_X	240400	14749440	1202 ~ 7682	-	-	200 ~ 1920	no
+ YUV_SCALE_LOOP_Y	1200	7680	6	-	-	200 ~ 1280	no

(a) ZedBoard

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
961205	58993925	961206	58993926	none

Detail

Instance

Loop

	Latency			Initiation Interval			
Loop Name	min	max	Iteration Latency	achieved	target	Trip Count	Pipelined
- YUV_SCALE_LOOP_X	280400	17207040	1402 ~ 8962	-	-	200 ~ 1920	no
+ YUV_SCALE_LOOP_Y	1400	8960	7	-	-	200 ~ 1280	no

(b) Zybo

Figure 8. Loop latency

3-1-8. You can verify this by opening an analysis perspective view, expanding the **YUV_SCALE_LOOP_X** entry, and then expanding the **YUV_SCALE_LOOP_Y** entry.

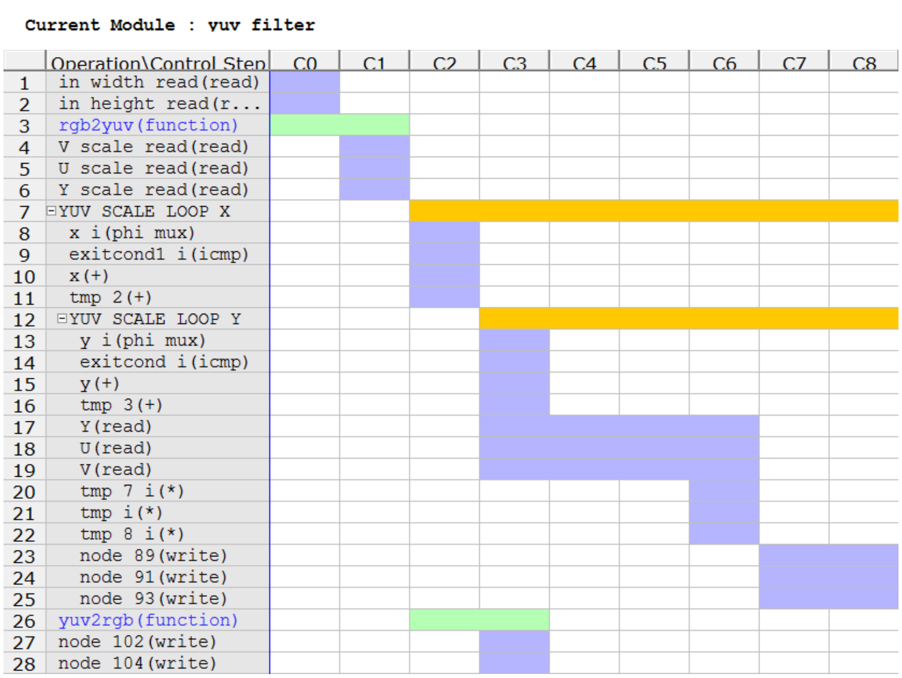


Figure 9. Design analysis view of the YUV_SCALE_LOOP_Y loop

3-1-9. In the report tab, expand **Detail > Instance** section of the *Utilization Estimates* and click on the **grp_rgb2yuv_fu_244** (rgb2yuv) entry to open the report.

3-1-10. Answer the following question pertaining to rgb2yuv function.

Question 2

Estimated clock period: ____________________________

Worst case latency: ____________________________

Number of DSP48E used: ____________________________

Number of FFs used: ____________________________

Number of LUTs used: ____________________________

3-1-11. Similarly, open the yuv2rgb report.

3-1-12. Answer the following question pertaining to yuv2rgb function.

Question 3

Estimated clock period: ____________________________

Worst case latency: ____________________________

Number of DSP48E used: ____________________________

Number of FFs used: ____________________________

Number of LUTs used: ____________________________

3-1-13. For the rgb2yuv function, in case of ZedBoard, the worst case latency is reported as 17207041 clock cycles. The reported latency can be estimated as follows.

- RGB2YUV_LOOP_Y total loop latency = 7 x 1280 = 8960 cycles
- 1 entry and 1 exit clock for loop RGB2YUV_LOOP_Y = 8962 cycles
- RGB2YUV_LOOP_X loop body latency = 10242 cycles
- RGB2YUV_LOOP_X total loop latency = 8962 x 1920 =17207040 cycles
- 1 exit clock for the loop = 17207041 cycle

3-1-14. For the rgb2yuv function, in case of ZYBO, the worst case latency is reported as 2212241 clock cycles. The reported latency can be estimated as follows.

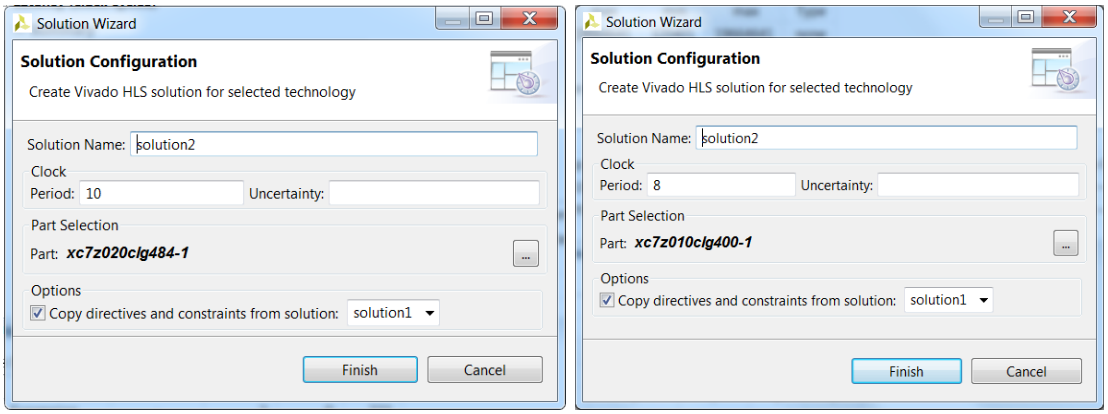
- RGB2YUV_LOOP_Y total loop latency = 9 x 1280 = 11520 cycles
- 1 entry and 1 exit clock for loop RGB2YUV_LOOP_Y = 11522 cycles
- RGB2YUV_LOOP_X loop body latency = 11522 cycles
- RGB2YUV_LOOP_X total loop latency = 11522 x 1920 =2212240 cycles
- 1 exit clock for the loop = 2212241 cycles

Turn OFF INLINE and Apply PIPELINE Directive Step 4

4-1. Create a new solution by copying the previous solution settings. Prevent the automatic INLINE and apply PIPELINE directive. Generate the solution and understand the output.

4-1-1. Select **Project > New Solution** or click on ( ) from the tools bar buttons.

4-1-2. A *Solution Configuration* dialog box will appear. Note that the check boxes of *Copy existing directives from solution* and *Copy custom constraints directives from solution* are checked with Solution1 selected. Click the **Finish** button to create a new solution with the default settings.



(a) ZedBoard **(b) Zybo**

Figure 10. Creating a new Solution after copying the existing solution

4-1-3. Make sure that the **yuv_filter.c** source is opened and visible in the information pane, and click on the **Directive** tab.

4-1-4. Select function **yuv_scale** in the directives pane, right-click on it and select *Insert Directive...*

4-1-5. Click on the drop-down button of the *Directive* field. A pop-up menu shows up listing various directives. Select **INLINE** directive.

4-1-6. In the *Vivado HLS Directive Editor* dialog box, click on the **off** option to turn OFF the automatic inlining. Make sure that the Directive File is selected as destination. Click **OK**.

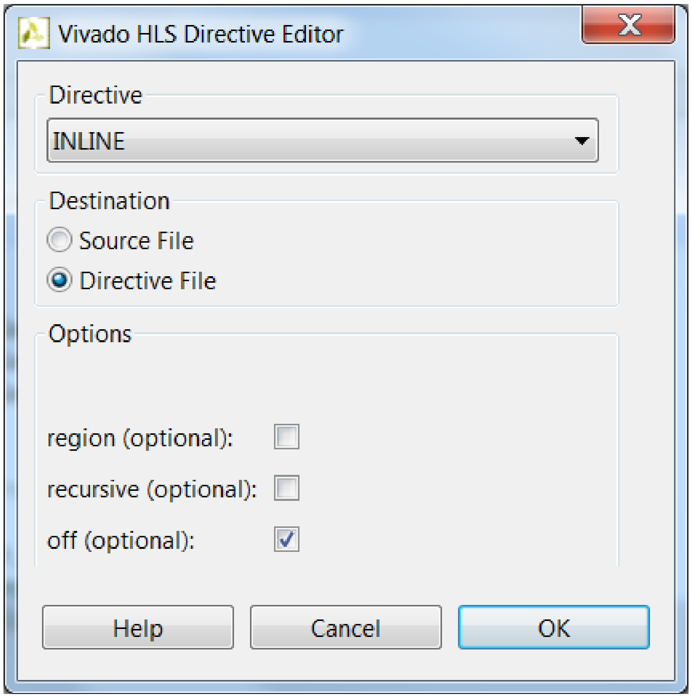


Figure 11. Turning OFF the inlining function

- o When an object (function or loop) is pipelined, all the loops below it, down through the hierarchy, will be automatically unrolled.
- o In order for a loop to be unrolled it must have fixed bounds: all the loops in this design have variable bounds, defined by an input argument variable to the top-level function.
- o Note that the TRIPCOUNT directive on the loops only influences reporting, it does not set bounds for synthesis.
- o Neither the top-level function nor any of the sub-functions are pipelined in this example.
- o The pipeline directive must be applied to the inner-most loop in each function – the inner-most loops have no variable-bounded loops inside of them which are required to be unrolled and the outer loop will simply keep the inner loop fed with data

4-1-7. Expand the *yuv_scale* in the Directives tab, right-click on *YUV_SCALE_LOOP_Y* object and select insert directives …, and select **PIPELINE** as the directive.

4-1-8. Leave **II** (Initiation Interval) blank as Vivado HLS will try for an II=1, one new input every clock cycle.

4-1-9. Click **OK**.

4-1-10. Similarly, apply the PIPELINE directive to *YUV2RGB_LOOP_Y* and *RGB2YUV_LOOP_Y* objects. At this point, the Directive tab should look like as follows.

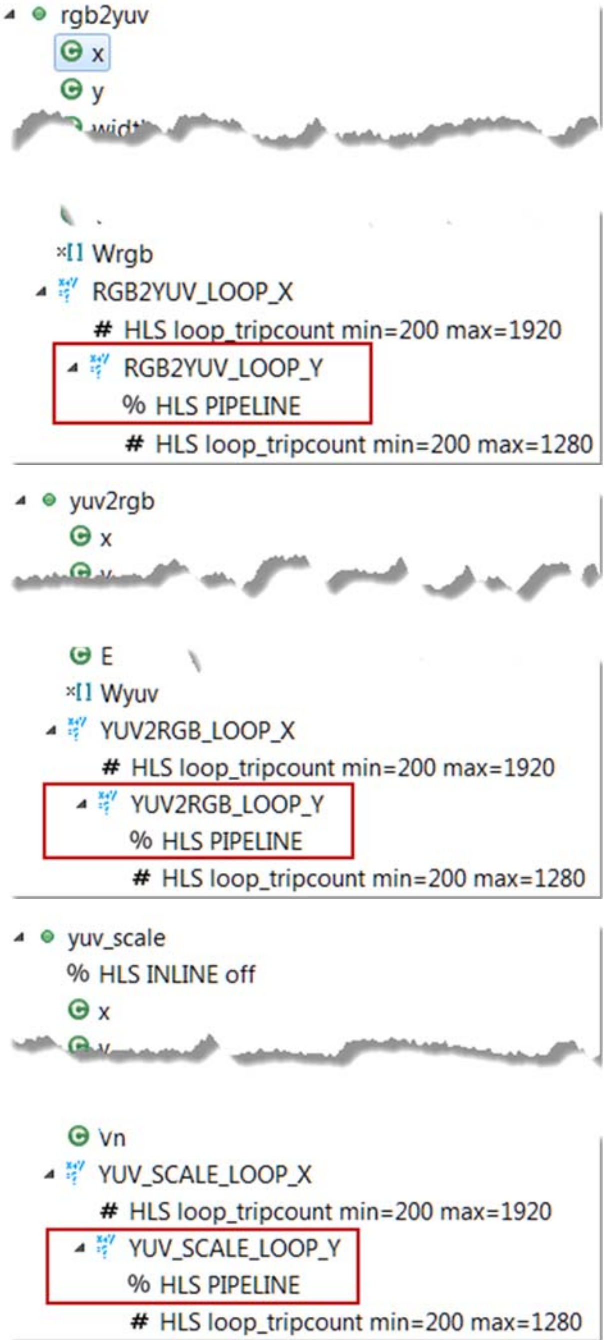


Figure 12. PIPELINE directive applied

4-1-11. Click on the **Synthesis** button.

4-1-12. When the synthesis is completed, select **Project > Compare Reports…** or click on to compare the two solutions.

4-1-13. Select *Solution1* and *Solution2* from the **Available Reports,** and click on the **Add>>** button.

4-1-14. Observe that the latency reduced from 51621125 to 7372828 (ZedBoard), and 61451525 to 7372835 (ZYBO) clock cycles.

All Compared Solutions

solution2: xc7z020clg484-1

solution1: xc7z020clg484-1

Performance Estimates

Timing (ns)

Clock		solution2	solution1
ap_clk	Target	10.00	10.00
	Estimated	10.85	10.85

Latency (clock cycles)

		solution2	solution1
Latency	min	120028	841205
	max	7372828	51621125
Interval	min	120028	841205
	max	7372828	51621125

(a) ZedBoard

All Compared Solutions

solution2: xc7z010clg400-1

solution1: xc7z010clg400-1

Performance Estimates

Timing (ns)

Clock		solution2	solution1
ap_clk	Target	8.00	8.00
	Estimated	9.63	8.71

Latency (clock cycles)

		solution2	solution1
Latency	min	120035	1001205
	max	7372835	61451525
Interval	min	120035	1001205
	max	7372835	61451525

(b) Zybo

Figure 13. Performance comparison after pipelining

In Solution1, the total loop latency of the inner-most loop was loop_body_latency x loop iteration count, whereas in Solution2 the new total loop latency of the inner-most loop is loop_body_latency + loop iteration count.

4-1-15. Scroll down in the comparison report to view the resources utilization. Observe that the FFs, LUTs, and DSP48E utilization increased whereas BRAM remained same.

Utilization Estimates

	solution2	solution1
BRAM_18K	12288	12288
DSP48E	9	6
FF	1297	688
LUT	2051	1482

(a) ZedBoard

Utilization Estimates

	solution2	solution1
BRAM_18K	12288	12288
DSP48E	9	6
FF	1593	785
LUT	2083	1494

(b) Zybo

Figure 14. Resources utilization after pipelining

Apply DATAFLOW Directive and Configuration Command Step 5

5-1. Create a new solution by copying the previous solution (Solution2) settings. Apply DATAFLOW directive. Generate the solution and understand the output.

5-1-1. Select **Project > New Solution** or click on ( ) from the tools bar buttons.

5-1-2. A *Solution Configuration* dialog box will appear. Click the **Finish** button (with copy from Solution2 selected).

5-1-3. Close all inactive solution windows by selecting **Project > Close Inactive Solution Tabs.**

5-1-4. Make sure that the *yuv_filter.c* source is opened in the information pane and select the Directive tab.

5-1-5. Select function **yuv_filter** in the directives pane, right-click on it and select *Insert Directive...*

5-1-6. A pop-up menu shows up listing various directives. Select **DATAFLOW** directive and click **OK**.

5-1-7. Click on the **Synthesis** button.

5-1-8. When the synthesis is completed, the synthesis report is automatically opened.

5-1-9. Observe additional information, Dataflow Type, in the Performance Estimates section is mentioned.

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	10.00	11.02	1.25

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
120025	7372825	40009	2457609	dataflow

(a) ZedBoard

Performance Estimates

Timing (ns)

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	8.00	9.63	1.00

Latency (clock cycles)

Summary

Latency		Interval		
min	max	min	max	Type
120031	7372831	40011	2457611	dataflow

(b) Zybo

Figure 15. Performance estimate after DATAFLOW directive applied

- The Dataflow pipeline throughput indicates the number of clocks cycles between each set of inputs reads. If this throughput value is less than the design latency it indicates the design can start processing new inputs before the currents input data are output.
- While the overall latencies haven't changed significantly, the dataflow throughput is showing that the design can achieve close to the theoretical limit (1920x1280 = 2457600) of processing one pixel every clock cycle.

5-1-10. Scrolling down into the Utilization Estimates, observe that the number of BRAMs required has doubled. This is due to the default dataflow ping-pong buffering.

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	200
FIFO	0	-	35	172
Instance	0	11	1188	1834
Memory	12288	-	96	0
Multiplexer	-	-	-	90
Register	-	-	10	-
Total	12288	11	1329	2296
Available	280	220	106400	53200
Utilization (%)	4388	5	1	4

(a) ZedBoard

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	200
FIFO	0	-	35	172
Instance	0	11	1426	1834
Memory	12288	-	96	0
Multiplexer	-	-	-	90
Register	-	-	10	-
Total	12288	11	1567	2296
Available	120	80	35200	17600
Utilization (%)	10240	13	4	13

(b) Zybo

Figure 16. Resource estimate with DATAFLOW directive applied

- When DATAFLOW optimization is performed, memory buffers are automatically inserted between the functions to ensure the next function can begin operation before the previous function has finished. The default memory buffers are ping-pong buffers sized to fully accommodate the largest producer or consumer array.
- Vivado HLS allows the memory buffers to be the default ping-pong buffers or FIFOs. Since this design has data accesses which are fully sequential, FIFOs can be used. Another advantage to using FIFOs is that the size of the FIFOs can be directly controlled (not possible in ping-pong buffers where random accesses are allowed).

5-1-11. The memory buffers type can be selected using Vivado HLS Configuration command.

5-2. Apply Dataflow configuration command, generate the solution, and observe the improved resources utilization.

5-2-1. Select **Solution > Solution Settings…** or click on to access the configuration command settings.

5-2-2. In the *Configuration Settings* dialog box, select **General** and click the **Add…** button.

5-2-3. Select *config_dataflow* as the command using the drop-down button and **fifo** as the default_channel. Enter **2** as the fifo_depth. Click **OK**.

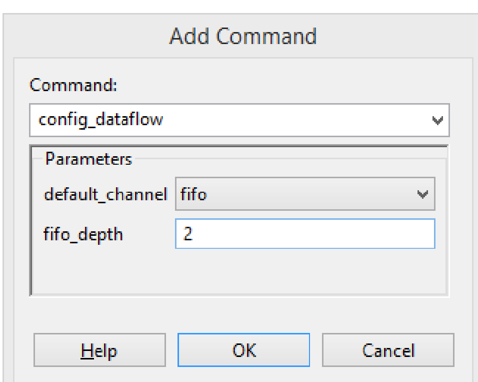


Figure 17. Selecting Dataflow configuration command and FIFO as buffer

5-2-4. Click **OK** again.

5-2-5. Click on the **Synthesis** button.

5-2-6. When the synthesis is completed, the synthesis report is automatically opened.

5-2-7. Note that the performance parameter has not changed; however, resource estimates show that the design is not using any BRAM and other resources (FF, LUT) usage has also reduced.

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	8
FIFO	0	-	65	292
Instance	0	11	855	1786
Memory	-	-	-	-
Multiplexer	-	-	-	-
Register	-	-	-	-
Total	0	11	920	2086
Available	280	220	106400	53200
Utilization (%)	0	5	~0	3

(a) ZedBoard

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT
DSP	-	-	-	-
Expression	-	-	0	8
FIFO	0	-	65	292
Instance	0	11	1116	1818
Memory	-	-	-	-
Multiplexer	-	-	-	-
Register	-	-	-	-
Total	0	11	1181	2118
Available	120	80	35200	17600
Utilization (%)	0	13	3	12

(b) Zybo

Figure 18. Resource estimation after Dataflow configuration command

Export and Implement the Design in Vivado HLS — Step 6

6-1. In Vivado HLS, export the design, selecting VHDL as a language, and run the implementation by selecting Evaluate option.

6-1-1. In Vivado HLS, select **Solution > Export RTL** or click on the button to open the dialog box so the desired implementation can be run.

An Export RTL Dialog box will open.

6-1-2. Click on the drop-down button of the **Evaluate Generated RTL** field and select **VHDL** as the language and click on the Vivado synthesis, place and route check box underneath.

6-1-3. Click **OK** and the implementation run will begin. You can observe the progress in the Vivado HLS Console window. When the run is completed the implementation report will be displayed in the information pane.

Export Report for 'yuv_filter'

General Information

Report date:	Wed Feb 14 07:41:30 -0800 2018
Project:	yuv_filter.prj
Solution:	solution3
Device target:	xc7z020clg484-1
Implementation tool:	Xilinx Vivado v.2017.4

Resource Usage

	VHDL
SLICE	315
LUT	782
FF	700
DSP	11
BRAM	0
SRL	68

Final Timing

	VHDL
CP required	10.000
CP achieved post-synthesis	8.918
CP achieved post-implementation	9.227

Timing met

(a) ZedBoard

Export Report for 'yuv_filter'

General Information

Report date:	Sat Feb 24 08:37:33 -0800 2018
Project:	yuv_filter.prj
Solution:	solution4
Device target:	xc7z010clg400-1
Implementation tool:	Xilinx Vivado v.2017.4

Resource Usage

	VHDL
SLICE	340
LUT	772
FF	826
DSP	11
BRAM	0
SRL	69

Final Timing

	VHDL
CP required	8.000
CP achieved post-synthesis	7.158
CP achieved post-implementation	7.099

Timing met

(b) Zybo

Figure 19. Implementation results in Vivado HLS

Note that the implementation was successful in case of ZedBoard but failed in case of Zybo.

6-1-4. Close Vivado HLS by selecting **File > Exit.**

Conclusion

In this lab, you learned that even though this design could not be pipelined at the top-level, a strategy of pipelining the individual loops and then using dataflow optimization to make the functions operate in parallel was able to achieve the same high throughput, processing one pixel per clock. When DATAFLOW directive is applied, the default memory buffers (of ping-pong type) are automatically inserted between the functions. Using the fact that the design used only sequential (streaming) data accesses allowed the costly memory buffers associated with dataflow optimization to be replaced with simple 2 element FIFOs using the Dataflow command configuration.

Answers

1. Answer the following questions for yuv_filter:

Estimated clock period:	10.85 ns (ZedBoard) 8.71 ns (Zybo)
Worst case latency:	51621125 (ZedBoard) 61451525 (Zybo) clock cycles
Number of DSP48E used:	6
Number of BRAMs used:	12288
Number of FFs used:	688 (ZedBoard) 785 (Zybo)
Number of LUTs used:	1482 (ZedBoard) 1494 (Zybo)

2. Answer the following questions rgb2yuv:

Estimated clock period:	10.28 ns (ZedBoard) 6.42 ns (Zybo)
Worst case latency:	17207041 (ZedBoard) 22122241 (Zybo) clock cycles
Number of DSP48E used:	3
Number of FFs used:	203 (ZedBoard) 249 (Zybo)
Number of LUTs used:	514 (ZedBoard) 520 (Zybo)

3. Answer the following questions for yuv2rgb:

Estimated clock period:	10.85 ns (ZedBoard) 8.71 ns (Zybo)
Worst case latency:	19664641 (ZedBoard) 22122241 (Zybo) clock cycles
Number of DSP48E used:	3
Number of FFs used:	195 (ZedBoard) 221 (Zybo)
Number of LUTs used:	438 (ZedBoard) 441 (Zybo)