**System Design on Zynq using SDx**

**ZYBO**

**COURSE DESCRIPTION**

This course provides professors with hands-on experience of creating application-specific systems on chip from C/C++ programs using the SDx development environment.

# Install Xilinx software

Professors may submit the online donation request form at <https://www.xilinx.com/support/university/donation-program.html> to obtain the latest Xilinx software. The workshop was tested on a PC running Microsoft Windows 7 professional edition.

* SDx 2017.2

1. **Setup hardware**

Connect ZYBO

* 1. Set the power supply jumper to USB so the board can be powered up and laboratory assignments can be carried out using single micro-usb cable
  2. Connect micro USB cable between PROG UART port of ZYBO and PC

You will also need Micro-SD card adaptor and a SD card writer

1. **Install distribution**

Extract the **2017\_2\_zybo\_source.zip** file in the *c:\xup\SDSoC* directory. This will create a **source** folder. Create the *c:\xup\SDSoC\labs* directory. This is where you will do the labs. The **2017\_2\_zynq\_labdocs\_pdf.zip** file consists of lab documents in the PDF format. Extract this zip file in *c:\xup\SDSoC* directory or any other directory of your choice.

Download the zybo.zip file and extract it in the **<SDSoC\_2017\_2\_install\_dir>\2017.2\ Vivado\data\boards\board\_files.** This directory is the board files directory and having it in the specified directory will allow you to select Zybo board during the design creation.

1. **For Professors only**

Download the **2017\_2\_zynq\_docs\_source.zip** file using your membership account. Do not distribute them to students or post them on a web site. The **2017\_2\_zynq\_docs\_source.zip** file contains lab documents in Microsoft Word and presentations in PowerPoint format for you to use in your classroom.

1. **Get Started**

Review the presentation slides (see course agenda) and step through the lab exercises (see lab descriptions) to complete the labs.

# COURSE AGENDA

|  |  |
| --- | --- |
| **Day 1 Agenda** | **Day 1 Materials** |
| Class Intro | 01\_class\_intro.pptx |
| Zynq Architecture and Vivado IPI | 11\_Zynq\_Architecture\_and\_Vivado\_IPI.ppt x |
| SDSoC Overview | 12\_SDSoC\_Overview.pptx |
| Lab 1: Creating a System with SDSoC | lab1.docx |
| Data Motion Networks | 13\_DataMotion\_and\_Optimization.pptx |
| Lab 2: Pragmas and Data Motion Networks | lab2.docx |
| Coding Considerations | 14\_Coding\_Considerations |
| Profiling | 15\_Profiling |
| Lab 3: Profiling Application and Create Accelerators | lab3.docx |
| **Day 2 Agenda** | **Day 2 Materials** |
| Estimation and Events Tracing | 21\_Estimation\_and\_Events\_Tracing.pptx |
| Lab 4: Estimating Accelerator Performance and Events Tracing | lab4.docx |
| Debugging | 22\_Debugging.pptx |
| Lab 5: Debugging | lab5.docx |
| Using C-Callable Libraries and Creating Multiple Accelerators | 23\_C\_Callable\_Multiple\_Accelerators.pptx |
| Improving Performance with Vivado\_HLS | 24\_Vivado\_HLS |
| Lab 6: Fine-Tuning with Vivado | lab6.docx |
| SDSoC Platform | 25\_Platform\_Creation.pptx |
| Lab 7: Creating and Using Platform for an Application | lab7.docx |

**LAB** **DESCRIPTIONS**

Lab 1- Go through the process of using SDSoC to create a new project using available templates.

Lab 2 - Handling data movements between the software and hardware accelerators using various pragmas and SDSoC API.

Lab 3 - Profiling an application, analyzing the results, identifying function(s) for hardware implementation.

Lab 4 - Estimating the expected performance of an application when functions are targeted in hardware, without going through the entire build cycle.

Lab 5 - Debugging software application targeting Standalone and Linux OS in SDSoC.

Lab 6 - Using various techniques and directives of Vivado HLS which can be used in SDSoC to improve design performance.

Lab 7 - Creating a custom platform for an audio application.

1. **Contact XUP**

Send an email to [xup@xilinx.com](mailto:xup@xilinx.com) for questions or comments