Versal ACAP PCB Design

User Guide

UG863 (v1.0) November 24, 2020

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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
11/24/2020 Version 1.0	
Initial release.	N/A

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Chapter 1

Overview

Introduction to Versal ACAP

Versal™ adaptive compute acceleration platforms (ACAPs) combine Scalar Engines, Adaptable Engines, and Intelligent Engines with leading-edge memory and interfacing technologies to deliver powerful heterogeneous acceleration for any application. Most importantly, Versal ACAP hardware and software are targeted for programming and optimization by data scientists and software and hardware developers. Versal ACAPs are enabled by a host of tools, software, libraries, IP, middleware, and frameworks to enable all industry-standard design flows.

Built on the TSMC 7 nm FinFET process technology, the Versal portfolio is the first platform to combine software programmability and domain-specific hardware acceleration with the adaptability necessary to meet today's rapid pace of innovation. The portfolio includes six series of devices uniquely architected to deliver scalability and AI inference capabilities for a host of applications across different markets—from cloud—to networking—to wireless communications—to edge computing and endpoints.

The Versal architecture combines different engine types with a wealth of connectivity and communication capability and a network on chip (NoC) to enable seamless memory-mapped access to the full height and width of the device. Intelligent Engines are SIMD VLIW AI Engines for adaptive inference and advanced signal processing compute, and DSP Engines for fixed point, floating point, and complex MAC operations. Adaptable Engines are a combination of programmable logic blocks and memory, architected for high-compute density. Scalar Engines, including Arm® Cortex™-A72 and Cortex-R5F processors, allow for intensive compute tasks.

The Versal AI Core series delivers breakthrough AI inference acceleration with AI Engines that deliver over 100x greater compute performance than current server-class of CPUs. This series is designed for a breadth of applications, including cloud for dynamic workloads and network for massive bandwidth, all while delivering advanced safety and security features. AI and data scientists, as well as software and hardware developers, can all take advantage of the high-compute density to accelerate the performance of any application.

The Versal Prime series is the foundation and the mid-range of the Versal platform, serving the broadest range of uses across multiple markets. These applications include 100G to 200G networking equipment, network and storage acceleration in the Data Center, communications test equipment, broadcast, and aerospace & defense. The series integrates mainstream 58G transceivers and optimized I/O and DDR connectivity, achieving low-latency acceleration and performance across diverse workloads.

The Versal Premium series provides breakthrough heterogeneous integration, very high-performance compute, connectivity, and security in an adaptable platform with a minimized power and area footprint. The series is designed to exceed the demands of high-bandwidth, compute-intensive applications in wired communications, data center, test & measurement, and other applications. Versal Premium series ACAPs include 112G PAM4 transceivers and integrated blocks for 600G Ethernet, 600G Interlaken, PCI Express® Gen5, and high-speed cryptography.

The Versal architecture documentation suite is available at: https://www.xilinx.com/versal.

Navigating Content by Design Process

Xilinx® documentation is organized around a set of standard design processes to help you find relevant content for your current development task. This document covers the following design processes:

- **System and Solution Planning:** Identifying the components, performance, I/O, and data transfer requirements at a system level. Includes application mapping for the solution to PS, PL, and AI Engine. Topics in this document that apply to this design process include:
  - Chapter 5: Migration between Versal Devices and Packages
- **Board System Design:** Designing a PCB through schematics and board layout. Also involves power, thermal, and signal integrity considerations. Topics in this document that apply to this design process include:
  - Decoupling Capacitor Methodology
  - Recommended Decoupling Capacitor Quantities for Versal AI Core Series
  - Chapter 3: PCB Guidelines for Memory Interfaces
  - Chapter 4: PCB Guidelines for PS, PMC, MIPI, and GTY/GTYP Transceiver Interfaces

PCB Design Features

The PCB guidelines in this document cover two primary areas:

- Power distribution:
  - Current step loads and device utilization
  - Recommended PCB decoupling capacitor quantities
  - Capacitor specification requirements
- Memory interface routing:
  - Required routing guidelines for all memory interfaces
  - DDR4
  - LPDDR4/4x
  - RLDRAM3
  - QDR-IV

Differences from Previous Generations

The Versal architecture PCB guidelines have been streamlined from prior generations to be more accessible to PCB layout professionals as well as hardware designers. Some examples of this streamlining are:

- Assumptions used in determining PCB capacitor quantities are better explained
- Memory routing guidelines are geared specifically for PCB layout professionals, with easy-to-find guidelines and specific constraint definitions

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Chapter 2

Power Distribution System in Versal ACAPs

Introduction

This chapter documents the power distribution system (PDS) for Versal ACAPs, including various power management scenarios and obtaining decoupling quantities via the Xilinx Power Estimator (XPE) tool.

For additional resources regarding board design planning, refer to the Board and Device Planning chapter of *Versal ACAP Hardware, IP, and Platform Development Methodology Guide* (UG1387).

Versal ACAP Power Rails

Versal ACAPs contain a number of power rails that each serve a specific function, as shown in the following table. Refer to *Versal AI Core Series Data Sheet: DC and AC Switching Characteristics* (DS957) for the most current information regarding supply names and voltage levels.

Table 1: **Primary Versal ACAP Power Supplies**

Power Rail	Voltage (V)	Circuitry Powered
Core Rails		
VCCINT	0.70/0.80/0.88	Logic, AI Engine, Clocking, Block RAM/ UltraRAM, DSP, GTY, I/O
VCC_RAM	0.80/0.88	Block RAM/UltraRAM, Clocking
VCC_SOC	0.80/0.88	Network-on-Chip (NOC), Memory Controller
VCC_IO	0.80/0.88	I/O
Auxiliary		
VCCAUX	1.50	AI Engine, Clocking, I/O
Platform Management Controller (PMC)		
VCC_PMC	0.88	PMC

Table 1: **Primary Versal ACAP Power Supplies** *(cont'd)*

Power Rail	Voltage (V)	Circuitry Powered
VCCO_500, VCCO_501	1.80 to 3.30	PMC MIO
VCCO_503	1.80 to 3.30	PMC Dedicated Pins
VCCAUX_PMC	1.50	PMC
VCCAUX_SMON	1.50	PMC
Processing System (PS)		
VCC_PSFP	0.70/0.80/0.88	PS Full Power
VCC_PSLP	0.70/0.80/0.88	PS Low Power
VCCO_502	1.80 to 3.30	LPD MIO
I/O		
VCCO (multiple)	0.6 to 3.30	XPIO, HDIO
GTY		
MGTYAVCC	0.88	GTY/GTYP
MGTYAVTT	1.20	GTY/GTYP
MGTYVCCAUX	1.50	GTY/GTYP

Power Management Scenarios

While it is possible to power each rail with its own voltage regulator module (VRM), it can be beneficial both cost-wise and area-wise to consolidate power rails that share the same voltage. Xilinx has defined two power management scenarios that can be used depending on design needs. These power management scenarios are further defined into sub-categories depending on the core voltage and whether or not the processing system (PS) is powered at a higher voltage.

- **Minimum Rails:** This category aims to reduce the amount of regulators and unique power rails on the board. This saves on complexity, component count, and board space at the expense of reduced flexibility in regards to powering individual rails.
- **Full Power Management:** This category allows for the greatest flexibility in regards to powering individual rails, resulting in power savings, though with increased complexity, component count, and board space.

The following subsections describe each supported power management scenario, including the sequencing requirements, rail groupings, voltage values, and voltage tolerances. The Xilinx Power Estimator (XPE) tool also contains this information with the additions of graphical images for all of the scenarios. XPE is intended be used along with user power estimation to ensure the most robust power system design.

Table 2: **Power Management Scenarios for Versal Devices**

Power Management Scenario	Minimum Supplies Required	Description
Minimum Rails, Low Voltage	7	For use with -L devices (VCCINT @ 0.70V)
Minimum Rails, Low Voltage, PS Overdrive	8	For use with -L devices (VCCINT @ 0.70V) and PS rails VCC_PSFP and VCC_PSLP @ 0.88V
Minimum Rails, Mid/High Voltage	6	All core supplies powered with a single 0.80V (-M) or 0.88V (-H) supply
Full Power Management, Low Voltage	15	For use with -L devices (VCCINT @ 0.70)
Full Power Management, Low Voltage, PS Overdrive	15	For use with -L devices (VCCINT @ 0.70). All core and PS rails powered with individual supplies. PS rails powered at either 0.80V or 0.88V.
Full Power Management, Mid/High Voltage	14	All core and PS rails powered with individual 0.80V or 0.88V supplies

***Note*:** The Versal ACAP data sheets express the voltage tolerances for each rail with minimum, typical, and maximum values. These values take into consideration the typical DC regulator tolerances (usually 1%) as well as an allowable AC ripple noise due to switching activity. In the following tables, the voltage tolerances are divided into those two categories with the AC ripple of 17 mV specifically called out for the core rails.

Minimum Rails, Low Voltage

This scenario utilizes a minimum number of power rails along with the lowest possible core voltage of 0.70V. This scenario can be selected in XPE by choosing a -L device (VCCINT=0.70V).

Table 3: **Power Supply Groupings for Minimum Rails, Low Voltage Scenario**

Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
1	VCCINT, VCC_PSFP, VCC_PSLP, VCC_PMC, VCC_CPM5 (when present)	0.70	1%	±17 mV
2	VCC_RAM, VCC_SOC, VCC_IO, VCCINT_GT (when present)	0.80	1%	±17 mV
3	VCCAUX, VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%
4	MGTYAVCC	0.88	2%	10 mV pk-pk[2]
5	MGTYVCCAUX	1.50	2%	10 mV pk-pk[2]
6	MGTYAVTT	1.20	2%	10 mV pk-pk[2]
7	VCCO (multiple rails)	1.0 to 3.3	1%	4% +2%/–4% (3.3V)

Notes:

1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Minimum Rails, Low Voltage, PS Overdrive

This scenario utilizes a minimum number of power rails along with the lowest possible core voltage of 0.70V while the processing system (PS) and PMC rails are powered at 0.88V. This scenario can be selected in XPE by choosing a -1LI device along with the core voltage specifying the PS at 0.88V.

Table 4: **Power Supply Groupings for Minimum Rails, Low Voltage, PS Overdrive Scenario**

Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
1	VCCINT	0.70	1%	±17 mV
2	VCC_RAM, VCC_SOC, VCC_IO, VCCINT_GT (when present)	0.80	1%	±17 mV
3	VCC_PSLP, VCC_PSFP, VCC_PMC, VCC_CPM5 (when present)	0.88	1%	±17 mV
4	VCCAUX, VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%
5	MGTYAVCC	0.88	2%	10 mV pk-pk[2]
6	MGTYVCCAUX	1.50	2%	10 mV pk-pk[2]
7	MGTYAVTT	1.20	2%	10 mV pk-pk[2]
8	VCCO (multiple rails)	0.6 to 3.3	2%	4% +2%/–4% (3.3V)

Notes:

1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Minimum Rails, Mid/High Voltage

This scenario utilizes a minimum number of power rails along with a core voltage of either 0.80V or 0.88V. This scenario can be selected in XPE by choosing a -M (0.80V) or -H (0.88V) device.

Table 5: **Power Supply Groupings for Minimum Rails, Mid-/High-Voltage Scenario**

Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
1	VCCINT, VCC_RAM, VCC_SOC, VCC_IO, VCC_PSFP, VCC_PSLP, VCC_PMC, VCCINT_GT (when present), VCC_CPM5 (when present)	0.80 or 0.88	1%	±17 mV
2	VCCAUX, VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%
3	MGTYAVCC	0.88	2%	10 mV pk-pk[2]
4	MGTYVCCAUX	1.50	2%	10 mV pk-pk[2]
5	MGTYAVTT	1.20	2%	10 mV pk-pk[2]
6	VCCO (multiple rails)	0.6 to 3.3	1%	4% +2%/–4% (3.3V)

Notes:

1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Full Power Management, Low Voltage

This scenario utilizes multiple power rails for maximum power up/down flexibility, along with the lowest possible core voltage of 0.70V. This scenario can be selected in XPE by choosing a -L device.

Table 6: **Power Supply Groupings for Full Power Management, Low Voltage Scenario**

Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
PMC/1	VCC_PMC	0.70	1%	±17 mV
PMC/2	VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%
PMC/3	VCCO_500, VCCO_501	1 to 3.3	1%	4%
System/1	VCC_SOC, VCC_IO	0.80	1%	±17 mV
System/2	VCCAUX	1.50	1%	2%
System/3	VCCO (DDRMC)	1 to 3.3	1%	4%
LPD/1	VCC_PSLP, VCC_CPM5 (when present)	0.70	1%	±17 mV
LPD/2	VCCO_502	1 to 3.3	1%	4%
FPD/1	VCC_PSFP	0.70	1%	±17 mV
PL/1	VCCINT	0.70	1%	±17 mV
PL/2	VCC_RAM, VCCINT_GT (when present)	0.80	1%	±17 mV
PL/3	MGTYAVCC	0.88	2%	10 mV pk-pk[2]
PL/4	MGTYVCCAUX	1.50	2%	10 mV pk-pk[2]
PL/5	MGTYAVTT	1.20	2%	10 mV pk-pk[2]
PL/6	VCCO (multiple rails)	0.6 to 3.3	1%	4% +2%/–4% (3.3V)

Notes:

1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Full Power Management, Low Voltage, PS Overdrive

This scenario utilizes multiple power rails for maximum power up/down flexibility, along with the lowest possible core voltage of 0.70V for VCCINT, with the processing system (PS) and PMC rails at the highest voltage of 0.88V. This scenario can be selected in XPE by choosing a -1LI device along with the core voltage specifying the PS at 0.88V.

Table 7: **Power Supply Groupings for Full Power Management, Low Voltage, PS Overdrive Scenario**

Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
PMC/1	VCC_PMC	0.88	1%	±17 mV
PMC/2	VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%
PMC/3	VCCO_500, VCCO_501	1 to 3.3	1%	4%
System/1	VCC_SOC, VCC_IO	0.80	1%	±17 mV
System/2	VCCAUX	1.50	1%	2%
System/3	VCCO (DDRMC)	1 to 3.3	1%	4%
LPD/1	VCC_PSLP, VCC_CPM5 (when present)	0.88	1%	±17 mV
LPD/2	VCCO_502	1 to 3.3	1%	4%
FPD/1	VCC_PSFP	0.88	1%	±17 mV
PL/1	VCCINT	0.70	1%	±17 mV
PL/2	VCC_RAM, VCCINT_GT (when present)	0.80	1%	±17 mV
PL/3	MGTYAVCC	0.88	2%	10 mV pk-pk[2]
PL/4	MGTYVCCAUX	1.50	2%	10 mV pk-pk[2]
PL/5	MGTYAVTT	1.20	2%	10 mV pk-pk[2]
PL/6	VCCO (multiple rails)	0.6 to 3.3	1%	4% +2%/–4% (3.3V)

Notes:

1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Full Power Management, Mid/High Voltage

This scenario utilizes multiple power rails for maximum power up/down flexibility, along with a core voltage of either 0.80V or 0.88V. This scenario can be selected in XPE by choosing a -M (0.80V) or -H (0.88V) device.

Table 8: **Power Supply Groupings for Full Power Management, Mid-/High-Voltage Scenarios**

Sequence Order	Combined Rails	Nominal Voltage (V)	DC VRM Tolerance[1]	AC Ripple Noise[1]
PMC/1	VCC_PMC	0.80 or 0.88	1%	±17 mV
PMC/2	VCCAUX_PMC, VCCAUX_SMON (filtered)	1.50	1%	2%
PMC/3	VCCO_500, VCCO_501	1 to 3.3	1%	4%
System/1	VCC_SOC, VCC_IO	0.80 or 0.88	1%	±17 mV
System/2	VCCAUX	1.50	1%	2%
System/3	VCCO (DDRMC)	1 to 3.3	1%	4%
LPD/1	VCC_PSLP, VCC_CPM5 (when present)	0.80 or 0.88	1%	±17 mV
LPD/2	VCCO_502	1 to 3.3	1%	4%
FPD/1	VCC_PSFP	0.80 or 0.88	1%	±17 mV
PL/1	VCCINT, VCC_RAM, VCCINT_GT (when present)	0.80 or 0.88	1%	±17 mV
PL/2	MGTYAVCC	0.88	2%	10 mV pk-pk[2]
PL/3	MGTYVCCAUX	1.50	2%	10 mV pk-pk[2]
PL/4	MGTYAVTT	1.20	2%	10 mV pk-pk[2]
PL/5	VCCO (multiple rails)	0.6 to 3.3	1%	4% +2%/–4% (3.3V)

Notes:

1. Expressed as ±% from nominal voltage.
2. 10 kHz to 80 MHz.

Recommended Decoupling Capacitor Quantities for Versal AI Core Series

Recommended decoupling quantities for Versal AI core, Auxiliary, and VCCO rails can be obtained via the Xilinx Power Estimator (XPE) tool. XPE provides a custom set of decoupling guidelines based on the actual usage parameters of the design.

For designs that are in the early stages and where a set of "placeholder" capacitors are desired, see Appendix A: Default Capacitor Quantities for Versal Devices for a list of default quantities. These quantities, if used, should be replaced by the quantities recommended in XPE after the design usage parameters are known.

The following sections illustrate the methodology that XPE uses for determining the appropriate number of decoupling capacitors to use for a particular power rail.

Decoupling Capacitor Methodology

Device Resource Utilization

The amount of decoupling required is primarily determined by the amount of power utilized by the design. The power can be accurately estimated by using the XPE tool. By entering such usage parameters as the number of logic cells and DSPs, an accurate current power profile can be obtained.

Resource utilization consists (in part) of:

- AI Engine: Number of cores used, frequency, loading, and read/write rate
- Logic: Number of registers and LUTs, toggles rates, and frequency
- Block RAM: Number of block RAMs, toggles rates, enable rates, and frequencies
- URAM: Number of UltraRAMs, toggles rates, enable rates, and frequencies
- DSP: Number of DSP blocks, toggles rates, enable rates, and frequencies
- GTY: Number of GTY transceivers used, types (PCIe or MRMAC), and frequencies
- Processing System: Low Power Domain (LP): Processor speeds, interconnect, loading, and interconnect
- Processing System: Full Power Domain (FP): Processor speeds, interconnect, loading, and interconnect
- Processing System: I/O (MIO): Interfaces types (USB, QSPI, and eMMC) and speeds
- XPIO: I/O standards, enable rates, and frequencies
- HDIO: I/O standards, enable rates, and frequencies

Current Step Load Assumptions

The step load is the percentage of the dynamic current that is expected to be demanded at any given switching event. This is the instantaneous current that will be provided primarily by the decoupling capacitors until the regulators can respond. XPE has predefined step load percentages for each rail, which can be adjusted as determined by the needs of the individual system design. As a point of reference, the current consumption of VCCINT has the most notable effect on the amount of decoupling required by the system, so it is important to ensure the step load percentage is as accurate as possible. It is recommended to leave the other step load percentages at their default values because they are much more stable in regards to system design.

Voltage Ripple Assumptions

AC voltage ripple along with VRM DC tolerance on each rail is assumed to fall within the specifications as defined in the Versal ACAP data sheets. For purposes of determining PCB decoupling, the core rails (VCCINT, VCC_RAM, VCC_SOC, VCC_IO, VCC_PSFP, VCC_PSLP, and VCC_PMC) use a fixed 17 mV for AC ripple in addition to a DC VRM tolerance of 1%. For example, if the Versal ACAP data sheets list a minimum/maximum operating voltage, decoupling capacitors are designed to ensure that the AC ripple stays within 17 mV while the rest of the margin is allocated to account for the 1% DC tolerance of most voltage regulator modules (VRMs).

Target Impedance

Given the required ripple tolerance and step load amount, a target impedance can be calculated. The impedance of the PDN network on the board should be targeted to be at or below this target impedance at the typical frequency in which decoupling capacitors are most effective, which is approximately 100 kHz to approximately 50–75 MHz (~15 MHz for VCCINT). Beyond these frequencies, the internal and mounting inductances of the capacitors reduce their effectiveness.

The formula for target impedance is shown in the following equation.

Equation 1: **Target Impedance Equation**

$$Z_{target} = \frac{VoltageRailValue \times \frac{\%\ Ripple}{100}}{StepLoadCurrent}$$

An example calculation for a 0.80V rail specified with 3% tolerance (1% DC, 2% AC) and 40A of required step current is as follows:

Equation 2: **Target Impedance Calculation**

$$Z_{target} = \frac{0.80 \times \frac{2}{100}}{40} = 0.40\ m\Omega$$

Recall that 2% is used as the ripple target because 1% is assumed to be taken by the tolerance of the VRM.

***Note*:** For the case where the ripple tolerance is given as a fixed number such as 17 mV, use the fixed value as the numerator in the above equation.

TIP: *Xilinx recommends running a full board-level PDN simulation to confirm that the voltage specifications are met.*

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Chapter 3

PCB Guidelines for Memory Interfaces

The Versal architecture provides solutions for interfacing with the following memory architectures:

- DDR4
- LPDDR4/4x
- RLDRAM3
- QDR-IV

Before the individual architecture guidelines is a section on required guidelines that apply to all memory interfaces.

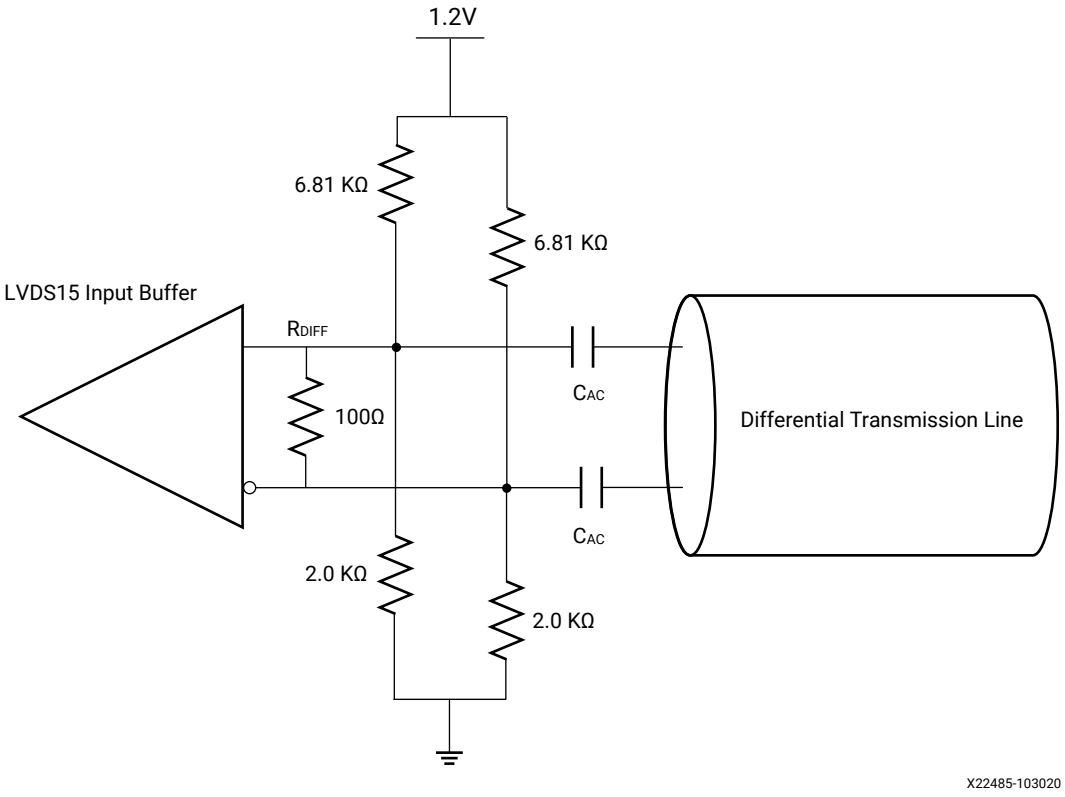
Required Memory Routing Guidelines for All Interfaces

The following list contains guidelines that apply to all memory interfaces (DDR4, LPDDR4/4x, RLD3, and QDR-IV interfaces).

1. Include package delay in routing constraints when determining signal trace lengths unless otherwise specified. When minimum and maximum values are available for the package delay, use the midpoint/average between the minimum and maximum values.
2. DQ and DQS signals in the same byte group should be routed on the same layer from Versal device to DRAM/DIMM. Include the data mask (DM) in the byte group as applicable.
3. Do not change layers when routing from one DIMM to the next for multi-slot topologies. Additionally, it is recommended to route data byte groups on the highest signal layers (closest to the DIMM connector) as much as possible. Depending on the DIMM placement, the longest DQ bytes could be the center ones or the edge ones.

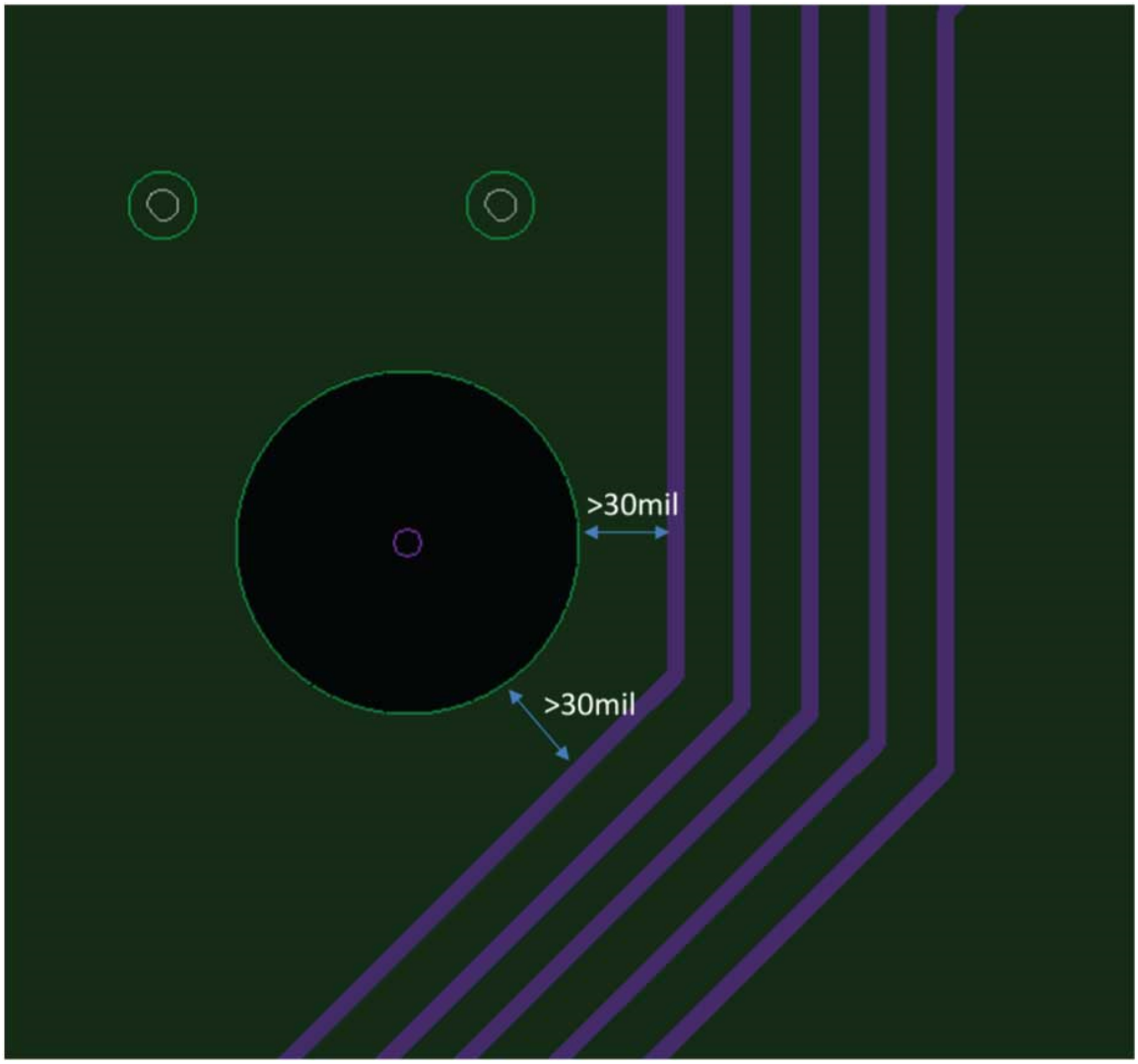
4. For fly-by routing, address, command, and control signals can be routed on different layers, but it is recommended to use as few as possible. Do not route any individual signal on more than two layers to minimize inductive loops that can lead to crosstalk issues. Any signal layer switching via needs to have one ground via within a 50 mil radius.
5. Versal device and memory drive strengths are assumed to be 40Ω. Versal device DCI and memory ODT are assumed to be 40Ω.
6. If the system clock is connected to a bank that is also used for memory, it may be necessary to bias the incoming clock signals so that they adhere to the signal level requirements of the IO standard in the bank. Refer to the "AC Coupling Recommendations" section in *Versal ACAP SelectIO Resources Architecture Manual* (AM010) for specific requirements. The following figure shows the biasing structure from that document.

Figure 1: **AC-Coupled with DC-Biased Differential Clock Input**



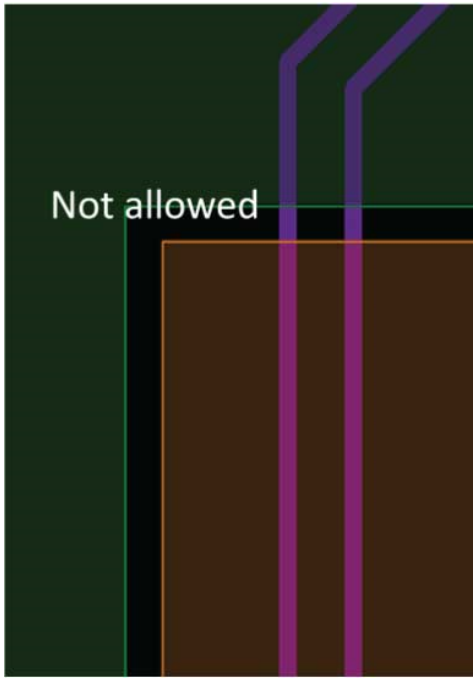
7. Signal lines must be routed over a solid reference plane. Avoid routing over voids, as shown in the following figure.

Figure 2: **Signal Routing Over Solid Reference Plane**



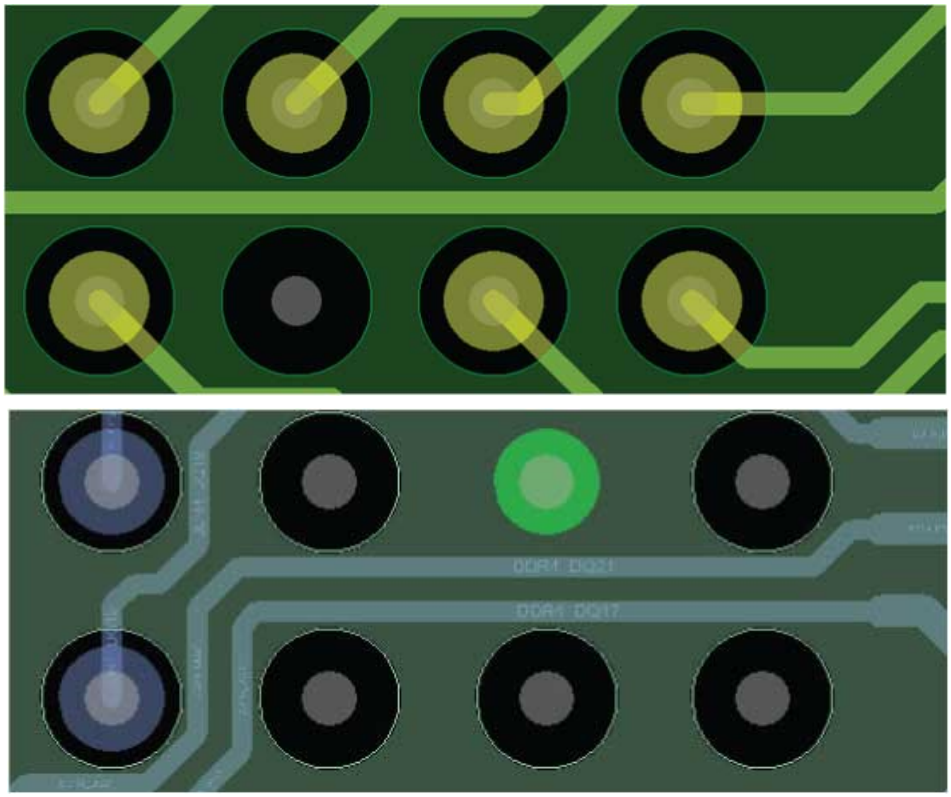
8. Avoid routing over reference plane splits, as shown in the following figure.

Figure 3: **Signal Routing Over Reference Plane Split**



9. Keep the routing at least 30 mils away from the reference plane and void edges with the exception of breakout regions, as shown in the following figure.

Figure 4: **Breakout Region Routing**



10. Use chevron-style routing to allow for ground stitch vias. Figure 5 shows recommended routing for fly-by configurations, while Figure 6 shows recommended routing to accommodate ground stitch vias in a more congested clamshell configuration.

Figure 5: **Example of Ground Stitching (Fly-by)**

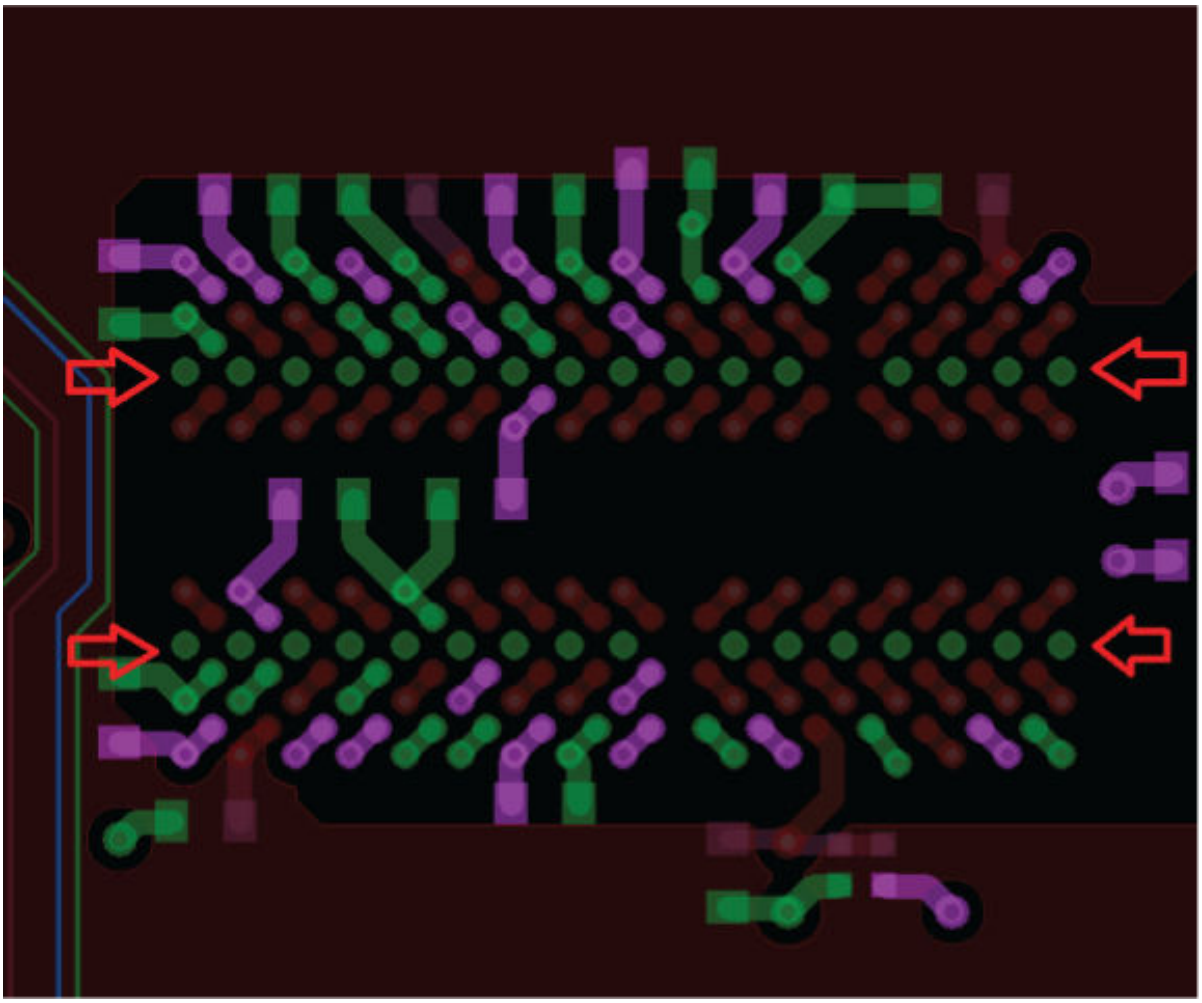
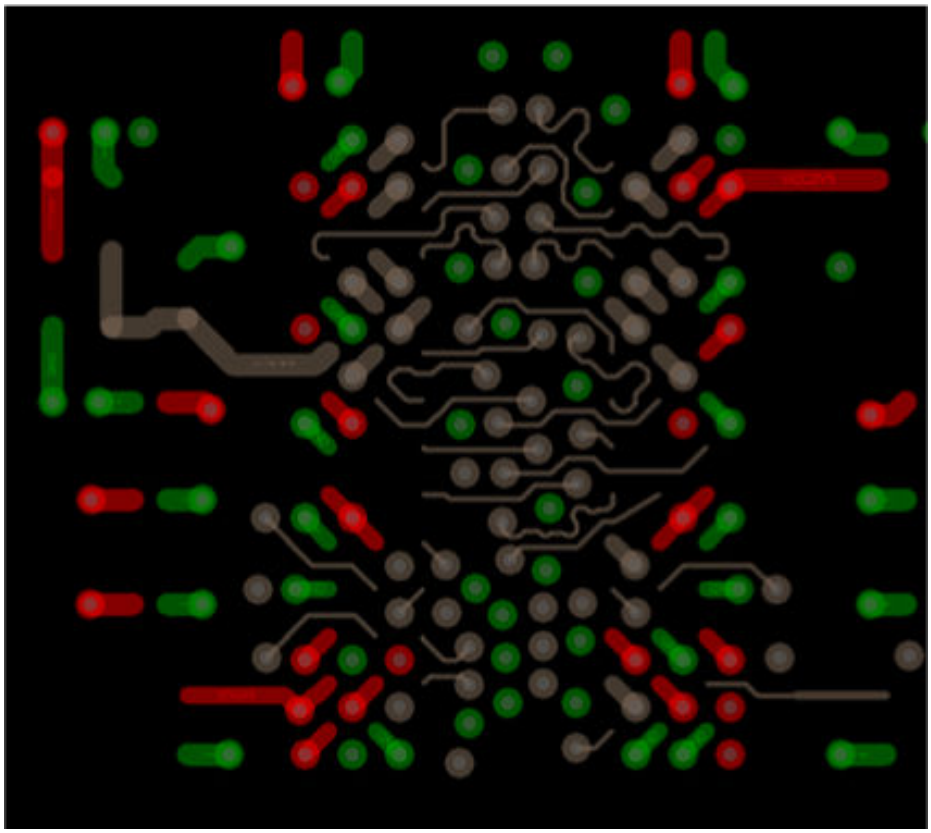


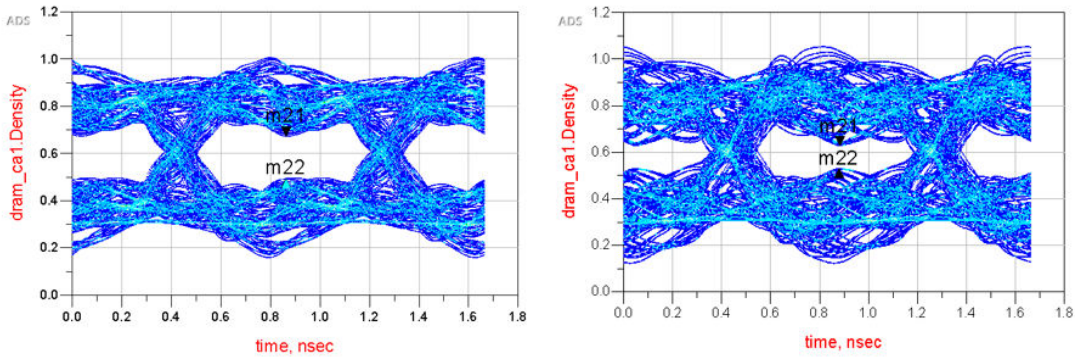
Figure 6: **Example of Ground Stitching (Clamshell) Red: Power, Green: Ground**



The following figure shows simulated eye diagrams for a DDR4 command/address/control bit with and without ground stitching vias. The simulation on the left shows an eye height of 180 mV with ground stitch vias, while the simulation on the right shows an eye height of only 99 mV when not utilizing ground stitch vias.

Figure 7: **Simulations With and Without Ground Stitching Vias**

	Case 1: with GND vias	Case 2: without GND vias
Eye Height (mV)	180	99



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11. Add ground vias as much as possible around the edges and inside the device (ACAP, memory component, DIMM) to make a better ground return path for signals and power, especially corners. Corner or edge balls are generally less populated as grounds.

12. For address/command/control VTT termination, every four termination resistors should be accompanied by one 1.0 µF capacitor, physically interleaving among resistors, as shown in the following figure. Refer to the memory vendor's data sheet for specifications regarding noise limits on the address/command/control VTT lines.

Figure 8: **Schematic Example of VTT Resistor and Capacitor Connections**

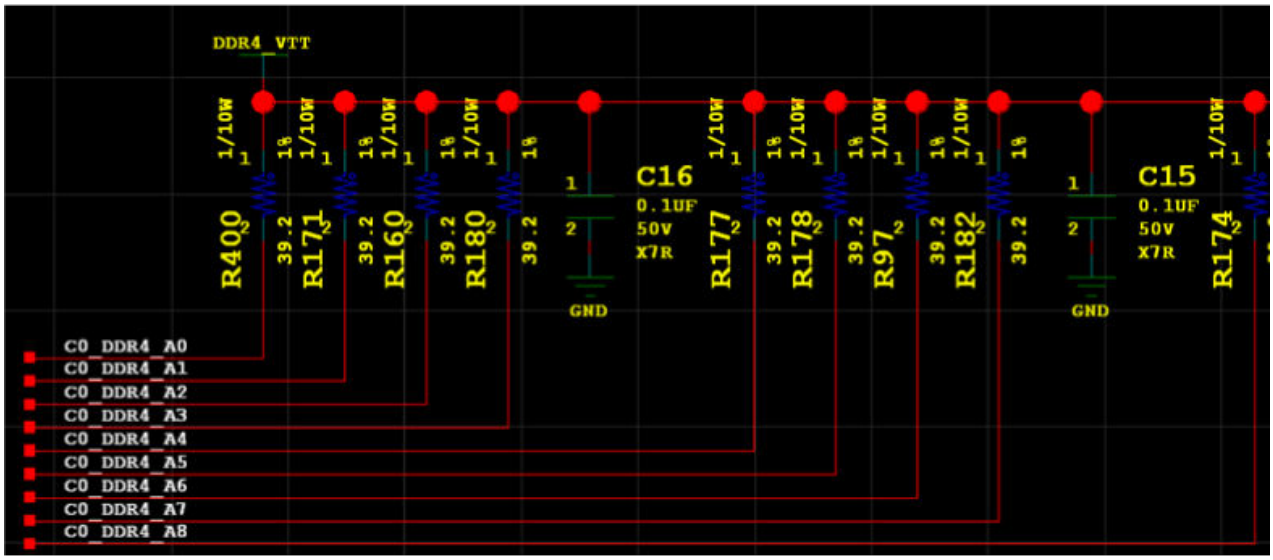
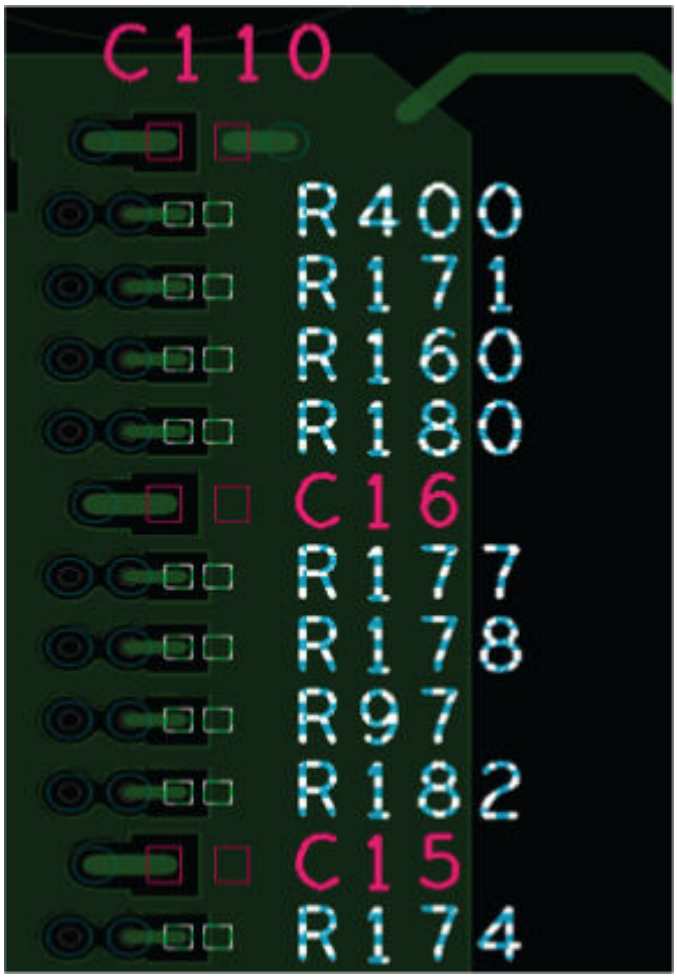


Figure 9: **Example of V_{TT} Termination Placement**



13. For DIMM topologies, place bypass capacitors near the command/address/control pads to provide extra ground via locations. These bypass capacitors also provide a lower impedance path from power to ground. This is important because the address/command/control pins are referenced to ground on the ACAP and PCB while they are referenced to power on the DIMM.
14. For dual-slot DIMM topologies, place DIMM #0 on the furthest connector from the ACAP to reduce the effect of SI reflections. The DIMM #1 connector should be placed nearest to the ACAP.
15. For DDR4 interfaces with two copies of the clock and nine or more components (e.g., interfaces with dual-die package (DDP) devices), it is recommended to route the clocks in an alternating pattern such that clock 1 connects to devices 1, 3, 5, 7, etc., and clock 2 connects to devices 2, 4, 6, 8, etc. All terminations should be placed at the end of the fly-by topology.
16. For clamshell configurations that use address mirroring, ensure that both chip select lines have adequate decoupling at their terminations as well as sufficient plane/trace thicknesses to/from VTT.

Reference Material Specifications

The guidelines in this chapter were determined based on the following PCB material specifications. Signal integrity simulations are encouraged for any material or specifications that deviate from those listed here.

- Board material: FR-4
- Dielectric constant: 4.0
- Dissipation factor: 0.023
- Board thickness: 65 mil

PCB Routing Guidelines for DDR4 Interfaces

This section provides PCB design guidelines for DDR4 interfaces. Connections between the ACAP and DDR4 device(s) are defined along with physical design rules and timing constraints. Both component and DIMM architectures are covered.

Signals and Connections for DDR4 Interfaces

The required signals used in DDR4 applications are shown in the following table. The signal list might vary slightly depending on the particular DDR4 architecture used.

IMPORTANT! *For dual-slot DIMM topologies, place DIMM #0 on the furthest connector from the ACAP to reduce the effect of SI reflections. The DIMM #1 connector should be placed nearest to the ACAP.*

Table 9: **DDR4 Signal Definitions**

Signal	Description	Required PCB Termination[1]	Signal Routing Methodology
Clock Signals			
CK_T/CK_C[2]	Address/Command Clock	See Figure 11	Fly-by
Address Signals			
A[17], A[13:0]	Address	39Ω to VTT at far end	Fly-by
RAS_N/A[16]	Row Access Strobe	39Ω to VTT at far end	Fly-by
CAS_N/A[15]	Column Access Strobe	39Ω to VTT at far end	Fly-by
WE_N/A[14]	Write Enable	39Ω to VTT at far end	Fly-by
BA[1:0]	Bank Address	39Ω to VTT at far end	Fly-by
BG[1:0]	Bank Group	39Ω to VTT at far end	Fly-by
Command/Control Signals			
ACT_N	Activate Command	39Ω to VTT at far end	Fly-by

Table 9: **DDR4 Signal Definitions** *(cont'd)*

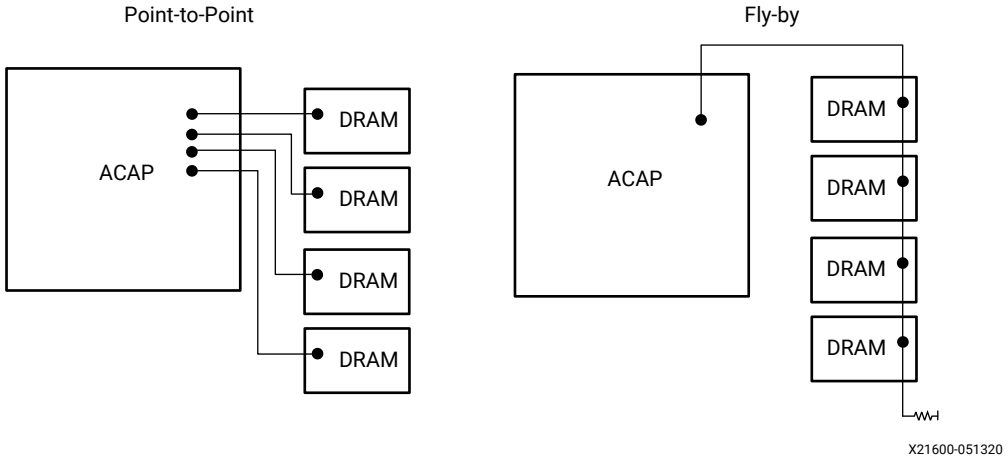
Signal	Description	Required PCB Termination[1]	Signal Routing Methodology
CKE	Clock Enable	39Ω to VTT at far end	Fly-by
CS_N	Chip Select	39Ω to VTT at far end	Fly-by
ODT	On-Die Termination Enable	39Ω to VTT at far end	Fly-by
PAR	Command/Address Parity	39Ω to VTT at far end	Fly-by
Data Signals			
DQ byte/nibble (8 or 4 bits each)	Data	None, uses ODT	Point-to-point
DM/DBI (If present, one per byte)	Data Mask/Data Bus Inversion	None, uses ODT	Point-to-point
Data Strobe Signals			
DQS_T/DQS_C (one pair per byte/nibble)	Data Strobe	None, uses ODT	Point-to-point
Miscellaneous Signals			
RESET_N	Reset	4.7 kΩ to GND at far end	Fly-by
DDR4 Devices/DIMMs Only			
ALERT_N (devices)	CRC Error Flag Open-Drain Output	Tie all ALERT_N pins in same interface to DRAM VDD through 50Ω resistor if not used in system	Shared Pull-up
TEN (devices)	Connectivity Test Mode Input	50Ω to GND	One per memory device
ZQ (devices)	Calibration Reference	240Ω to GND	One per memory device
EVENT_N (DIMM)	Temperature Event Open-Drain Output	Tie all EVENT_N pins in same interface to VDDSPD through 4.7 kΩ resistor	Shared Pull-up
ACAP Device Only			
IO_VP_700 IO_VP_800 (if present)	Calibration Reference	240Ω to VCCO_700 240Ω to VCCO_800 (if present)	

Notes:

1. Clock and address/command/control signals only require PCB termination for component interfaces.
2. To reduce loading on CK when using DDP-wide or DDP-deep component interfaces, two CK pairs are required for interfaces that have larger than nine loads and a data rate of 1866 Mb/s or higher.

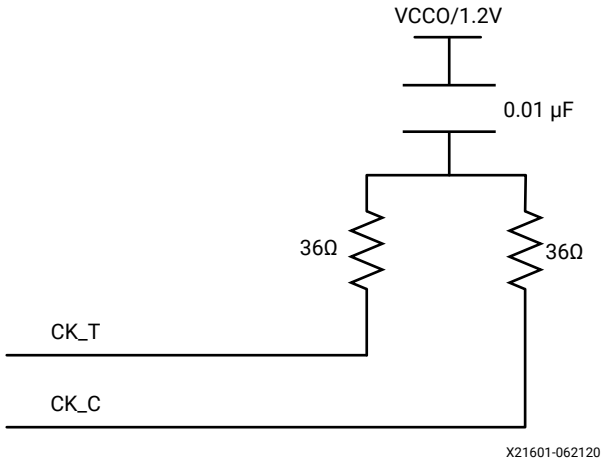
Command/address/control (CAC) signals are routed in a fly-by pattern with far-end termination. DQ and DQS signals are routed point-to-point. The following figure shows examples of fly-by and point-to-point routing.

Figure 10: **Point-to-Point (DQ/DQS) and Fly-by (CAC) Routing**



IMPORTANT! *When creating a DDR4 interface, all components in the interface must be the same (i.e., share the same part number, data width, density, and speed grade).*

Figure 11: **Far-End Termination for Differential Clock CK_T/CK_C (Component Interfaces Only)**



Physical Design Rules for DDR4 Signals

The following table defines routing rules for DDR4 signals.

Table 10: **Physical Design Rules for DDR4 Signals**

Parameter	Value
Impedance Rules	
Impedance for single-ended CAC[1] and data signals	50Ω[2] ± 10%
Impedance for differential clock (CK) and data strobe (DQS)	90Ω[2] ± 10%
Trace Length Rules (from ACAP to Furthest Device or Termination)	
Maximum PCB trace length for CAC signals	11000 mils
Maximum PCB trace length for data/strobe signals	5500 mil
Spacing Rules for CAC Signals	
Minimum spacing between CAC signals	2H[3], except: 1H under ACAP 1.5H under DDR4 device
Minimum spacing between CAC signals and clock signals	5H, except: 2H under ACAP 2H under DDR4 device
Minimum spacing between CAC signals and data signals	5H, except: 2H under ACAP 2H under DDR4 device
Spacing Rules for Data and Data Strobe Signals	
Minimum spacing between data/strobe signals within the same byte	2H, except: 1H under ACAP 1.5H under DDR4 device
Minimum spacing between data/strobe signals to data/strobe signals in other bytes	5H, except: 2H under ACAP 2H under DDR4 device
Spacing Rules for Signals between Memory Interfaces	
Minimum spacing between signals in one memory interface to signals in another memory interface	5H, except: 2H under ACAP 2H under DDR4 device
Maximum Via Count per Signal Type	
CAC signals and clock signals	(2 × # of devices) + 2
Data and strobe signals	2
Other Physical Design Requirements	
Do not route CAC/clock signals on more than two internal signal layers	
Do not route data/strobe signals on more than one internal signal layer	

Table 10: **Physical Design Rules for DDR4 Signals** *(cont'd)*

Parameter	Value
Route data/strobe signals on internal layers as close to the memory devices as possible	

Notes:

1. CAC stands for command/address/control.
2. Up to 60Ω (single-ended) or 120Ω (differential) under ACAP or DRAM devices, taking into account PCB manufacturing tolerances.
3. H is the distance to the nearest ground return plane.

Timing Constraint Rules for DDR4 Signals

The timing constraints are defined in the following tables for various signal groups and their targets, similar to how they would be entered into PCB layout software tools. ACAP package delays should always be included for purposes of determining skews.

Table 11: **Skew Constraint Rules for DDR4 Signals (Components)**[1]

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address to Clock[2]	ACAP to DDR4 component	–34	–50	A[17], A[13:0] RAS_N/A[16] CAS_N/A[15] WE_N/A[14] BA[1:0] BG[1:0] ACT_N CKE CS_N ODT PAR	CK_T
Clock[2,3]	ACAP to DDR4 component	0	2	CK_T CK_C	-
Data to DQS[4]	ACAP to DDR4 component	–100	+100	DQ (4/8 bits) DM/DBI (if present)	DQS_T
DQS[3,4]	ACAP to DDR4 component	0	2	DQS_T DQS_C	-
Clock to DQS[4]	ACAP to DDR4 component	–149	+1796	CK_T	DQS_T

Notes:

1. Include ACAP package delays for all skew calculations.
2. There should be individual constraint sets for each DDR4 component (e.g., ACAP to DRAM 1, ACAP to DRAM 2, etc.).
3. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.
4. There should be individual constraint sets for each byte/nibble/DQS pair.

Table 12: **Skew Constraint Rules for DDR4 Signals (DIMM)[1]**

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address to Clock[2]	ACAP to DIMM	–8	+8	A[17], A[13:0] RAS_N/A[16] CAS_N/A[15] WE_N/A[14] BA[1:0] BG[1:0] ACT_N CKE CS_N ODT PAR	CK_T
Clock[2,3]	ACAP to DIMM	0	2	CK_T CK_C	-
Data to DQS[4]	ACAP to DIMM	–100	+100	DQ (4/8 bits) DM/DBI (if present)	DQS_T
DQS[3,4]	ACAP to DIMM	0	2	DQS_T DQS_C	-
Clock to DQS[4]	ACAP to DIMM	–150	+150	CK_T	DQS_T

Notes:

1. Include ACAP package delays for all skew calculations.
2. There should be individual constraint sets for each DDR4 DIMM (e.g., ACAP to DIMM 1, ACAP to DIMM 2, etc.).
3. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.
4. There should be individual constraint sets for each byte/nibble/DQS pair.

PCB Routing Guidelines for LPDDR4/4x Interfaces

This section provides PCB design guidelines for LPDDR4/4x interfaces. Connections between the ACAP and LPDDR4/4x device(s) are defined, along with physical design rules and timing constraints.

Note: To obtain maximum LPDDR4/4x speed, it is recommended to keep the board thickness less than 62 mil. See Reference Material Specifications.

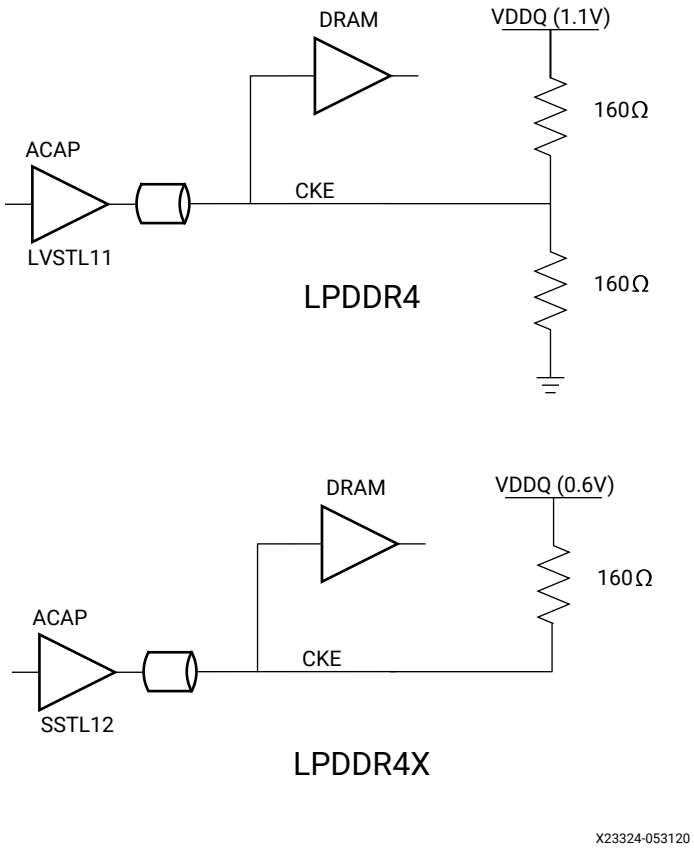
Signals and Connections for LPDDR4/4x Interfaces

The required signals used in LPDDR4/4x applications are shown in the following table.

Table 13: **LPDDR4/4x Signal Definitions**

Signal	Description	Required PCB Termination
Clock Signals		
CK_T[C]_A, CK_T[C]_B	Address/Command clock	None, uses ODT 48Ω
Command/Address Signals		
CA[5:0]_A, CA[5:0]_B	Address	None, uses ODT 48Ω
Control Signals		
CS0_A, CS0_B	Chip Select	None, uses ODT 48Ω
CS1_A, CS1_B	Chip Select (dual rank only)	None, uses ODT 48Ω
LPDDR4: CKE0_A, CKE0_B LPDDR4: CKE1_B, CKE1_B (dual rank only)	Clock Enable	160Ω to GND/160Ω to VDDQ (1.1V) (see Figure 12)
LPDDR4X: CKE0_A, CKE0_B LPDDR4X: CKE1_B, CKE1_B (dual rank only)	Clock Enable	160Ω to VDDQ (0.6V) (see Figure 12)
Data Signals		
DQ[15:0]_A, DQ[15:0]_B	Data	None, uses ODT 48Ω
DM[1:0]_A, DM[1:0]_B (if present)	Data Mask	None, uses ODT 48Ω
Data Strobe Signals		
DQS[1:0]_T[C]_A, DQS[1:0]_T[C]_B	Differential Data Strobe	None, uses ODT 48Ω
Miscellaneous Signals		
RESET_n	Reset (one per LPDDR4/4x device)	4.7 kΩ to GND
LPDDR4/4x Device Only		
LPDDR4: ODT_A, ODT_B	On Die Termination Control (per device)	Direct to VDD2 (except for ODT_A on 2x32 pin efficient, see Figure 18).
LPDDR4x: ODT_A, ODT_B	On Die Termination Control (per device)	Direct to VDD2
ZQ0	Calibration Reference (per device)	240Ω to VDDQ
ZQ1	Calibration Reference (per device, dual rank only)	240Ω to VDDQ
ACAP Only		
IO_VP_700 IO_VP_800 (if present)	Calibration Reference	240Ω to VCCO_700 240Ω to VCCO_800 (if present)

Figure 12: **LPDDR4/4X CKE Termination**



Supply Voltage Differences between LPDDR4 and LPDDR4x

Users should be aware of the varying voltages levels for the ACAP and memory devices between LPDDR4 and LPDDR4x, as shown in the following table.

Table 14: **Typical Supply Voltages for LPDDR4 and LPDDR4x**

	VCCO_xxx (ACAP)	VDD2	VDDQ
LPDDR4	1.1V	1.1V	1.1V
LPDDR4x	1.2V	1.1V	0.6V

The following figures show the various supported connection options for LPDDR4/4x such as 2x32, 1x32 with and without ECC, 2x16, 1x16, and *pin efficient* 2x32 and 1x32 that use significantly fewer ACAP pins than the regular 2x32 and 1x32 options.

Figure 13: **Connections for a 2x32 LPDDR4/4x Interface**

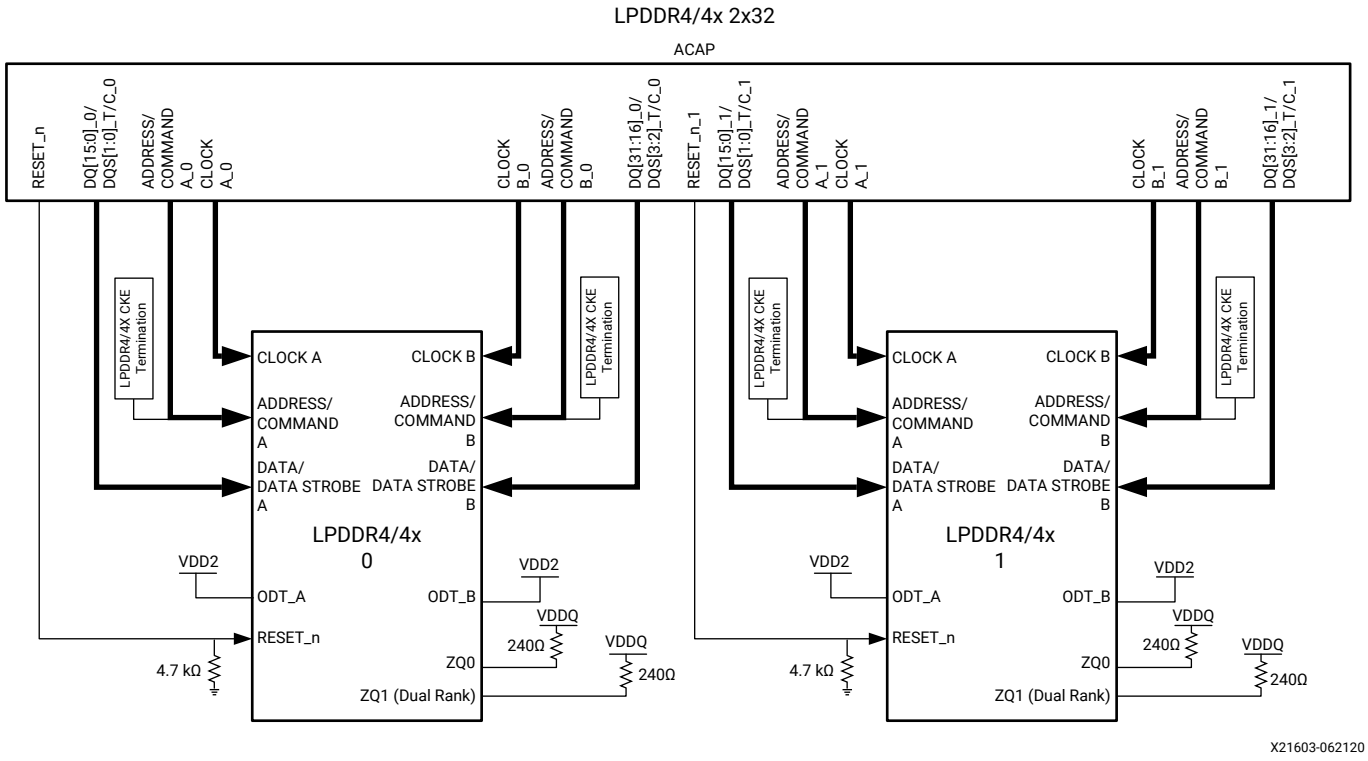


Figure 14: **Connections for a 1x32 (or x48) with ECC LPDDR4/4x Interface**

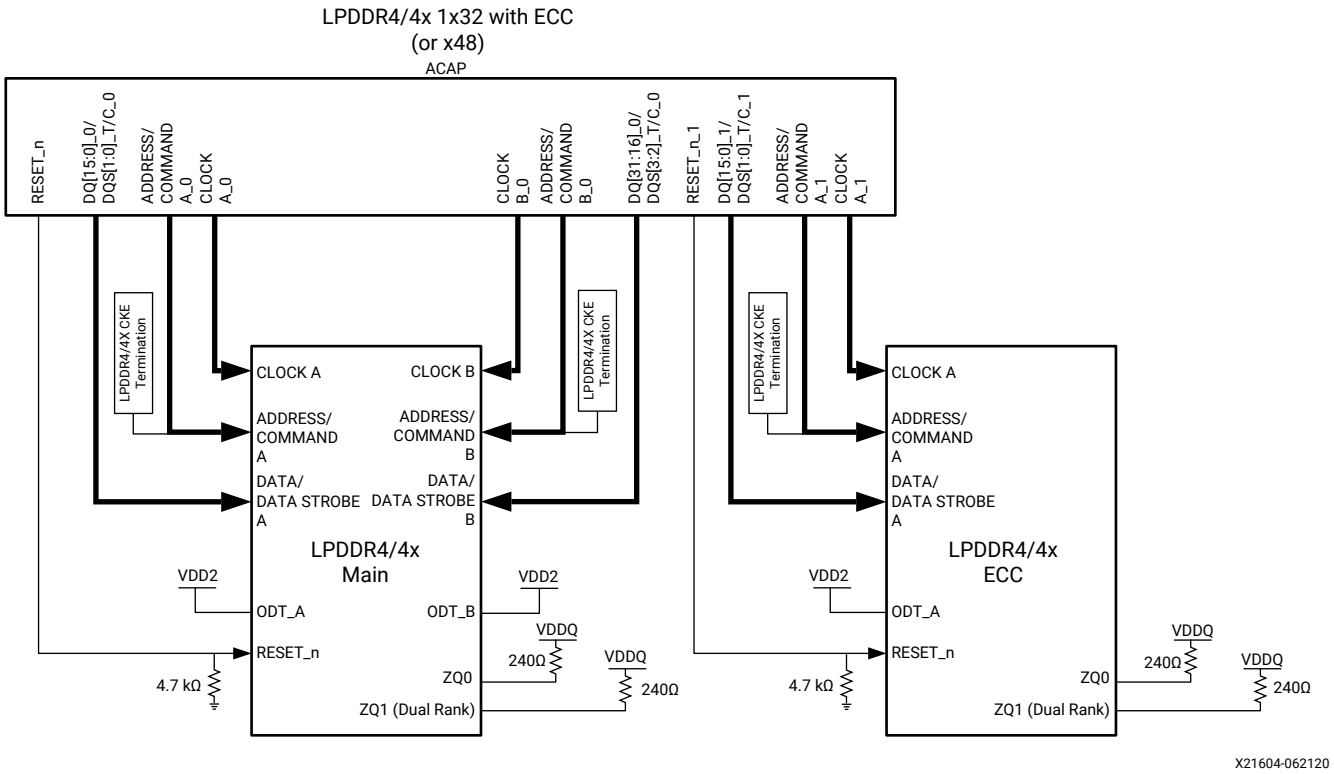


Figure 15: **Connections for a 1x32 LPDDR4/4x Interface**

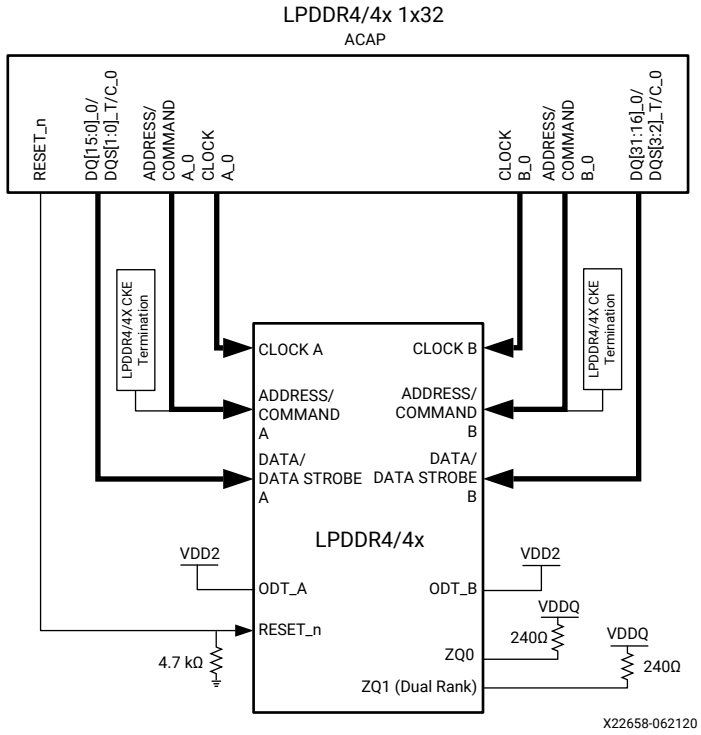


Figure 16: **Connections for a 2x16 LPDDR4/4x Interface**

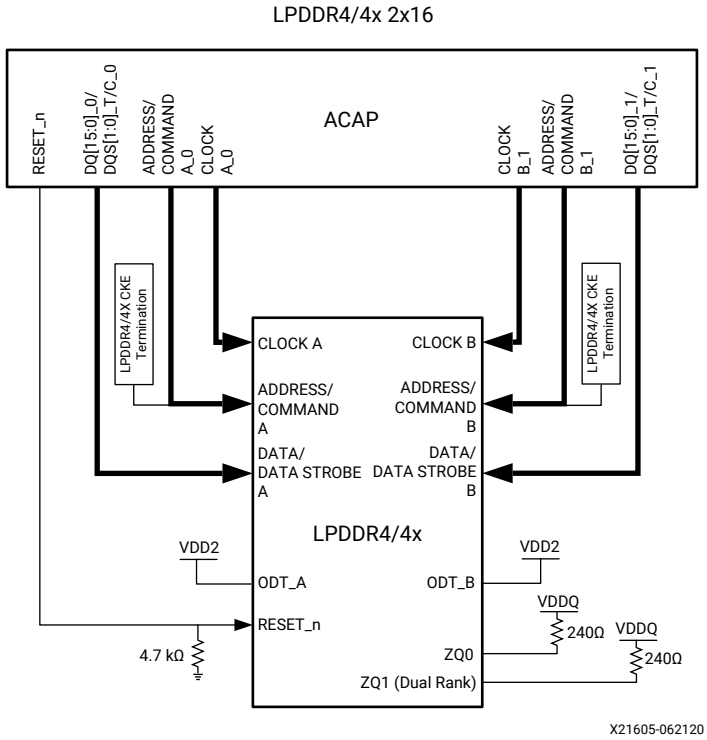


Figure 17: **Connections for a 1x16 LPDDR4/4x Interface**

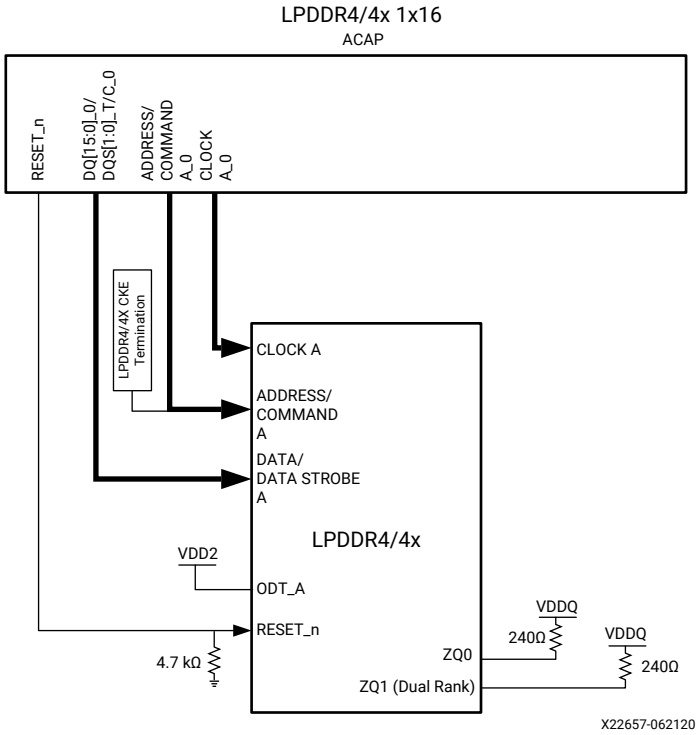


Figure 18: **Connections for a Pin Efficient 2x32 LPDDR4/4x Interface**

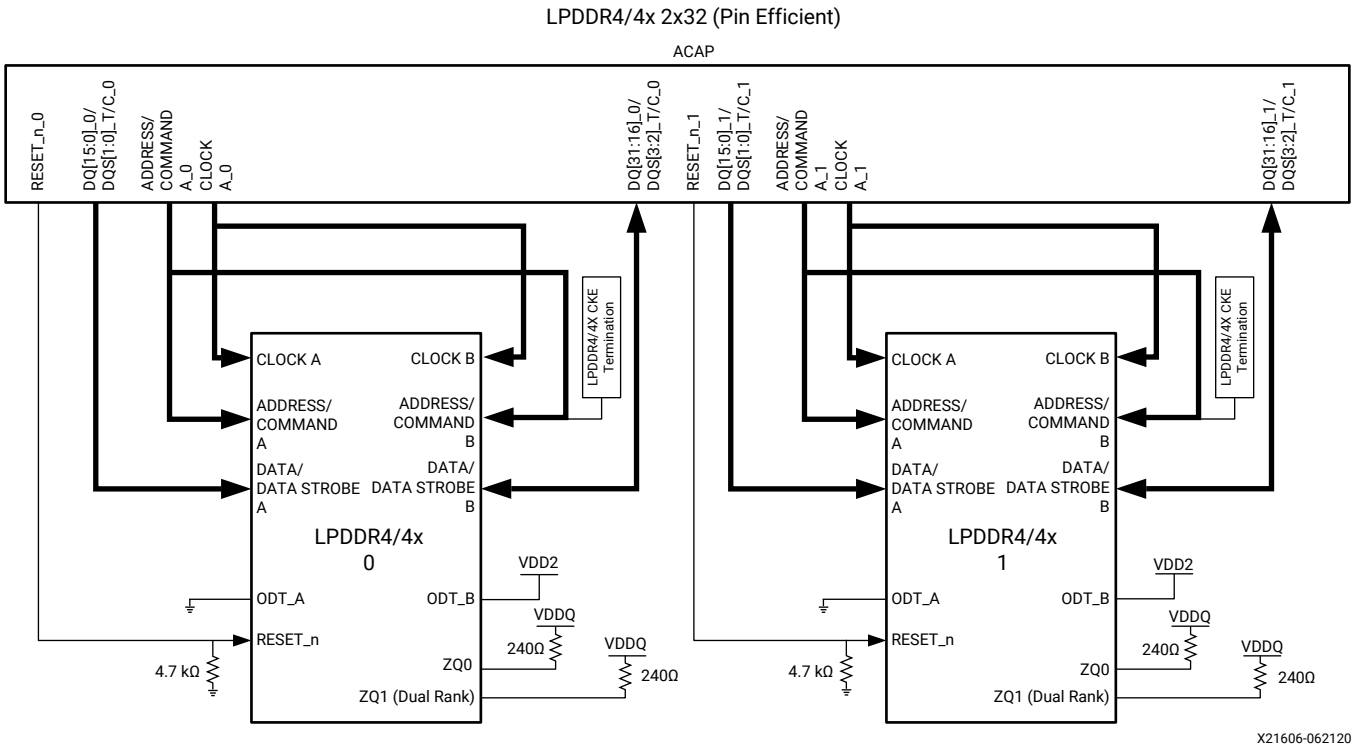
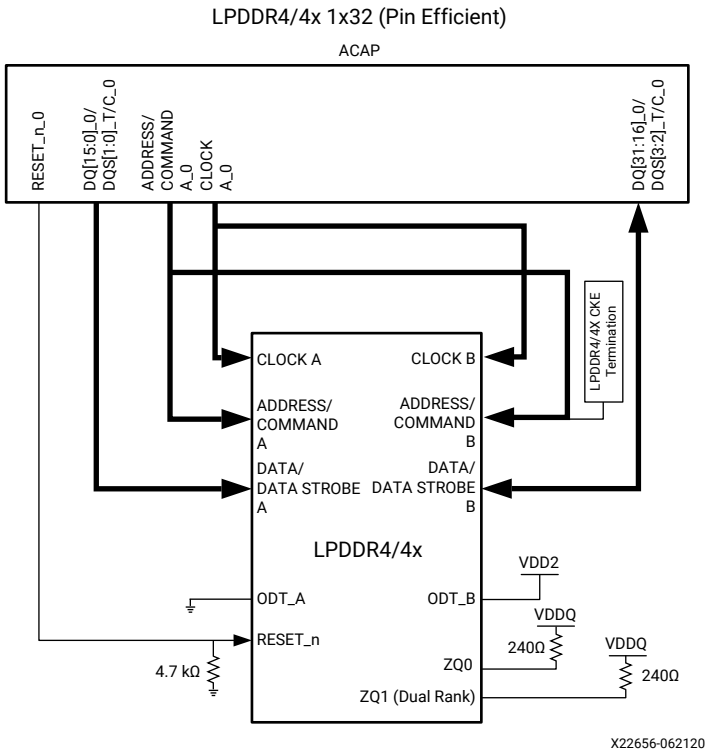


Figure 19: **Connections for a Pin Efficient 1x32 LPDDR4/4x Interface**



Physical Design Rules for LPDDR4/4x Signals

The following table defines routing rules for LPDDR4/4x signals.

Table 15: **Physical Design Rules for LPDDR4/4x Signals**

Parameter	Value
Impedance Rules	
Impedance for single-ended CAC[1] and data signals	45Ω ±10%
Impedance for differential clock and data strobe signals	82Ω ±10%
Trace Length Rules (from ACAP to Furthest Device or Termination)	
Maximum PCB trace length for CAC signals	2600 mil
Maximum PCB trace length for data signals	2600 mil
Spacing Rules for CAC and Clock Signals	
Minimum spacing between CAC signals within the same channel[2]	2H[3], except: 1H under ACAP or LPDDR4/4x device
Minimum spacing between CAC signals and clock signals within the same channel[2]	5H[3], except: 2H under ACAP or LPDDR4/4x device
Minimum spacing between CAC/clock signals and data/strobe signals within the same channel[2]	7H[3], except: 2H under ACAP or LPDDR4/4x device
Spacing Rules for Data and Data Strobe Signals	
Minimum spacing between data signals within the same byte	2H[3], except: 1H under ACAP or LPDDR4/4x Device
Minimum spacing between data signals and data strobe signals within the same byte	5H[3], except: 1H under ACAP or LPDDR4/4x device
Minimum spacing between data/strobe signals between different bytes	7H[3], except: 2H under ACAP or LPDDR4/4x device
Minimum spacing between data/strobe signals and other signals within the same channel[2]	7H[3], except: 2H under ACAP or LPDDR4/4x device
Spacing Rules for Signals between Channels or Memory Interfaces	
Minimum spacing between signals in one memory interface to signals in another channel or memory interface	7H[3], except: 2H under ACAP or LPDDR4/4x device
Maximum Vias per Signal	
CAC signals and clock signals	2 each, except: 4 for signals touching more than one channel, such as with pin-efficient pinouts
CKE signals	3 each
Data and strobe signals	2 each
Other Physical Design Requirements	
Do not route CAC/clock signals on more than one internal signal layer	
Route all data/strobe signals with a byte on one internal signal layer	

Table 15: **Physical Design Rules for LPDDR4/4x Signals** *(cont'd)*

Parameter	Value
Route data/strobe signals on internal layers as close to the memory devices as possible	

Notes:

1. CAC stands for command/address/control.
2. A channel is defined as either the "A" side of the LPDDR4/4x device or the "B" side of the LPDDR4/4x device.
3. H is the distance to the nearest ground return plane.

Timing Constraint Rules for LPDDR4/4x Signals

The following table defines timing constraints for various signal groups and their targets, similar to how they would be entered into PCB layout software tools. ACAP package delays should always be included for purposes of determining skews.

Table 16: **Skew Constraint Rules for LPDDR4/4x Signals**[1]

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address to Clock A	ACAP to LPDDR4/4x Device	–100	+100	CA[5:0]_A	CK_T_A
Address to Clock B	ACAP to LPDDR4/4x Device	–100	+100	CA[5:0]_B	CK_T_B
Command to Clock A	ACAP to LPDDR4/4x Device	–20	+20	CKE0_A CKE1_A[2] CS0_A CS1_A[2]	CK_T_A
Command to Clock B	ACAP to LPDDR4/4x Device	–20	+20	CKE0_B CKE1_B[2] CS0_B CS1_B[2]	CK_T_B
Clock (A or B)[3]	ACAP to LPDDR4/4x Device	0	2	CK_T_A/B CK_C_A/B	-
Data to DQS0	ACAP to LPDDR4/4x Device	–100	+100	DQ[7:0] DM0	DQS0_T
Data to DQS1	ACAP to LPDDR4/4x Device	–100	+100	DQ[15:8] DM1	DQS1_T
Data to DQS2	ACAP to LPDDR4/4x Device	–100	+100	DQ[23:16] DM2	DQS2_T
Data to DQS3	ACAP to LPDDR4/4x Device	–100	+100	DQ[31:24] DM3	DQS3_T
DQS0[3]	ACAP to LPDDR4/4x Device	0	2	DQS0_T DQS0_C	-
DQS1[3]	ACAP to LPDDR4/4x Device	0	2	DQS1_T DQS1_C	-
DQS2[3]	ACAP to LPDDR4/4x Device	0	2	DQS2_T DQS2_C	-

Table 16: **Skew Constraint Rules for LPDDR4/4x Signals[1]** *(cont'd)*

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
DQS3[3]	ACAP to LPDDR4/4x Device	0	2	DQS3_T DQS3_C	
DQS0 to Clock A[3]	ACAP to LPDDR4/4x Device	–150	+150	DQS0_T	CK_A
DQS1 to Clock A[3]	ACAP to LPDDR4/4x Device	–150	+150	DQS1_T	CK_A
DQS2 to Clock B[3]	ACAP to LPDDR4/4x Device	–150	+150	DQS2_T	CK_B
DQS3 to Clock B[3]	ACAP to LPDDR4/4x Device	–150	+150	DQS3_T	CK_B

Notes:

1. Include ACAP package delays for all skew calculations.
2. These signals are only present on dual rank devices.
3. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.

PCB Routing Guidelines for RLDRAM3 Interfaces

This section provides PCB design guidelines for RLDRAM3 (RLD3) interfaces. Connections between the ACAP and RLD3 device(s) are defined, along with physical design rules and timing constraints.

Signals and Connections for RLDRAM3 Interfaces

The required signals used in RLD3 applications are shown in the following table. Signal options are shown for both 36-bit and 18-bit RLD3 devices.

Table 17: **RLD3 Signal Definitions**

Signal	Description	Required PCB Termination	Signal Routing Methodology
Clock Signals			
CK/CK_B	Address/Command Clock	See Figure 11	Fly-by
DK/DK_B[1:0]	Data Write Clock	None, uses ODT	Point-to-Point
QK/QK_B[3:0] (36-bit) QK/QK_B[1:0] (18-bit)	Data Read Clock	None, uses ODT	Point-to-Point
Address Signals			
A[20:0]	Address	39Ω to VTT at far end	Fly-by
BA[3:0]	Bank Address	39Ω to VTT at far end	Fly-by
Command/Control Signals			
CS_B	Chip Select	39Ω to VTT at far end	Fly-by
REF_B	Refresh	39Ω to VTT at far end	Fly-by
WE_B	Write Enable	39Ω to VTT at far end	Fly-by
Data Signals			
DQ[35:0] (36-bit) DQ[17:0] (18-bit)	Data	None, uses ODT	Point-to-point
DM[1:0]	Data Mask	None, uses ODT	Point-to-point
QVLD/QVLD[1:0]	Data Valid	None	Not used
Miscellaneous Signals			
RESET_B	Reset	4.7 kΩ to GND at far end	Fly-by
RLD3 Devices Only			
ZQ	External Impedance	240Ω to GND	One per memory device
MF	Mirror Function	Direct to GND or through 0Ω resistor for fly-by. See Figure 20 for clamshell.	One per memory device or shared fly-by

Table 17: **RLD3 Signal Definitions** *(cont'd)*

Signal	Description	Required PCB Termination	Signal Routing Methodology
ACAPs Only			
IO_VP_700 IO_VP_800 (if present)	Calibration Reference	240Ω to VCCO_700 240Ω to VCCO_800 (if present)	

A common usage for RLDRAM3 is a x72 architecture composed of two x36 RLD3 devices. The following figures show the connections for clamshell and fly-by configurations, respectively.

Figure 20: **Clamshell RLDRAM3 Memory with Width Expansion**

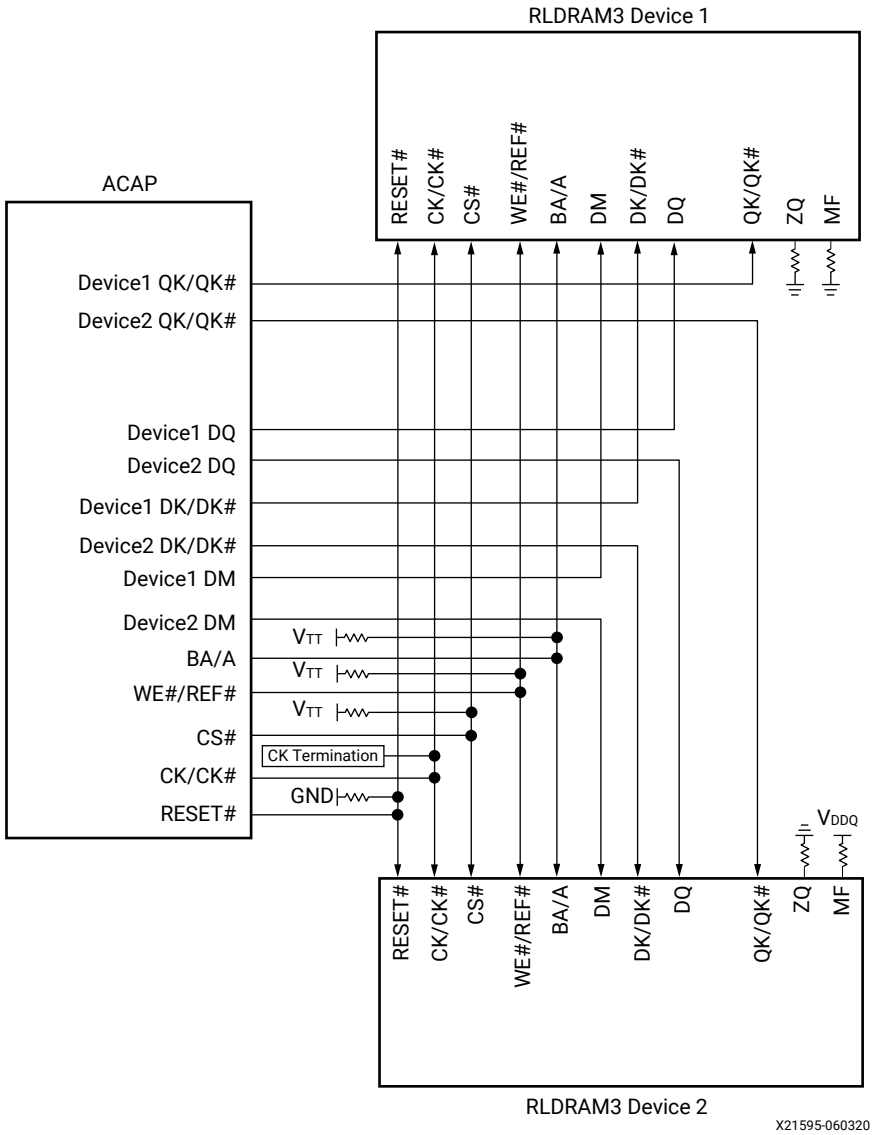
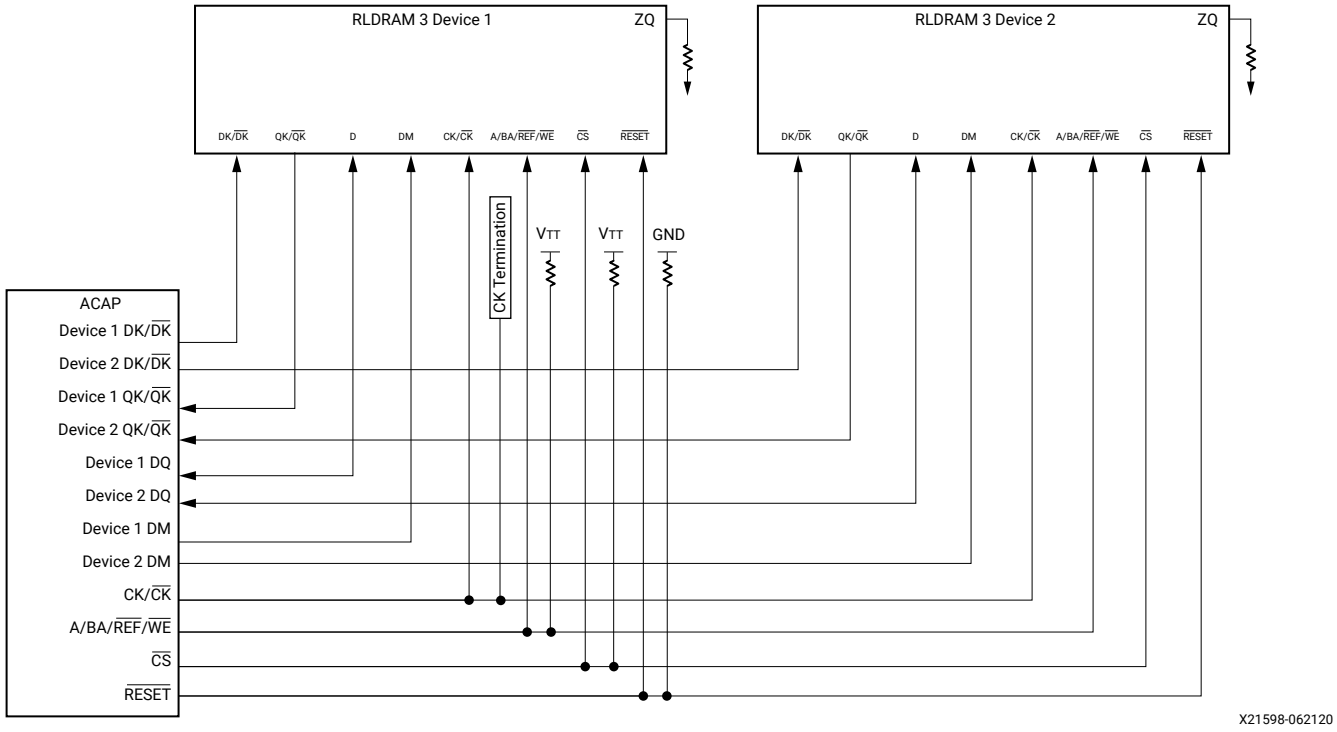


Figure 21: **Fly-by RLDRAM3 Memory with Width Expansion**



Physical Design Rules for RLDRAM3 Signals

The following table defines routing rules for RLD3 signals.

Table 18: **Physical Design Rules for RLD3 Signals**

Parameter	Value
Impedance Rules	
Impedance for single-ended address/command/control and data signals	50Ω[1] ± 10%
Impedance for differential clock (CK), data write clock (DK), and data read clock (QK)	90Ω[1] ± 10%
Maximum Trace Length Rules	
Maximum PCB trace length for all signals	5000 mil
Spacing Rules for Address/Command/Control Signals	
Minimum spacing between address/command/control signals	3H[2], except: 1H under ACAP 1H under DDR4 device
Minimum spacing between address/command/control and other signal types	5H, except: 2H under ACAP 2H under DDR4 device
Spacing Rules for Data Signals	
Minimum spacing between data/DK/QK signals within the same byte	3H, except: 1H under ACAP 1H under DDR4 device
Minimum spacing between data/DK/QK signals between different bytes	5H, except: 2H under ACAP 2H under DDR4 device
Minimum spacing between data/DK/QK signals and other signal types	5H, except: 2H under ACAP 2H under DDR4 device
Routing Notes	
x18 Devices	
DQ[8:0], DK0, DK0_B, DM0, QK0, QK0_B	Must be routed on the same layer
DQ[17:9], DK1, DK1_B, DM1, QK1, QK1_B	Must be routed on the same layer
x36 Devices	
DQ[8:0], DQ[26:18], DK0, DK0_B, DM0, QK0, QK0_B, QK2, QK2_B	Must be routed on the same layer
DQ[17:9], DQ[35:27], DK1, DK1_B, DM1, QK1, QK1_B, QK3, QK3_B	Must be routed on the same layer

Notes:

1. Up to 60Ω (single-ended) or 120Ω (differential) under ACAP or DRAM devices, taking into account PCB manufacturing tolerances.
2. H is the distance to the nearest ground return plane.

Timing Constraint Rules for RLDRAM3 Signals

The following tables define timing constraints for various groups and their targets, similar to how they would be entered into PCB layout software tools. ACAP package delays should always be included for purposes of determining skews.

Table 19: **Skew Constraint Rules for RLDRAM3 Signals (x18 Devices)[1]**

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address/Command to Clock	ACAP to RLD3 device	–8	+8	A[20:0] BA[3:0] CS_B REF_B WE_B	CK
Data to DK0	ACAP to RLD3 device	–100	+100	DQ[8:0] DM0	DK0
Data to DK1	ACAP to RLD3 device	–100	+100	DQ[17:9] DM1	DK1
Data to QK0	ACAP to RLD3 device	–100	+100	DQ[8:0]	QK0
Data to QK1	ACAP to RLD3 device	–100	+100	DQ[17:9]	QK1
Data Write Clocks to Address/Command Clock	ACAP to RLD3 device	–110	+110	DK0 DK1	CK
Data Read Clocks to Address/Command Clock	ACAP to RLD3 device	-85	+85	QK0 QK1	CK
Clock[2]	ACAP to RLD3 device	0	2	CK CK_B	-
DK0[2]	ACAP to RLD3 device	0	2	DK0 DK0_B	-
DK1[2]	ACAP to RLD3 device	0	2	DK1 DK1_B	-
QK0[2]	ACAP to RLD3 device	0	2	QK0 QK0_B	-
QK1[2]	ACAP to RLD3 device	0	2	QK1 QK1_B	-

Notes:

1. Include ACAP package delays for all skew calculations.
2. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.

Table 20: **Skew Constraint Rules for RLDRAM3 Signals (x36 Devices)**[1]

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address/Command to Clock	ACAP to RLD3 device	–8	+8	BA[3:0] A[20:0] CS_B REF_B WE_B	CK
Data to DK0	ACAP to RLD3 device	–100	+100	A[20:0] DQ[8:0] DQ[26:18] DM0	DK0
Data to DK1	ACAP to RLD3 device	–100	+100	DQ[17:9] DQ[35:27] DM1	DK1
Data to QK0	ACAP to RLD3 device	–100	+100	DQ[8:0]	QK0
Data to QK1	ACAP to RLD3 device	–100	+100	DQ[17:9]	QK1
Data to QK2	ACAP to RLD3 device	–100	+100	DQ[26:18]	QK2
Data to QK3	ACAP to RLD3 device	–100	+100	DQ[35:27]	QK3
Data Write Clocks to Address/Command Clock	ACAP to RLD3 device	–110	+110	DK0 DK1	CK
Data Read Clocks to Address/Command Clock	ACAP to RLD3 device	-85	+85	QK0 QK1 QK2 QK3	CK
Clock[2]	ACAP to RLD3 device	0	2	CK CK_B	-
DK0[2]	ACAP to RLD3 device	0	2	DK0 DK0_B	-
DK1[2]	ACAP to RLD3 device	0	2	DK1 DK1_B	-
QK0[2]	ACAP to RLD3 device	0	2	QK0 QK0_B	-
QK1[2]	ACAP to RLD3 device	0	2	QK1 QK1_B	-
QK2[2]	ACAP to RLD3 device	0	2	QK2 QK2_B	-
QK3[2]	ACAP to RLD3 device	0	2	QK3 QK3_B	-

Notes:

1. Include ACAP package delays for all skew calculations.
2. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.

PCB Routing Guidelines for QDR-IV Interfaces

This section provides PCB design guidelines for QDR-IV interfaces. Connections between the ACAP and QDR-IV device(s) are defined, along with physical design rules and timing constraints.

Signals and Connections for QDR-IV Applications

The following table shows the required signals used in QDR-IV applications. Applications include 2x18 (36-bit) interfaces as well as 2x36 (72-bit) interfaces.

Table 21: **QDR-IV Signal Definitions**

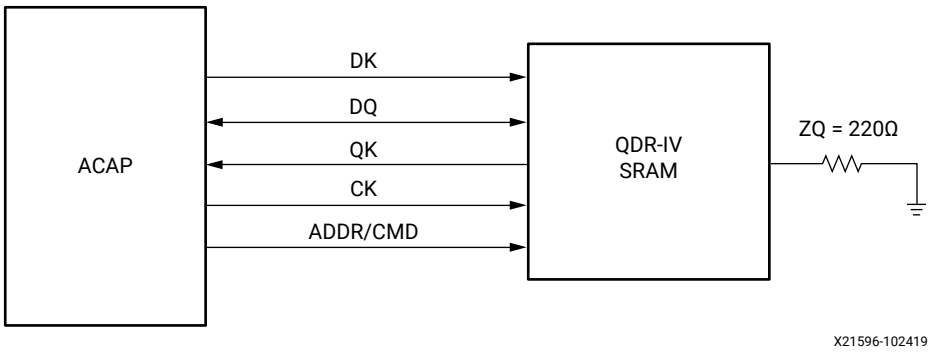
Signal	Description	Required PCB Termination	Signal Routing Methodology
Clock Signals			
CK_P/CK_N	Address/Command Clock	None, uses ODT	Point-to-Point
DKA_P/N[1:0] DKB_P/N[1:0]	Data Write Clock	None, uses ODT	Point-to-Point
QKA_P/N[1:0] QKB_P/N[1:0]	Data Read Clock	None, uses ODT	Point-to-Point
Address Signals			
A[21:0] (2x18, 36-bit) A[20:0] (2x36, 72-bit)	Address	None, uses ODT	Point-to-Point
Command Signals			
AP	Address Parity	None, uses ODT	Point-to-Point
AINV	Address Inversion	None, uses ODT	Point-to-Point
CFG_N	Mode Register Configuration	None, uses ODT	Point-to-Point
LBK0_N LBK1_N	Loopback Mode for Addr/Cmd/CK deskew	None, uses ODT	Point-to-Point
LDA_N LDB_N	Synchronous Load	None, uses ODT	Point-to-Point
RWA_N RWB_N	Synchronous Read/Write	None, uses ODT	Point-to-Point
Data Signals			
DQA[17:0] (2x18, 36-bit) DQB[17:0] (2x18, 36-bit) DQA[35:0] (2x36, 72-bit) DQB[35:0] (2x36, 72-bit)	Data	None, uses ODT	Point-to-point
QVLDA[1:0] QVLDB[1:0]	Output Data Valid	None, uses ODT	Point-to-Point
Miscellaneous Signals			
RST_N	Reset	4.7 kΩ to GND at far end	Pull-down
PE_N	Address Parity Error Output	None, direct connection	Point-to-point

Table 21: **QDR-IV Signal Definitions** *(cont'd)*

Signal	Description	Required PCB Termination	Signal Routing Methodology
QDR-IV Devices Only			
DINVA[1:0] DINVB[1:0]	Data Inversion	Tie each to GND via 100Ω	Pull-down
ZQ_ZT	External Impedance	Tie 220Ω to GND	One per device
ACAP Device Only			
IO_VP_700 IO_VP_800 (if present)	Calibration Reference	240Ω to VCCO_700 240Ω to VCCO_800 (if present)	

The following figure shows conceptual point-to-point routing for QDR-IV devices.

Figure 22: **Point-to-Point Connections for QDR-IV Devices**



Physical Design Rules for QDR-IV Signals

The following table defines routing rules for QDR-IV signals.

Table 22: **Physical Design Rules for QDR-IV Signals**

Parameter	Value
Impedance Rules	
Impedance for single-ended address/command/control and data signals	50Ω[1] ± 10%
Differential impedance for clock (CK), data write clock (DK), and data read clock (QK)	90Ω[1] ± 10%
Maximum Trace Length Rules	
Maximum PCB trace length for all signals	5000 mil
Spacing Rules for Address/Command/Control Signals	
Minimum spacing between address/command/control signals	3H[2], except 1H under ACAP or QDR-IV device
Minimum spacing between address/command/control signals and other signals	5H[2], except 2H under ACAP or QDR-IV device
Spacing Rules for Data Signals	
Minimum spacing between data signals and DK/QK signals within the same byte	3H[2], except 1H under ACAP or QDR-IV device
Minimum spacing between data signals and DK/QK signals between different bytes	5H[2], except 2H under ACAP or QDR-IV device
Minimum spacing between data signals and DK/QK signals and other signals	5H[2], except 2H under ACAP or QDR-IV device
Routing Notes for 2x18 (36-bit) Interfaces	
DQA[8:0], DKA0_P, DKA0_N, QKA0_P, QKA0_N, QVLDA[0]	Must be routed on the same routing layer
DQA[17:9], DKA1_P, DKA1_N, QKA1_P, QKA1_N, QVLDA[1]	Must be routed on the same routing layer
DQB[8:0], DKB0_P, DKB0_N, QKB0_P, QKB0_N, QVLDB[0]	Must be routed on the same routing layer
DQB[17:9], DKB1_P, DKB1_N, QKB1_P, QKA1_N, QVLDB[1]	Must be routed on the same routing layer
Routing Notes for 2x36 (72-bit) Interfaces	
DQA[17:0], DKA0_P, DKA0_N, QKA0_P, QKA0_N, QVLDA[0]	Must be routed on the same routing layer
DQA[35:18], DKA1_P, DKA1_N, QKA1_P, QKA1_N, QVLDA[1]	Must be routed on the same routing layer
DQB[17:0], DKB0_P, DKB0_N, QKB0_P, QKB0_N, QVLDB[0]	Must be routed on the same routing layer
DQB[35:18], DKB1_P, DKB1_N, QKB1_P, QKA1_N, QVLDB[1]	Must be routed on the same routing layer

Notes:

1. Up to 60Ω (single-ended) or 120Ω (differential) under ACAP or DRAM devices, taking into account PCB manufacturing tolerances.
2. H is the distance to the nearest ground return plane.

Timing Constraint Rules for QDR-IV Signals

The timing constraints are defined in the following tables for various signal groups and their targets, similar to how they would be entered into PCB layout software tools. ACAP package delays should always be included for purposes of determining skews.

Table 23: **Skew Constraint Rules for 2x18 (36-bit) QDR-IV Signals**[1]

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address to Clock	ACAP to QDR-IV device	–6	+6	A[21:0] AP AINV CFG_N LBK0_N LBK1_N LDA_N LDB_N RWA_N RWB_N	CK_P
Data to DKA0	ACAP to QDR-IV device	–5	+5	DQA[8:0]	DKA_P0
Data to DKA1	ACAP to QDR-IV device	–5	+5	DQA[17:9]	DKA_P1
Data to DKB0	ACAP to QDR-IV device	–5	+5	DQB[8:0]	DKB_P0
Data to DKB1	ACAP to QDR-IV device	–5	+5	DQB[17:9]	DKB_P1
Data to QKA0	ACAP to QDR-IV device	–5	+5	DQA[8:0] QVLDA[0]	QKA_P0
Data to QKA1	ACAP to QDR-IV device	–5	+5	DQA[17:9] QVLDA[1]	QKA_P1
Data to QKB0	ACAP to QDR-IV device	–5	+5	DQB[8:0] QVLDB[0]	QKB_P0
Data to QKB1	ACAP to QDR-IV device	–5	+5	DQB[17:9] QVLDB[1]	QKB_P1
DK to CK	ACAP to QDR-IV device	0	+50	DKA0_P DKA1_P DKB0_P DKB1_P	CK_P
QK to CK	ACAP to QDR-IV device	0	+50	QKA0_P QKA1_P QKB0_P QKB1_P	CK_P
Clock[2]	ACAP to QDR-IV device	0	2	CK_P CK_N	-
DKA0[2]	ACAP to QDR-IV device	0	2	DKA0_P DKA0_N	–

Table 23: **Skew Constraint Rules for 2x18 (36-bit) QDR-IV Signals[1]** *(cont'd)*

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
DKA1[2]	ACAP to QDR-IV device	0	2	DKA1_P DKA1_N	–
DKB0[2]	ACAP to QDR-IV device	0	2	DKB0_P DKB0_N	–
DKB1[2]	ACAP to QDR-IV device	0	2	DKB1_P DKB1_N	–
QKA0[2]	ACAP to QDR-IV device	0	2	QKA0_P QKA0_N	–
QKA1[2]	ACAP to QDR-IV device	0	2	QKA1_P QKA1_N	–
QKB0[2]	ACAP to QDR-IV device	0	2	QKB0_P QKB0_N	–
QKB1[2]	ACAP to QDR-IV device	0	2	QKB1_P QKB1_N	–

Notes:

1. Include ACAP package delays for all skew calculations.
2. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.

Table 24: **Skew Constraint Rules for 2x36 (72-bit) QDR-IV Signals[1]**

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Address to Clock	ACAP to QDR-IV device	–6	+6	A[20:0] AP AINV CFG_N LBK0_N LBK1_N LDA_N LDB_N RWA_N RWB_N	CK_P
Data to DKA0	ACAP to QDR-IV device	–5	+5	DQA[17:0]	DKA_P0
Data to DKA1	ACAP to QDR-IV device	–5	+5	DQA[35:18]	DKA_P1
Data to DKB0	ACAP to QDR-IV device	–5	+5	DQB[17:0]	DKB_P0
Data to DKB1	ACAP to QDR-IV device	–5	+5	DQB[35:18]	DKB_P1
Data to QKA0	ACAP to QDR-IV device	–5	+5	DQA[17:0] QVLDA[0]	QKA_P0

Table 24: **Skew Constraint Rules for 2x36 (72-bit) QDR-IV Signals[1]** *(cont'd)*

Skew Constraint	Pin Pair Set	Minimum (ps)	Maximum (ps)	Group	Target
Data to QKA1	ACAP to QDR-IV device	–5	+5	DQA[35:18] QVLDA[1]	QKA_P1
Data to QKB0	ACAP to QDR-IV device	–5	+5	DQB[17:0] QVLDB[0]	QKB_P0
Data to QKB1	ACAP to QDR-IV device	–5	+5	DQB[35:18] QVLDB[1]	QKB_P1
DK to CK	ACAP to QDR-IV device	0	+50	DKA0_P DKA1_P DKB0_P DKB1_P	CK_P
QK to CK	ACAP to QDR-IV device	0	+50	QKA0_P QKA1_P QKB0_P QKB1_P	CK_P
Clock[2]	ACAP to QDR-IV device	0	2	CK_P CK_N	-
DKA0[2]	ACAP to QDR-IV device	0	2	DKA0_P DKA0_N	–
DKA1[2]	ACAP to QDR-IV device	0	2	DKA1_P DKA1_N	–
DKB0[2]	ACAP to QDR-IV device	0	2	DKB0_P DKB0_N	–
DKB1[2]	ACAP to QDR-IV device	0	2	DKB1_P DKB1_N	–
QKA0[2]	ACAP to QDR-IV device	0	2	QKA0_P QKA0_N	–
QKA1[2]	ACAP to QDR-IV device	0	2	QKA1_P QKA1_N	–
QKB0[2]	ACAP to QDR-IV device	0	2	QKB0_P QKB0_N	–
QKB1[2]	ACAP to QDR-IV device	0	2	QKB1_P QKB1_N	–

Notes:

1. Include ACAP package delays for all skew calculations.
2. It does not matter which signal is faster or slower, but the difference in time between the two should be no longer than specified.

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Chapter 4

PCB Guidelines for PS, PMC, MIPI, and GTY/GTYP Transceiver Interfaces

This chapter lists PCB layout guidelines specific to the PS/PMC multiplexed I/O (MIO) and GTY/GTYP transceiver interfaces in Versal ACAPs.

IMPORTANT! *Refer to Versal ACAP Technical Reference Manual (AM011) for architectural descriptions of each peripheral interface listed in this chapter.*

IMPORTANT! *All GTY/GTYP transceiver interfaces mentioned in this chapter refer to Versal ACAP GTY Transceivers Architecture Manual (AM002).*

GTY/GTYP Transceiver Interfaces

For GTY/GTYP transceiver interfaces such as DisplayPort, SGMII, PCIe®, SATA, and USB3.0, refer to *Versal ACAP GTY Transceivers Architecture Manual* (AM002).

PMC Dedicated Pins

Versal ACAP dedicated pins assist with system management. There are 15 dedicated I/O in the PMC power domain. The dedicated pins provide key functions such as boot mode selection, external reference clock input, power-on reset input, JTAG interface, status signals, error signals, and crystal oscillator pins for the real-time clock (RTC).

- Connect DONE to a 4.7 kΩ pull-up resistor to VCCO_503 near the Versal ACAP.
- Connect ERROR_OUT to a 4.7 kΩ pull-up resistor to VCCO_503 near the Versal ACAP.
- Connect POR_B to a 4.7 kΩ pull-up resistor to VCCO_503 near the Versal ACAP.
- Place 4.7 kΩ pull-up resistors on the TMS, TCK, and TDI lines to VCCO_503 near the Versal ACAP.

- Connect REF_CLK to a clock generator providing a 27–60 MHz clock (typically 33 MHz). The clock must be a single-ended LVCMOS signal using the same voltage level as VCCO_503. Signal integrity analysis should be run to determine the need for clock buffering and/or termination. Termination can be either a series termination at the clock source or a Thevenin termination as close as possible to the REF_CLK pin of the ACAP. See Versal ACAP data sheets for timing information for REF_CLK.
- For real-time clock (RTC) specifications, including resistor and capacitor values, refer to the Versal ACAP data sheets.

CAN FD

A level shifter must be implemented if using a CAN PHY that operates at a voltage higher than the Versal ACAP.

Gigabit Ethernet MAC 10/100/1000 RGMII

- Skew between GEMx_TX_DATA[0:3]/GEMx_TX_CTRL and GEMx_TX_CLK should be within ±50 ps.
- Skew between GEMx_RX_DATA[0:3]/GEMx_RX_CTRL and GEMx_RX_CLK should be within ±50 ps.
- Trace delays should be within 1.5s – 2.1 ns (~9 – 12") for all signals.
- Include Versal ACAP package delays for all skew and trace delay calculations.

I2C

- Place 4.7 kΩ pull-up resistors at the far end of the serial clock lines (LPD_I2Cx_SCL) and serial data lines (LPD_I2Cx_SDA) furthest from the Versal ACAP.
- A level-shifter/repeater might be required depending on the particular multiplexers used.

MIPI

- Skew between clock and data should be within ± 2 ps.
- Include ACAP package delays for all skew and trace delay calculations.

Octal SPI

- Skew between OSPI_IO[7:0]/OSPI_DS and OSPI_CLK should be within ±50 ps for production silicon.

  ***Note*:** For ES1 silicon, an additional delay of 890–990 ps is required on OSPI_CLK with respect to OSPI_IO[7:0]/OSPI_DS.

- Trace delays should be between 500 ps (3.0 inches) to 1.3 ns (7.8 inches) for all signals

  ***Note*:** For ES1 silicon, an additional delay of 890–990 ps is required on OSPI_CLK.

- Include ACAP package delays for all skew and trace delay calculations.
- It is highly recommended to perform a signal integrity analysis on the clock line at the near end (close to the Versal ACAP) and far end.

Table 25: **OSPI Board Delay Guidelines**

OSPI Operating Mode	PCB Trace Delay Guideline (ACAP to QSPI)	Maximum OSPI Operating Frequency
SDR ≤ 50 MHz	0.5 ns – 1.3 ns[1]	1/(20 ns + (2 × PCB Trace Delay (ns) – 2.6 ns) + 2 × (Tspicto (ns) – 6 ns))[2, 3]
SDR 50 MHz – 166 MHz	0.5 ns – 1.3 ns	See note 4
DDR 50 MHz – 200 MHz	0.5 ns – 1.3 ns	See note 4

Notes:

1. The guidelines for SDR ≤ 50 MHz assume a flash clock-to-out time of ≤ 6 ns. If the flash clock-to-out time is greater than 6 ns and/or if the PCB trace delays are outside of the listed ranges, refer to the Maximum OSPI Operating Frequency column to determine the maximum operating frequency.
2. Use this equation to determine maximum OSPI operating frequency for this mode if the flash device clock-to-out is greater than 6 ns and/or if the trace delay guidelines in the PCB Trace Delay column cannot be met.
3. Tspicto refers to the clock-to-out time for the flash device.
4. Due to RX tuning, the maximum frequency is not a function of the PCB trace delay, though it is advised to keep the trace delay within the specified guideline.

CAUTION! *To boot the Versal ACAP in OSPI boot mode, the octal SPI flash must be compatible and support the SDR commands listed in the Octal SPI Boot Mode section in Versal ACAP Technical Reference Manual (AM011).*

Quad SPI

- Skew between QSPIx_IO[3:0] and QSPIx_CS_b lines relative to QSPIx_CLK should be within ±50 ps. Include ACAP package delays for all skew calculations.
- Keep QSPI_LPBK_CLK (MIO[6]) unconnected for higher operating QSPIx_CLK frequencies (> 37.5 MHz). This allows the loopback feature to work properly.

- It is highly recommended to perform a signal integrity analysis on the QSPIx_CLK line(s) at the near end (close to the Versal ACAP) and far end.
- Place 4.7 kΩ pull-up resistors to VCCO_503 on the QSPIx_IO[3], Write Protect/QSPIx_IO[2], and QSPIx_CS_b lines. QSPIx_IO[3] is shared with HOLD, and QSPIx_IO[2] is shared with the Write Protect function.
- For optimum performance, limit trace delays to 0.5 ns between the ACAP and QSPI device. Refer to the following table for specific trace delay guidelines based on intended operating mode.

Table 26: **QSPI Board Delay Guidelines**

QSPI Operating Mode	PCB Trace Delay Guideline (ACAP to QSPI)[1]	Maximum QSPI Operating Frequency[2, 3]
≤ 37.5 MHz	0.5 ns – 1.3 ns	1/(26.66 ns + 2 × (2 × PCB Trace Delay (ns) – 2.6 ns) + 2 × (Tspicto (ns) – 6 ns))
37.5 MHz – 100 MHz	0.5 ns – 1.0 ns	1/(10 ns + (2 × PCB Trace Delay (ns) – 2 ns) + (Tspicto (ns) – 6 ns))
100 MHz – 150 MHz	0.5 ns	1/(6.66 ns + (2 × PCB Trace Delay (ns) – 1 ns) + (Tspicto (ns) – 6 ns))

Notes:

1. The guidelines in this column assume a flash clock-to-out time of ≤ 6 ns. If the flash clock-to-out time is greater than 6 ns and/or if the PCB trace delays are outside of the listed ranges, refer to the Maximum QSPI Operating Frequency column to determine the maximum operating frequency for the intended operating mode.
2. Use the equations in this column to determine the maximum QSPI operating frequency if the flash device clock-to-out is greater than 6 ns and/or if the trace delay guidelines in the PCB Trace Delay Guideline column cannot be met.
3. Tspicto refers to the clock-to-out time for the flash device.

SD/SDIO/eMMC

eMMC

- Pull-up resistors are required on data[0–7] per JEDEC specification JESD84-B51A, Embedded Multi-media Card (eMMC), Electrical Standard (5.1).
- A 30Ω series resistor should be placed on the eMMCx_CLK, eMMCx_CMD, and eMMCx_DATA[7:0] lines, as close to the ACAP pins as possible.

Legacy and High-Speed SDR eMMC Interfaces

- Skew between eMMCx_DATA[7:0]/eMMCx_CMD and eMMCx_CLK should be within ±100 ps.
- Trace delays should be within 0.85 ns – 1.0 ns (~5 – 6 inches) for all signals.
- Include ACAP package delays for all skew and trace delay calculations.

High-Speed 200 and High-Speed DDR eMMC Interfaces

- Skew between eMMCx_DATA[7:0]/eMMCx_CMD and eMMCx_CLK should be within ±50 ps.
- Trace delays should be within 0.85 ns – 1.0 ns (~5 – 6 inches) for all signals.
- Include ACAP package delays for all skew and trace delay calculations.

SD/SDIO

- A 30Ω series resistor should be placed on the SDx_CLK, SDx_CMD, and SDx_DATA[3:0] lines, as close to the ACAP pins as possible.
- A level shifter might be required depending on the particular voltages (such as for SD 3.0) used on the Versal ACAP and SD chip.
- Asynchronous signals SDx_DETECT and SDx_WP have no timing relationship to SDx_CLK.
- The SDx_DETECT and SDx_WP lines should both be pulled up with their own 4.7 kΩ resistors to the MIO voltage. When using microSD, SDx_WP and SDx_DETECT can be no connects.
- A 10 kΩ pull-up resistor should be added to SDx_DATA[3] on the SD card side of the level shifter.

Default, High Speed, SDR12, and SDR25 SD Interfaces

- Skew between SDx_DATA[3:0]/SDx_CMD and SDx_CLK should be within ±100 ps.
- Trace delays should be within 0.85 ns – 1.0 ns (~5 – 6 inches) for all signals.
- Include ACAP package delays for all skew and trace delay calculations.

DDR50, SDR50, and SDR104 SD Interfaces

- Skew between SDx_DATA[3:0]/SDx_CMD and SDx_CLK should be within ±50 ps.
- Trace delays should be within 0.85 ns – 1.0 ns (~5 – 6 inches) for all signals.
- Include ACAP package delays for all skew and trace delay calculations.

SPI

- Skew between SPIx_MISO/SPIx_MOSI and SPIx_CLK should be within ±100 ps.
- Trace delays should be within 0.5 ns – 1.3 ns (~ 3 – 8 inches) for all signals.
- Include ACAP package delays for all skew and trace delay calculations.
- Place a 4.7 kΩ pull-up resistor on the SS pin near the serial peripheral interface (SPI) device.

Trace Port Interface Unit

When operating the trace port interface unit (TPIU) in MIO mode, the trace clock output should be delayed by approximately one half clock period. This can be done on the PCB, or by the debugging device (ARM_DSTREAM, Lauterbach, or Agilent).

Triple Time Counter

Suggested skew between TTCx_WAVE and TTCx_CLK is within ±100 ps.

UART

Xilinx suggests keeping trace delays below 1.30 ns.

USB 2.0

ULPI Interface (60 MHz):

- Skew between USB_ULPI_DATA[7:0]/USP_ULPI_DIR/USB_ULPI_NXT/USB_ULPI_STP and USB_ULPI_CLK should be within ±100 ps.
- Trace delays should be within 0.5 ns – 1.3 ns (~ 3 – 8 inches).
- Include ACAP package delays for all skew and trace delay calculations.
- For optimum signal integrity add a 30Ω series resistor to the DATA and STP lines near the Versal ACAP.

System Windowed Watchdog Timer

Suggested skew between SWDTx_WS0/SWDTx_WS1 and SWDTx_CLK is within ±100 ps.

Migration between Versal Devices and Packages

The high-level goal of package migration is to ensure that customers can use the same PCB across different devices in a footprint compatible package. Package migration places extra design complexity on the package layout because there are stringent migration design rules in place to ensure that migration is possible across devices in a given package. Most of the packages that are being offered support migration across devices within a given Versal portfolio. However, there are packages that span across device families offering migration support.

- VSVD176: Supports migration across devices within the Versal AI Core and Prime series
- VFVA1760 and VFVC1760: Supports migration across devices within the Versal Prime and Premium series
- VSVA2197: Supports migration across devices within the Versal AI Core, Prime, and Premium series

The key high-level differences between the various Versal devices that impact PCB design from a package migration perspective are as follows:

Versal AI Core Series

- High compute series with medium density PL, connectivity capability coupled with AI and DSP acceleration engines
- AI Core devices offer only GTY transceiver support
  - Maximum GTY transceiver data rate is 32.75 Gb/s
  - No GTM transceiver support
- Package type: Bare die, lidless
- Package overhang: Yes, for selected die/package combinations
- Die type: Monolithic

Versal Prime Series

- Mid range series with medium density PL, signal processing, and connectivity capability
- Prime devices offer a combination of GTY (32.75 Gb/s) and GTM (58 Gb/s) transceiver support

- Package type: Lidded, lidless
- Package overhang: None
- Die type: Monolithic

Versal Premium Series

- Premium Series: Premium platform with maximum adaptable engines, 112G SerDes, and 600G Integrated IP
- Premium devices offer a combination of GTY (32.75 Gb/s), GTM (58 Gb/s), and GTM (112 Gb/s) transceiver support along with PCIe Gen 5 support
- Package type: Lidded, lidless
- Package overhang: None
- Die type: Monolithic, SSI technology

To enable migration between any two devices in a given package, PCB designers should be aware of any differences that exist between devices upfront for a given package. This is necessary to ensure that the PCB layout can account for these differences during the board design phase and enable seamless migration. Refer to Versal ACAP Migration Checklist and the subsequent sections that explain each item in the checklist. Some of the items in the checklist might not be applicable for a given migration scenario. However, it would be helpful to go through the checklist to identify the differences that might be applicable for your specific implementation and ensure the PCB design accounts for the differences.

Customer should also be aware that there might be differences in package height when migrating across some die/package combinations. All the devices within the AI Core and Prime series are monolithic devices. However, Premium devices are a combination of monolithic and SSI technology variants. Some packages like the VSVA2785 within the Premium family migrate between monolithic and SSI technology variants, resulting in package height differences. This difference in package height needs to be considered when designing the thermal solution to ensure the same heat sink solution works across devices while meeting any height requirements to fit into the same chassis.

Versal ACAP Migration Checklist

- Review footprint compatibility
- Review differences in XPIO, HDIO, and GTY transceiver counts
- Review package dimensions, including height and overhang
- Review additional power rail requirements
- Review differences in transceiver data rates

- Review XPIO performance differences
- Review XPIO and GTY transceiver fabric access limitations
- Review I/O bank and GT Quad number differences
- Review VCC_IO and IO_VR pin differences
- Review GT_RCAL and GT_RREF pin differences
- Review decoupling capacitor requirements
- Review package pin flight time differences between devices

Footprint Compatibility Between Packages

Any two packages with the same footprint identifier code are footprint compatible. The footprint identifier code consists of a package designator code and BGA pin count information (such as A2197, C1760, or D1760). A customer that wants pin compatibility across any two devices in a given package should select a footprint compatible package such that they can be designed to be electrically compatible. Refer to the Overview chapter of *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013) to determine which packages are footprint compatible.

Example

Table 27 shows a snippet of the Footprint Compatibility table from *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013). The VM1302 in the A1760 package is only compatible with VM1402 and VM2602 in the A1760 package, but not with any of the devices in the C1760 package. A design created with the VM1302 in the A1760 package, for example, can be footprint compatible with any bigger A1760 device.

VFVA1760	VM1302	VM1402	VM2602			
VFVC1760	VM1502	VM1802	VM2602	VM2902	VP1102	VP1402

Notes:

1. For purposes of understanding footprint compatibility and migration, only the last letter in the package name is relevant. For example, the VSVA1596 and VIVA1596 are essentially the same with regard to footprint compatibility and migration due to the last letter "A" being the same.

Differences in XPIO, HDIO, and Transceiver Count

If migrating from a bigger device to a smaller device within the same package, there exists the potential for some I/O and transceiver banks to not be bonded out or present on the smaller device. Figure 23 shows a snippet of the I/O migration table from *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013). XPIO banks 704, 705, 804, and 805 are not bonded on VM1302 in the A1760 package while the same are available on the VM1402 device. Similarly, in addition to XPIO banks 704 and 705, the VM2602 device also bonds out XPIO banks 706, 707, and 708, which are not available on the VM1302 device. There will also be differences in the number of HDIOs and transceivers that are bonded out across devices in a given footprint compatible package.

Figure 23: **Snippet of I/O Migration Table**

Package		Device	A	B	C	D	E	F	G	H	I	J	K	L	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	AM	AN	AO	AP	AQ	AR	AS	AT	AU	Unbonded
VFVA1760	A1760	XCVM1302	700	701	702	703									800	801	802	803			307															804, 704, 805, 705
VFVA1760	A1760	XCVM1402	700	701	702	703	704	705							800	801	802	803	804	805	307															
VFVA1760	A1760	XCVM2602	700	701	702	703	704	705										706	707	708	609															608

Package Dimensions

Package dimensions for Versal devices can vary from one package to another, so care must be taken in system design to ensure that changes in length, width, or height do not interfere with other components in the system. Some packages are also “overhang” packages in that their lengths and widths extend further beyond the pin array than other devices with similar pin counts. If migrating from a smaller package to a bigger package, ensure that an appropriate keep-out area is in place so that no capacitors or other components interfere with the bigger outline. Refer to the Mechanical Drawings chapter in *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013) for the dimensions of the various Versal device packages.

Example

Customers considering device migration to VC1802/VC1902 in the VIVA1596 package from VC1502/VC1702 in the VSVA1596 package must account for package footprint differences between the two packages due to package overhang. The package size for the VSVA1596 is 37.5 mm x 37.5 mm while the package size for the VIVA1596 is 40 mm x 40 mm. However, the BGA ball footprint is identical for both the packages.

Power Rail Differences

This section describes the differences among the following power rails:

- VCCSDFEC Rail
- VCCINT_GT_L/R Rail
- VCC_CPM5 Rail

VCCSDFEC Rail

The VCCSDFEC rail is an additional rail that is not present on some of the AI Core devices lacking SDFEC support. This results in some pins being designated as N/C on the package files for select AI Core devices. These N/C pins are reserved for the VCCSDFEC rail on die/package combinations offering SDFEC support within the AI Core series.

Example

Certain pins on the XCVC1502-VSVA1596 (no SDFEC) are labeled N/C while the same pins on the XCVC1702-VSVA1596 (with SDFEC) are labeled as VCCSDFEC.

VCCINT_GT_L/R Rail

VCCINT_GT_L/R is an additional rail that is not present on some of the AI Core and Prime devices lacking GTM support. This results in some pins being designated as N/C on the package files for some select die/package combinations while the same set of pins will be part of the VCCINT_GT_L/R rail on other die/package combinations with GTM transceivers. This rail can be combined with the VCCINT rail on the PCB if they are operating at the same nominal voltage.

Example

The VM1802_VSVA2197 has N/C pins while the VM2502_VSVA2197 has those same set of pins labeled as VCCINT_GT_L/R (left/right). The above difference is applicable for die/package combinations involving the VFVA1760, VFVC1760, and VSVA2197 packages migrating within the Prime family or moving from an AI Core or Prime device to a Premium device.

VCC_CPM5 Rail

VCC_CPM5 is an additional rail that is not present on devices lacking PCIe Gen 5 support. The PCIe Gen 4 block is powered by the VCCINT rail while the Premium devices offering PCIe Gen 5 support have a dedicated rail called VCC_CPM5 that powers the CPM5 block. Customers considering migration from AI Core or Prime devices in select packages to the Premium series should be aware that some of the BGA balls that are part of the VCCINT rail will get converted to the VCC_CPM5 rail. The VCC_CPM5 rail on the PCB should always be tied to the VCC_PSLP rail because the CPM5 block is not active with the VCC_PSLP rail turned off.

Following is the matrix of the rail voltage and PCIe data rate support for various speed grades:

CPM4 Block is Part of the VCCINT Rail (AI Core and Prime Series)

- PCIe Gen 3 x16 supported across all device speed grades (-1/-2/-3):
  - Supported across all VCCINT (L - 0.7V/M - 0.80V/H - 0.88V) voltage variants
- PCIe Gen 4 x8 supported across -1/-2 speed grades:
  - Supported with VCCINT set to 0.7V (L) or 0.8V (M)
- PCIe Gen 4 x16 supported across -2/-3 speed grades:
  - Supported with VCCINT set to 0.88V (H)

CPM5 Block has its Own Dedicated Power Rail (VCC_CPM5 – Premium Series)

- VCC_CPM5 rail should always be tied on the PCB to the VCC_PSLP rail across all speed grades:
  - CPM5 block will not be active with the VCC_PSLP rail powered off
- CPM5 block will support PCIe Gen 4 x16 and Gen 5 x8 under the following scenarios:
  - VCC_CPM5/VCC_PSLP rail voltage should be set to 0.88V
  - Device speed grade should be either -2 or -3
  - Supported across all VCCINT (L - 0.7V/M - 0.8V/H - 0.88V) voltage variants:
    - Need a device with CPM5/PS overdrive support (-2LHP, -2MHP) when VCCINT is set to 0.7V (L)/0.8V (M)
    - This mode enables low power VCCINT operation while enabling PCIe Gen 5 support)
  - CPM5 support also enabled for -2HP/-3HP device variants:
    - Higher VCCINT performance/power compared to the above device variants

Differences in Transceiver Data Rates

Customers can expect GTY (32.75 Gb/s) transceivers or a combination of GTY and GTM (58 Gb/s) transceivers when moving from one device to another within a footprint compatible package. The total number of transceivers present might also vary depending on the die/package combination.

Example

VM1802_VSVA2197 has 44 GTY transceivers while VM2502_VSVA2197 has 16 GTY and 16 GTM transceivers (58 Gb/s). VM1502_VFVC1760 has 44 GTY transceivers while VM2902_VFVC1760 has 8 GTY and 40 GTM transceivers (58 Gb/s).

On the Premium devices, four 58 Gb/s GTM transceivers per Quad transition to two GTM transceivers per Quad operating at 112 Gb/s.

Differences in XPIO Performance

In select die/package combinations, customers can expect some performance differences in XPIO capability for LPDDR4 implementation when moving from one device to another within a footprint compatible package.

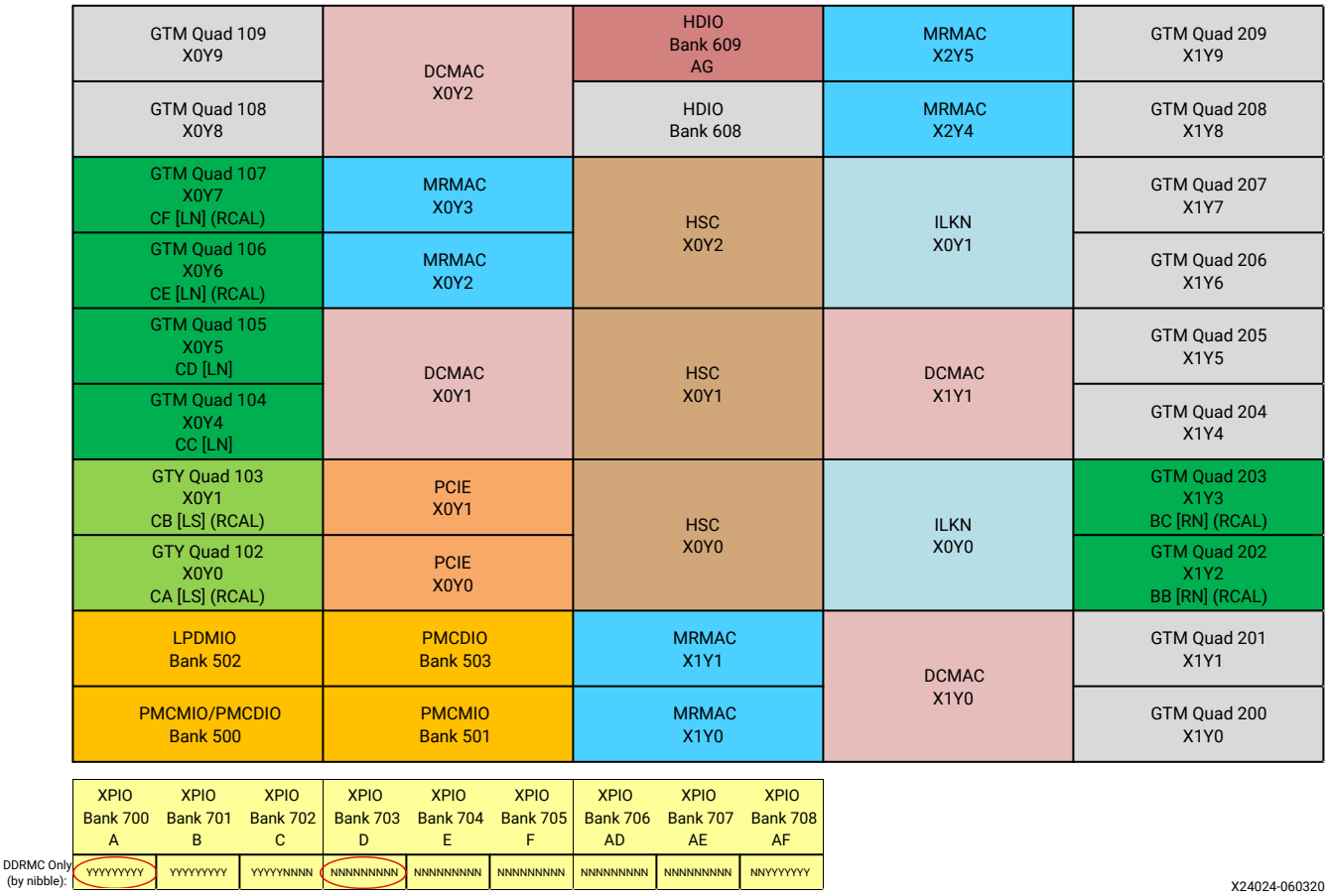
Example

All the 648 XPIOs on the VM1402_A1760 can support a maximum data rate of 4266 Mb/s for LPDDR4 implementation. However, out of 486 total XPIOs on the VM2602_A1760 package, 324 XPIOs support a maximum data rate of 4266 Mb/s for LPDDR4 implementation while the remaining 162 XPIOs can support 3200 Mb/s.

XPIO Bank Fabric Access Limitations

Users should be aware that not all XPIO banks are fabric accessible because some XPIO banks are accessible only by the hardened memory controller with no access to the fabric. The following figure shows a die/package floorplan highlighting which nibbles in a given I/O bank are fabric accessible and which ones are not. An XPIO bank contains 54 I/Os divided into nine nibbles with each nibble containing six I/Os.

Figure 24: **VM2602_A1760 Floorplan**



The nine *YYYYYYYYY* next to I/O bank 700 indicate that all the nine nibbles are accessible only by the DDR memory controller with no fabric access while the nine *NNNNNNNNN* next to bank 703 indicate that all the nine nibbles in this I/O bank are fabric accessible in addition to having access to the hardened memory controller. Users should pay attention to these differences when migrating across devices in a given package.

GTY Transceiver Fabric Access Limitations

Some of the GTY transceivers present on the different die/package combinations are not fabric accessible and connect only to the CPM5 block.

All the GTY transceivers (8) on the VP1402_A2785 are fabric accessible while only 12 out of 28 GTY transceivers on the VP1502_A2785 are fabric accessible with the remaining 16 connected to the CPM5 block. The following figures show the respective die/package floorplans with the GTYP Quad and hard block locations.

Figure 25: **VP1402_A2785 Floorplan**

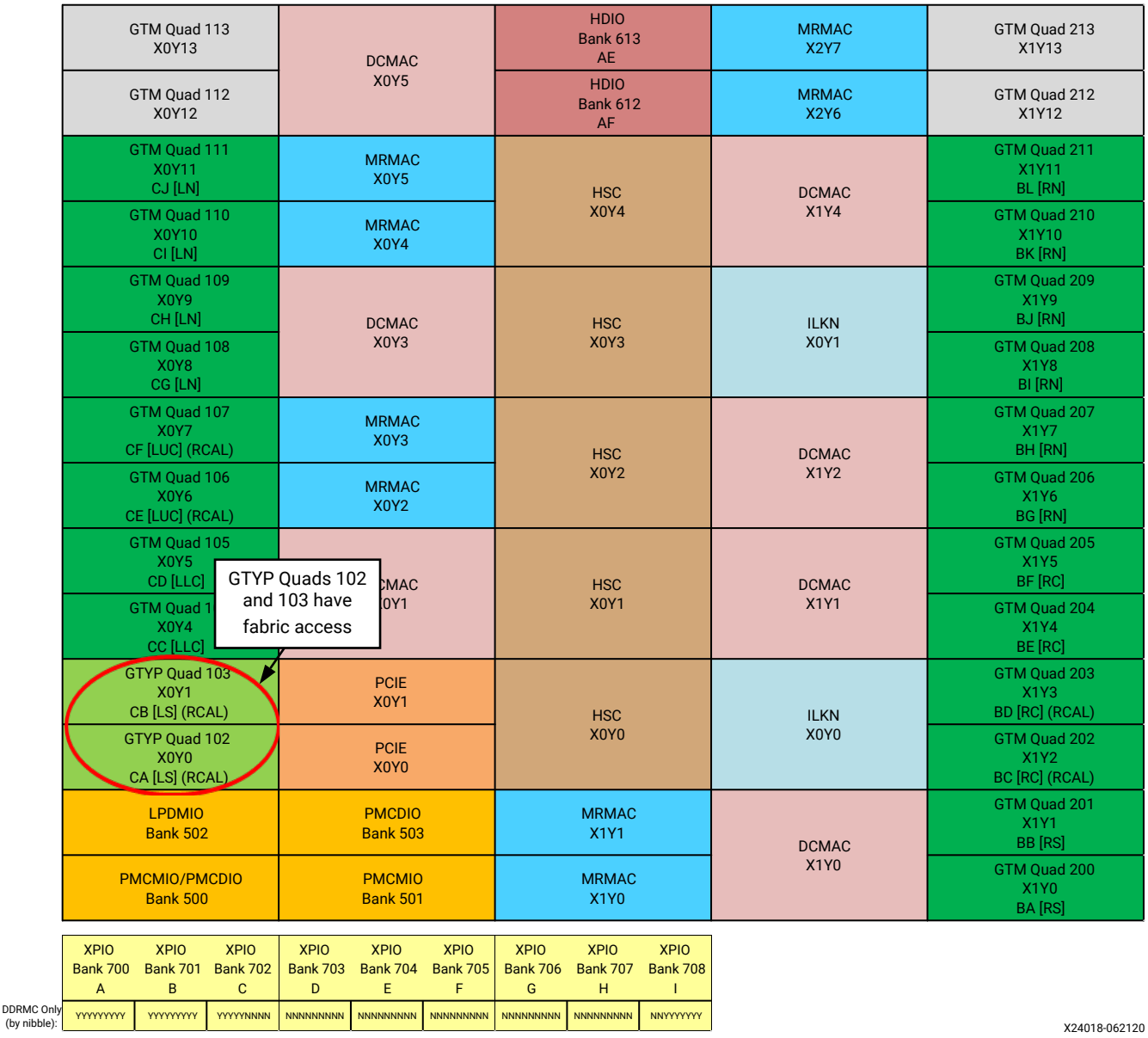
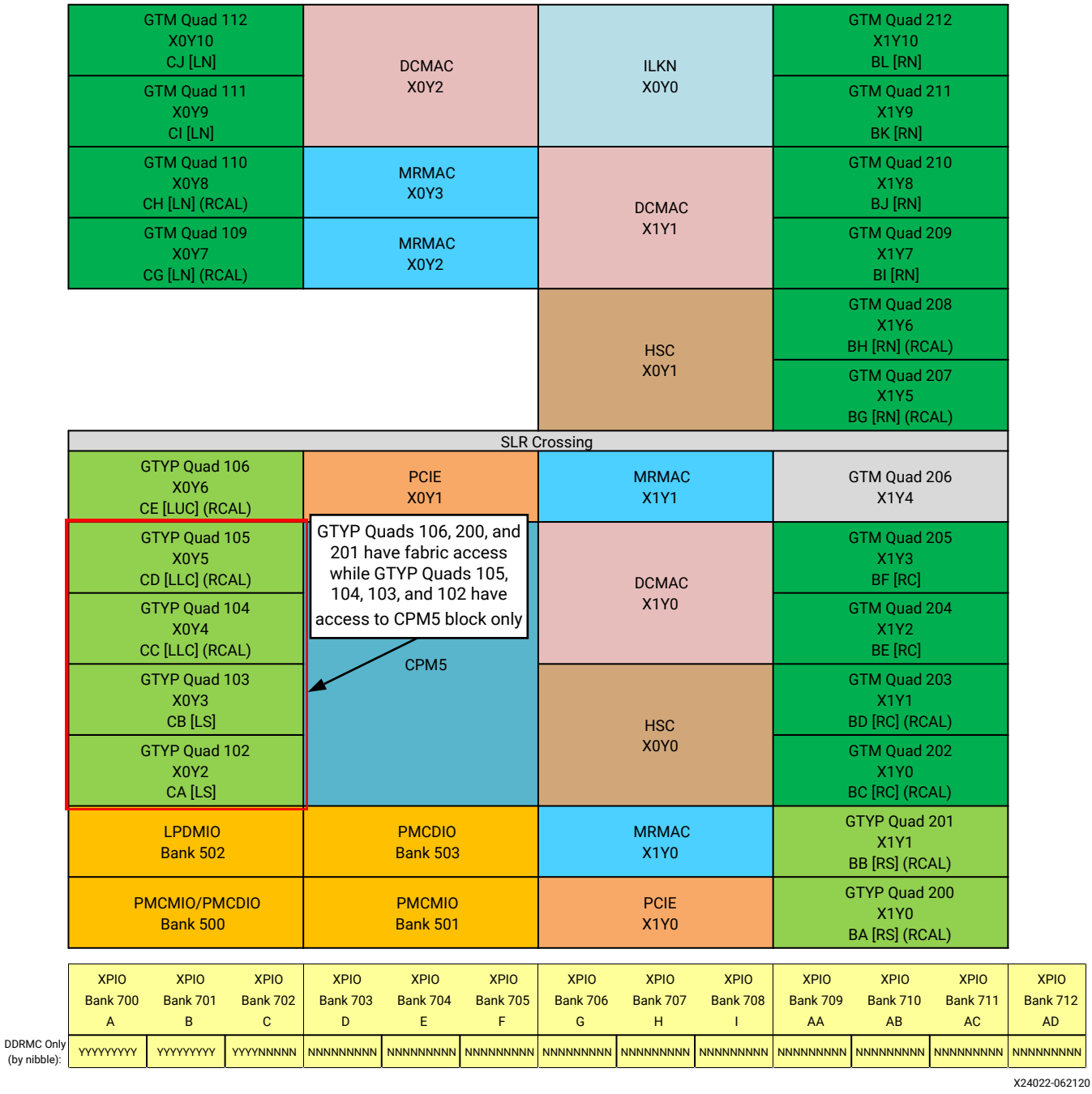


Figure 26: **XCVP1502_A2785 Floorplan**



I/O Bank and GT Quad Number Differences

Certain Versal devices that are footprint compatible in a package might have different I/O bank and transceiver Quad numbers associated with the same package pins. Depending on where these banks are physically located on the die, certain multi-bank interfaces (such as memory or transceiver) could be impacted with regard to migration from one device to another.

Refer to the I/O Bank Migration and Transceiver Quad Migration tables in *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013) for the bank and transceiver Quad numbering differences. To determine bank locations on a die, refer to the Die Level Bank Numbering Overview section of *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013).

The example below shows a successful migration path despite bank number changes between the two different devices.

Example: Planning Ahead for Bank Number Changes

As shown in the following figure, banks 803, 804, and 805 in XCVM1402_VFVA1760 connect to the same pins as banks 706, 707, and 708 in XCVM2602_VFVA1760 because they share the same alphabetic code (AD, AE, AF) indicating the same pin location.

Figure 27: **Snippet of I/O Migration Table**

Package		Device	A	B	C	D	E	F	G	H	I	J	K	L	AA	AB	AC	AD	AE	AF	AG	AH	AI	AJ	AK	AL	AM	AN	AO	AP	AQ	AR	AS	AT	AU	Unbonded
VFVA1760	A1760	XCVM1302	700	701	702	703									800	801	802	803			307															804, 704, 805, 705
VFVA1760	A1760	XCVM1402	700	701	702	703	704	705							800	801	802	803	804	805	307															
VFVA1760	A1760	XCVM2602	700	701	702	703	704	705										706	707	708	609															608

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The following figures show the die/package floorplans that confirm the multi-bank interface remains intact despite the differing locations on each die. All three banks remain part of the same triplet on each respective die. This would result in a successful migration for interfaces that use these three banks, with pin flight times being the only potential difference.

Figure 28: **VM1402_A1760 Floorplan**

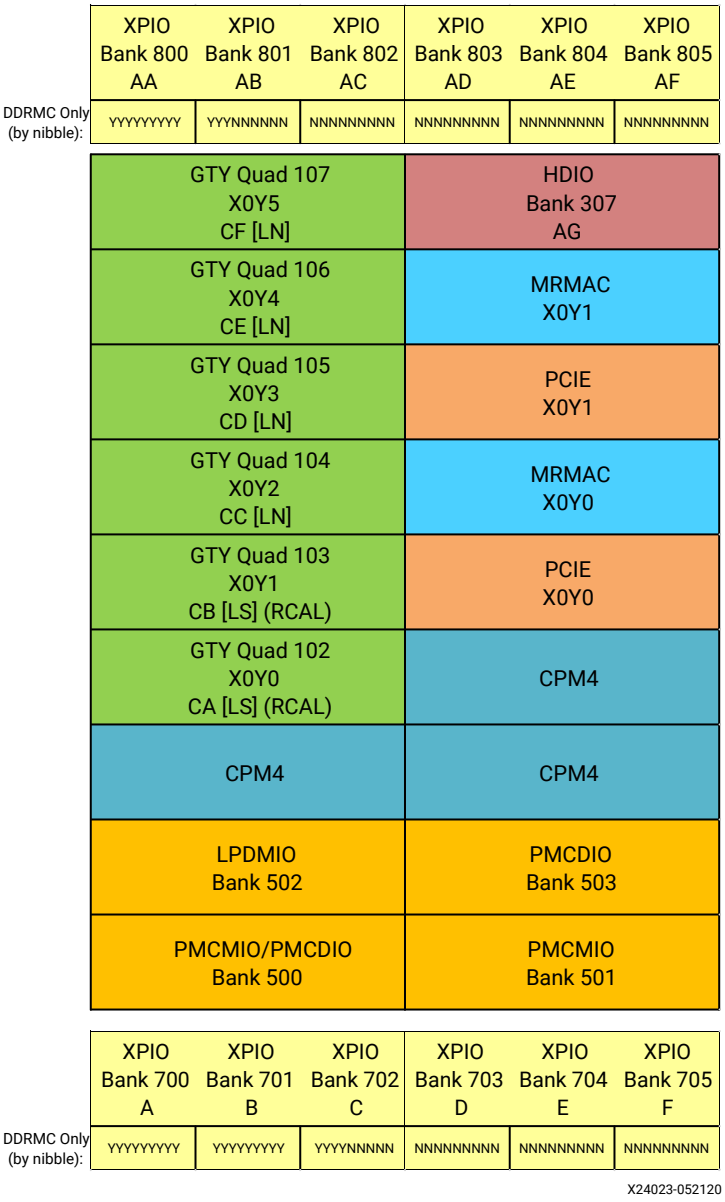
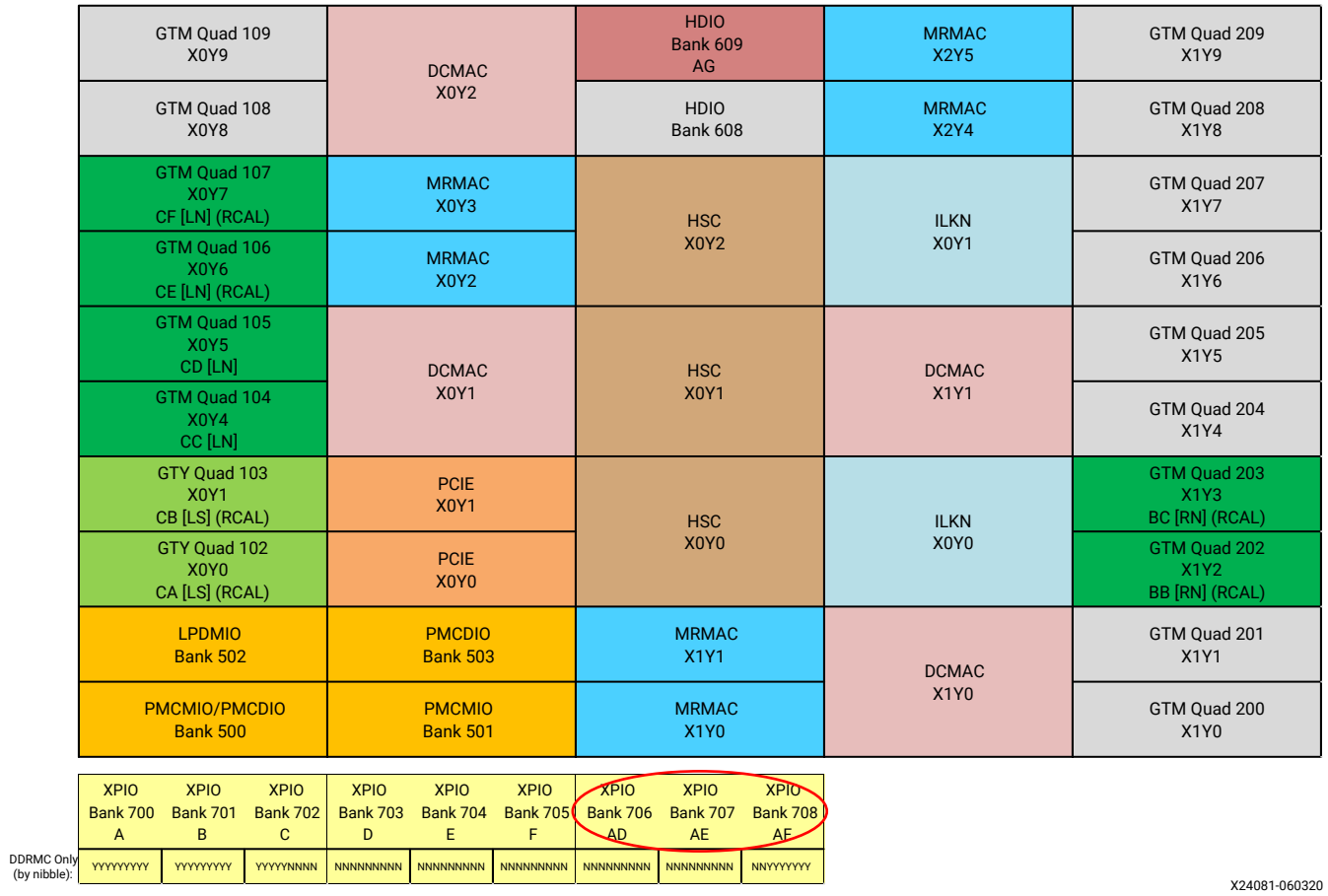


Figure 29: **VM2602_A1760 Floorplan**



VCC_IO and IO_VR Pin Differences

Some XPIO banks in certain die/package combinations are located on the north (top) side of the device in addition to the south (bottom) side of the device. This results in additional VCC_IO_N and IO_VR_800 pins which might not be present on die/package combinations that have all the XPIO banks on the south (bottom) of the device. These extra pins should be tied to the VCC_IO_S and IO_VR_700 pins on the PCB to facilitate migration.

Examples

- XCVM1402 and XCVM1502 in the VSVA1760 package (refer to the floorplans shown earlier)
- XCVP1402 and XCVP1502 in the VSVA2785 package

GT_RCAL and GT_RREF Differences

PCB designers must account for additional GT_RCAL and GT_REF pins when migrating from a monolithic device to an SSI technology device in a given package.

Example

XCVP1402 and XCVP1502 in the VSVA2785 package.

***Note*:** The VP1402 is a monolithic device while the VP1502 is an SSI technology device with two SLRs.

Decoupling Capacitors Guidelines

If the design is not expected to change when migrating to the new device, the same decoupling scheme can be used. If adding logic, Xilinx recommends using a decoupling scheme appropriate to the new device and design. Refer to Xilinx Power Estimator (XPE) for arriving at the decoupling capacitor guidelines using the new device and design.

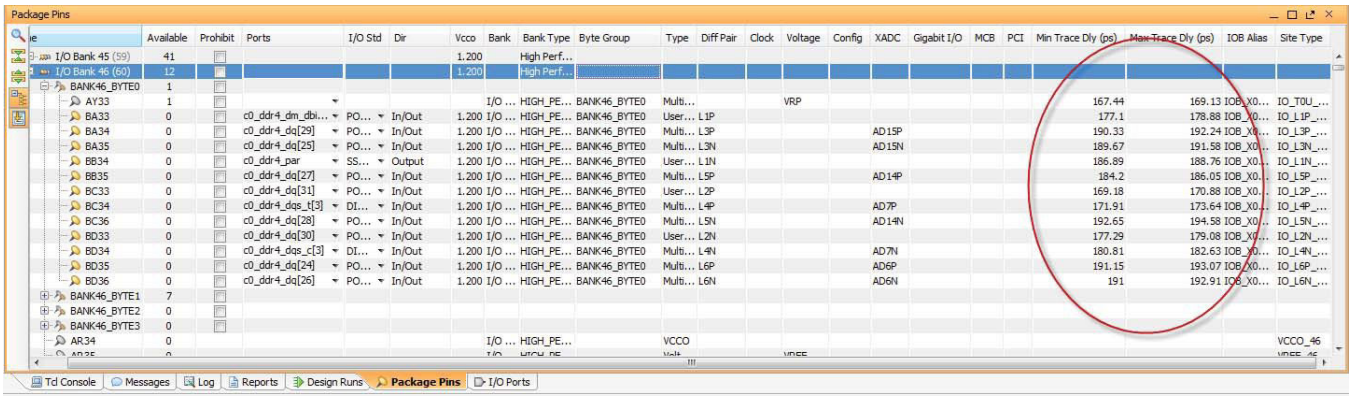
Package Flight Time Differences

Even if two devices across a given package are footprint compatible from a design and PCB standpoint, package flight times will be different across different devices. This difference in package flight time should be accounted for to minimize the overall skew. Flight time information can be found within the Vivado® tools in the Package Pins tab during the I/O planning stage or after synthesis. The ideal strategy to account for pin flight time differences is to deskew the printed circuit board when migrating to the new device. If this is not possible, it is recommended to lay out the printed circuit board with the final device in mind to maximize system performance for the long term. System performance might have to be derated when using the initial device in certain scenarios. As a last option, choosing the mid-point of the range of flight times and routing the board based on that value can act as a compromise, though maximum system performance might not be achievable with this method in certain scenarios.

Example

Pin flight time information can be obtained from the Package Pins tab within the Vivado tools, both in the I/O planning stage and after synthesis.

Figure 30: **Vivado Example Showing Pin Flight Times**



XILINX

Appendix A

Default Capacitor Quantities for Versal Devices

The current methodology for determining Versal decoupling capacitor quantities has been integrated into the Xilinx Power estimator (XPE) tool. The XPE tool allows users to enter the specific utilization parameters for their designs to obtain power estimations and to receive custom decoupling quantity recommendations.

For reference, the decoupling tables presented below can be used as a reference in order to estimate decoupling quantities when the XPE spreadsheet parameters are not yet known. The estimated device utilization is roughly 80% of resources, including the low power (LP) processing system, full power (FP) processing system, GTY blocks, and SelectIOs. Current step loads are assumed at 25% of dynamic current, and AC voltage ripple is assumed to be at the data sheet tolerance minus 1% for DC regulation tolerance. Refer to XPE for the definitions of all the power management scenarios as well as specifications for voltage levels, tolerances, rail groups, and sequencing requirements.

Minimum Rails, Low Voltage

Table 28: **Recommended Decoupling for Minimum Rails, Low Voltage Scenario**

AI Core Device	VCCINT, VCC_PSFP, VCC_PSLP					VCC_RAM, VCC_SOC, VCC_IO, VCC_PMC					VCCAUX, VCCAUX_PMC, VCCAUX_SMON (filtered)		VCCO[1]	
	330 µF	100 µF	47 µF	10 µF	1.0 µF	330 µF	100 µF	47 µF	10 µF	1.0 µF	47 µF	10 µF	47 µF	10 µF
All Devices	3	7	19	29	33	1	2	4	5	0	1	1	1	1

Notes:

1. Per bank. For banks that are combined together, one 47 µF can be used for up to four banks.
2. GTY/GTYP transceiver rails are covered in *Versal ACAP GTY Transceivers Architecture Manual* (AM002).

Minimum Rails, Low Voltage, PS Overdrive

Table 29: **Recommended Decoupling for Minimum Rails, Low Voltage, PS Overdrive Scenario**

AI Core Device	VCCINT					VCC_RAM, VCC_SOC, VCC_IO, VCC_PMC					VCCAUX, VCCAUX_PMC, VCC_SMON (filtered)		VCCO[1]	
	330 µF	100 µF	47 µF	10 µF	1.0 µF	330 µF	100 µF	47 µF	10 µF	1.0 µF	47 µF	10 µF	47 µF	10 µF
All Devices	3	7	19	29	33	1	2	4	5	0	1	1	1	1

Notes:

1. Per bank. For banks that are combined together, one 47 µF can be used for up to four banks.
2. GTY/GTYP rails are covered in *Versal ACAP GTY Transceivers Architecture Manual* (AM002).

Table 30: **Recommended Decoupling for Minimum Rails, Low Voltage, PS Overdrive Scenario**

AI Core Device	VCC_PSLP, VCC_PSFP	
	47 µF	10 µF
All Devices	1	2

Minimum Rails, Mid/High Voltage

Table 31: **Recommended Decoupling for Minimum Rails, Mid-/High-Voltage Scenario**

AI Core Device	VCCINT, VCC_RAM, VCCI_IO, VCC_SOC, VCC_PSFP, VCC_PSLP, VCC_PMC					VCCAUX, VCCAUX_PMC, VCCAUX_SMON (filtered)		VCCO[1]	
	330 µF	100 µF	47 µF	10 µF	1.0 µF	47 µF	10 µF	47 µF	10 µF
All Devices	3	8	27	29	32	1	1	1	1

Notes:

1. Per bank. For banks that are combined together, one 47 µF can be used for up to four banks.
2. GTY/GTYP rails are covered in *Versal ACAP GTY Transceivers Architecture Manual* (AM002).

Full Power Management, Low Voltage, and Low Voltage PS Overdrive

Table 32: **Recommended Decoupling for Full Power Management, Low Voltage, and Low Voltage PS Overdrive Scenarios**

AI Core Device	VCCINT					VCC_SOC, VCC_IO					VCC_RAM		VCCO[1]	
	330 µF	100 µF	47 µF	10 µF	1.0 µF	330 µF	100 µF	47 µF	10 µF	1.0 µF	47 µF	10 µF	47 µF	10 µF
All Devices	3	7	19	29	33	1	2	4	5	0	1	1	1	1

Notes:

1. Per bank. For banks that are combined together, one 47 µF can be used for up to four banks.
2. GTY/GTYP rails are covered in *Versal ACAP GTY Transceivers Architecture Manual* (AM002).

Table 33: **Recommended Decoupling for Full Power Management, Low Voltage, and Low Voltage PS Overdrive Scenario**

AI Core Device	VCC_PMC		VCCAUX		VCCAUX_PMC, VCCAUX_SMON (filtered)	
	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
All Devices	1	1	1	1	1	1

Table 34: **Recommended Decoupling for Full Power Management, Low Voltage, and Low Voltage PS Overdrive Scenario**

AI Core Device	VCC_PSFP (0.70V)		VCC_PSLP (0.70V)		VCC_PSFP (0.88V)		VCC_PSLP (0.88V)	
	47 µF	10 µF	47 µF	47 µF	10 µF	10 µF	47 µF	10 µF
All Devices	1	2	1	1	1	2	1	1

Full Power Management, Mid/High Voltage

Table 35: **Recommended Decoupling for Full Power Management, Mid-/High-Voltage Scenarios**

AI Core Device	VCCINT, VCC_RAM					VCC_SOC, VCC_IO					VCCO[1]	
	330 µF	100 µF	47 µF	10 µF	1.0 µF	330 µF	100 µF	47 µF	10 µF	1.0 µF	47 µF	10 µF
All Devices	3	9	25	46	28	1	2	4	5	0	1	1

Notes:

1. Per bank. For banks that are combined together, one 47 µF can be used for up to four banks.
2. GTY/GTYP rails are covered in *Versal ACAP GTY Transceivers Architecture Manual* (AM002).

Table 36: **Recommended Decoupling for Full Power Management, Mid-/High-Voltage Scenarios**

AI Core Device	VCC_PMC		VCCAUX		VCCAUX_PMC, VCCAUX_SMON (filtered)	
	47 µF	10 µF	47 µF	10 µF	47 µF	10 µF
All Devices	1	1	1	1	1	1

Table 37: **Recommended Decoupling for Full Power Management, Mid-/High-Voltage Scenarios**

AI Core Device	VCC_PSFP 0.80V		VCC_PSLP 0.80V		VCC_PSFP 0.88V		VCC_PSLP 0.88V	
	47 µF	10 µF	47 µF	47 µF	10 µF	10 µF	47 µF	10 µF
All Devices	1	2	1	1	1	2	1	1

Capacitor Specifications

The following table shows a list of recommended capacitors for the various power management scenarios and their placement rules. Other capacitors can be used, but simulation would be recommended to ensure similar frequency and transient response.

Table 38: **Recommended Capacitors**

Capacitance (µF)	Case	Temp	Manf	Manf_P/N	Placement Rules
330	1210	X6S	Murata	GRM32EC80E337ME05L	Within 1–1.5" of BGA edge

Table 38: **Recommended Capacitors** *(cont'd)*

Capacitance (µF)	Case	Temp	Manf	Manf_P/N	Placement Rules
100	0805	X6S	Murata	GRM21BC80G107ME15L	Within 1–1.5" of BGA edge
47	0603	X6S	Murata	GRM188C80E476ME05D	Within 1" of BGA edge
10	0402	X6S	Murata	GRM155C80E106ME44	Within 1" of BGA edge
1.0	0201	X6S	Murata	GRM033C80J105ME05	Under BGA between power/gnd vias

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Appendix B

Additional Resources and Legal Notices

Xilinx Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Xilinx Support.

Documentation Navigator and Design Hubs

Xilinx® Documentation Navigator (DocNav) provides access to Xilinx documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the Vivado® IDE, select **Help → Documentation and Tutorials**.
- On Windows, select **Start → All Programs → Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

Xilinx Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- On the Xilinx website, see the Design Hubs page.

Note: For more information on DocNav, see the Documentation Navigator page on the Xilinx website.

References

These documents provide supplemental material useful with this guide:

1. Versal ACAP data sheets:
   - *Versal Architecture and Product Data Sheet: Overview* (DS950)
   - *Versal Prime Series Data Sheet: DC and AC Switching Characteristics* (DS956)
   - *Versal AI Core Series Data Sheet: DC and AC Switching Characteristics* (DS957)
2. *Versal ACAP GTY Transceivers Architecture Manual* (AM002)
3. *Versal ACAP Technical Reference Manual* (AM011)
4. *Versal ACAP Packaging and Pinouts Architecture Manual* (AM013)
5. *Vivado Design Suite User Guide: Power Analysis and Optimization* (UG1275)

Please Read: Important Legal Notices

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