White Paper: FPGA

WP164 (v1.0) June 24, 2002

IBM Licenses Embedded FPGA Cores from Xilinx for Use in SoC ASICs

By: Shelly Davis, Senior Product Marketing Manager, Xilinx
Chris Reynolds Senior Engineer, IBM
Paul Zuchowski Senior Engineer, IBM

IBM and Xilinx recently announced a license agreement to develop programmable logic cores for use within the next generation IBM “Cu-08” ASIC product — this is a crucial link in the on-going quest for system-level integration. This collaboration to offer designers high-performance ASIC technology, with state-of-the-art programmable logic, opens a vast potential for new applications and the ultimate in both integration and flexibility. This development expands the growing relationship between these two leading technology companies. Both are ranked #1 in their product markets by Dataquest, where IBM has captured the #1 ASIC supplier ranking for 3 successive years, and Xilinx has similarly held the top FPGA supplier position.

The cores are being jointly developed using IBM's new 90 nm ASIC technology, which both companies share though separate foundry agreements. Three core sizes are plannned, from 10k to 40k gates, with up to 640 I/Os. Multiple cores of can be implemented within a single ASIC device, enabling integration of well over 100k gates of reconfigurable logic. The cores are projected to be available for customers' use in late 2003.

Important Step for the Industry:

Integration vs. Competing Partial Solutions

In the past, ASIC and FPGA technologies have overlapped and in some cases, competed. In the 1980s and early 1990s, FPGA technology was significantly less dense, lower in performance, and more expensive than ASIC technology. Programmable logic's popularity stemmed from its flexibility, especially in applications that required constant change. As process technology progressed through 0.25 µm toward 0.10 µm, FPGAs offered improved densities and price points that enabled them to encompass much of the gate array market and in some instances, compete directly with standard cell ASICs. Until now, designers had two choices: very dense standard cell technology, with its superior performance, integration, and lowest possible production price; or FPGA technology which offered flexibility and system-level features, but at significantly higher prices per gate, and with a larger footprint. Combining these two technologies gives designers the best of both worlds, providing industry-leading density and performance as well as flexibility. This fills the gap, opening new potential for integration and market success.

Important Step in SoC Design:

Sweeping in Additional Card Function and Incorporating Design Updates

Programmable logic has become common in many of today's challenging applications, where designers use FPGAs for portions of their systems that are not fixed — including logic that is likely to change as standards and requirements evolve. For these applications, embedded FPGA cores can provide tremendous competitive advantage by allowing designers to integrate reprogrammable functions directly into ASIC designs. This integration can improve performance by reducing chip boundary crossings, and open up new possibilities for closer interaction between fixed and reconfigurable logic.

As chip complexity increases past 10 million gates, designers are presented with opportunities to integrate logic that previously occupied entire system cards, with associated cost and performance improvements. IBM's Cu-08 product will have improvements of approximately 20% in performance and nearly 2x in density over previous ASIC technologies, enabling designs with up to 72 million gates. Many of tomorrow's applications require standard cell ASIC technology for this superior performance, gate count, and integration of IP. Broadening of IP to include processors, SRAM, DRAM, and now programmable logic continues to open new opportunities for design integration.

Enabling New Classes of Applications

Product Families Using a Single ASIC Design

Adding programmable logic to an ASIC device also creates opportunity for dramatic cost and time-to-market savings in many applications. In product lines where successive models are produced, the majority of the logic of each product may be similar, but require successive ASIC designs to accommodate new features. Including FPGA cores directly into an ASIC make it possible to incorporate these changes within a single-chip design. Many of today's applications already show the need for this, particularly in office equipment, telecommunications, and consumer electronics.

The benefits are substantial:

- Less inventory tracking — A single chip design vs. several chips to order and stock
- Less NRE expense potential for lower development costs vs. a family of designs (up to $1M NRE per design)
- Dramatic time to market reduction when new features are added (days vs. months)
- Ability to update hardware that is already deployed in the field, without changing boards or devices.

A Better Flow

Methodology Flow and Tools for Embedded FPGA Cores Will Combine the Best of Xilinx and IBM's Proven Expertise

This new offering will use a combination of existing software tools from both companies, which have been developed and thoroughly verified in previous ASIC and FPGA products. This use of proven tools for configuration, timing, layout, checking, and so on will ensure that designers can smoothly integrate their programmable functions into complex chip designs. The marriage of sophisticated design software from the two established leaders in ASIC and FPGA products is a key advantage for customers — ensuring rapid time to market and high confidence for "first-time-right" design.

The design flow will be divided into FPGA macro and full-chip processing. The cores will be synthesized and timed using the existing Xilinx tool suite. The chip integration will use IBM's proven ASIC methodology and tool suite, incorporating models and timing input for the personalized FPGA cores. Existing IBM tools include full-chip timing analysis and design timing closure, design checking, test pattern generation, and chip-level layout. Using both Xilinx and IBM tools in this manner will also enable design updates to be made easily to the programmable logic after fabrication, verifying updated chip timing whenever needed.

Success in This Endeavor Requires Essential Elements

The concept of embedded FPGA cores is not new. Designers have been asking for this capability ever since the inception of SoC design. Companies have tried to create embedded FPGA core offerings in the past, but have not had all the right elements to create a successful solution. One important element is a strong, shared process technology. IBM's strength in fabrication technology has been evident throughout their

progression of leading ASIC and other VLSI products. The current Xilinx Virtex™-II series uses 0.13 µm process technology shared with IBM, and is now the most successful product in the history of the company. Xilinx also has current design experience with IBM's 90 nm technology. This serves as a strong base for embedded FPGA core design, minimizing process-related issues and improving the ability to close design verification quickly.

Another key element is a robust design environment. IBM's strength in design tools and methodology is well known, and has been a cornerstone in its reputation for "first-time-right" silicon. This same environment enables efficient, high-confidence FPGA block integration, timing, checking, and testing.

A final element for success is a well-defined and easily implemented FPGA interface. Xilinx tools are easy to use, inexpensive, and are well known to logic designers.

Conclusion

Combining ASIC With Programmable Logic Will Change the Industry

This breakthrough will eliminate some of the most common drawbacks of both ASIC and FPGA design. It will also open up new design possibilities for complex ASICs, adding the flexibility to adapt to changing design requirements. Designers in many product sectors, who balance integration and complexity vs. quick time to market, can use these products to speed their system development. In markets where standards are changing, such as in telecommunications, use of FPGA technology on an ASIC can take care of last minute changes or can quickly accommodate variations for specific geographical markets. For producers of multiple product models, such as printers, fax machines, or GPS systems, the combination of ASIC and FPGA technology on a single chip can mean a shortened design cycle and fewer ASIC designs.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
06/24/02	1.0	Initial Xilinx release.