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CoolRunner-II Chip Scale Package Details

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The CoolRunner™-II CPLD family provides two unique CSP (Chip Scale Package options). Xilinx nomenclature defines two types of CSP. They are:

CS — which refers to a 0.8mm ball spacing

CP — which refers to a 0.5mm ball spacing.

These packages offer small size and high logic density for both high performance and low power applications. The two CSP discussed in this white paper are the CP56 and CP132 packages. Due to their small ball spacing and associated layout issues, there are certain topics such as solder mask openings and escape routing concerns which are discussed in this white paper.

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CSP Benefits

Portable and High-Speed Benefits

It is obvious that small packages are beneficial to portable and handheld electronic devices due to form factor constraints. But CoolRunner-II CPLDs can also benefit portable applications in other ways. They are one of the few reprogrammable logic devices that can offer low heat dissipation which lends to higher reliability.

CSP are also attractive to high-speed applications due to the expensive nature of multiple layer, high-speed digital PCBs (Printed Circuit Boards). Chip Scale CPLD packages provide cost reduced solutions by consuming less real estate for any application. Consider the replacement of a 44-pin PLCC package with a 56-ball Chip Scale package. The CP56 solution requires only 11% of the space previously occupied by the PLCC package while providing 45 I/O vs. 33 I/O. If a CP132 and TQ144 are compared, the result is 106 I/O vs. 118 I/O — that's only 12 less I/O for a board space savings of 47%. Table 1 describes common chip scale packages and their dimensions.

56-Ball Chip Scale Package

CP56 Basics

The CP56 package is offered in both the 32 (XC2C32) and 64 (XC2C64) macrocell CoolRunner-II CPLD devices and available in 33- and 45-ball I/O counts.

PCB Layout

Due to the ball spacing (0.5mm) the CP56 package requires a minimum of two PCB layers. These layers are needed due to the tight spacing of inner ball escape routing. Due to this limited spacing, only one escape route is permitted between outer ring adjacent solder I/O balls. The optimal CP56 escape routing is shown in Figure 1.

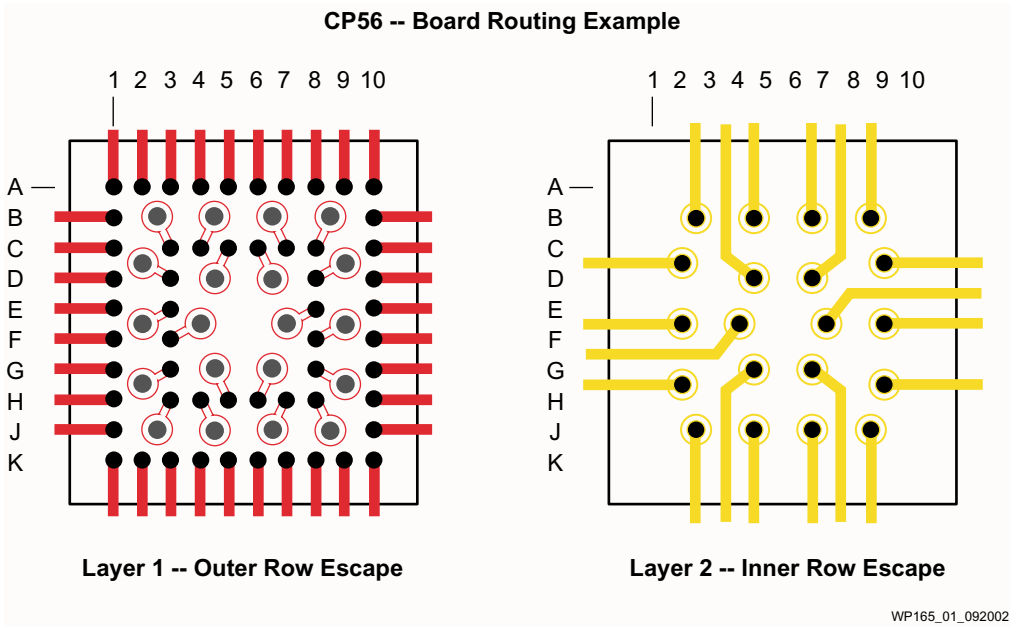

Figure 1: **CP56 PCB Layout**

Critical measurements for the CP56 package are as follows:

- Trace witdh <= 0.127mm
  - Inner row may go to 0.100mm
- Via size is 0.3mm
- Via capture pad is 0.50mm to 0.55mm
- Pad NSMD is 0.27mm

CP56 Device Offering

CoolRunner-II CP56 Device Features

Table 1 shows features for the associated CoolRunner-II CPLD devices in the CP56 package option.

Table 1: **Device Offerings**

Part Number	Max I/O	I/O Banks	I/O Standards	Dual-EDGE	Clock Divider	f_{MAX}
XC2C32-*CP56	33	1	LVTTL 3.3V LVCMOS 1.8-3.3V and 1.5V I/O	No	No	333 MHz
XC2C64-*CP56	45	1	LVTTL3.3V LVCMOS 1.8-3.3V and 1.5V I/O	No	No	333 MHz

Notes:

1. * indicates speed grade.

132-Ball Chip Scale Package

CP132 Basics

The CP132 package is offered in CoolRunner-II 128 (XC2C128) and 256 (XC2C256) macrocell CPLD densities. These two devices are offered in 100- and 106-ball I/O counts.

PCB Layout

Due to the ball spacing (0.5mm) the CP132 package, it requires a minimum of four PCB layers. As shown in Figure 2, there are seperate layers for power, grid (ground), and top and bottom ball layers.

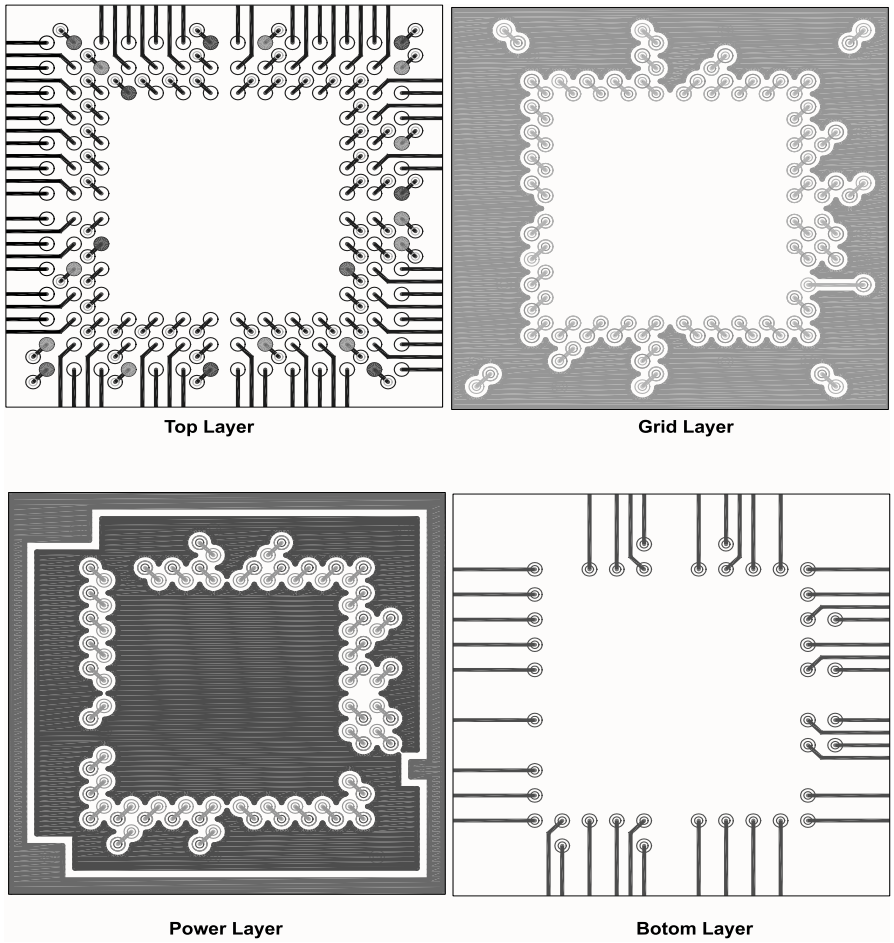

Figure 2: **CP132 PCB Layout**

Critical measurements for the CP132 package are as follows:

- Component Attributes
  - Ball diameter is 0.30mm
  - Pad opening is 0.27mm Solder Mask Defined
- Board Attributes
  - Solder landing diameter is 0.27mm NSMD
  - Via diameter is 0.15mm on 0.27mm diameter via landing
  - Top layer signal trace width is 0.075mm
  - Bottom layer signal trace width is 0.075mm

CoolRunner-II CP132 Device Features

Table 2 shows features for the associated CoolRunner-II CPLD devices in the CP132 package option.

Table 2: **CP132 Device Offerings**

Part Number	Max I/O	I/O Banks	I/O Standards	Dual-EDGE	Clock Divider	f_{MAX}
XC2C128-*CP132	100	2	LVTTL 3.3V LVCMOS 1.8-3.3V and 1.5V I/O	Yes	Yes	263 MHz
XC2C256-*CP132	106	2	LVTTL3.3V LVCMOS 1.8-3.3V and 1.5V I/O	Yes	Yes	263 MHz

Notes:
1. * indicates speed grade

Types of Landing Pads

Pad Layout

Other information necessary to design with CP type packages is regarding pad types on the component and PC board. Two definitions are covered including Non Solder Mask Defined (NSMD) and Solder Mask Defined Pad (SMD). In theory, thermal mismatch between the mounted device and PCB creates loading in solder joints as the device is under operation. This operation leaves stress in the joint which could cause fatigue. Thus, using solder screens of proper thickness will ensure that solder joints have proper bonding to the PCB material. NSMD offers greater area for the solder to bond creating a stronger electrical and mechanical contact.

NSMD

With NSMD, the solder mask opening is seperated from the pad metal allowing a clearance of bare PCB substrate material. Figure 3 shows this type of opening.

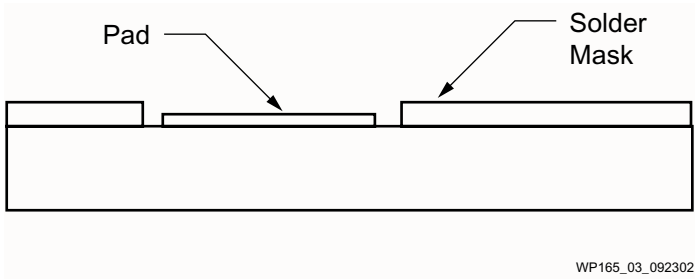

Figure 3: **NSDM Solder Mask Opening**

Topology of the connection method also differs between NSMD and SMD. Figure 4 shows the topology and via connection method for NSMD. As shown, the NSMD differs from the typical SMD dumbell construction.

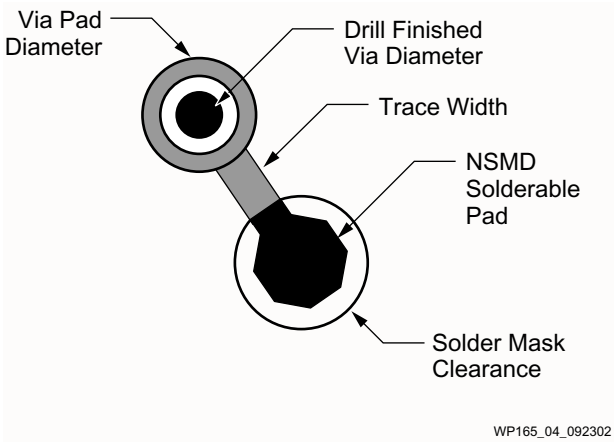

Figure 4: **NSMD Via and Pad**

SMD

With SMD, the solder mask opening overlaps the metal pads. The shape of exposed metal is defined by the mask. Figure 5 shows this type of opening. Due to the bonding properties of SMD, there is greater chance of solder shorts. This is due to the solder ball becoming larger than the intended joint due to the landing pad and solder mask layout.

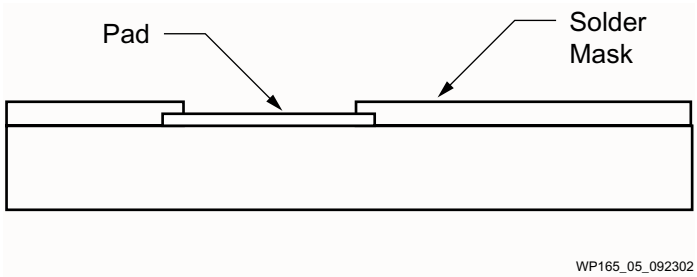

Figure 5: **SMD Solder Mask Opening**

Again the topology of the connection method is different between NSMD and SMD. Figure 6 shows the topology and via connection method for SMD. These types of pads lead to a higher occurance of solder shorts.

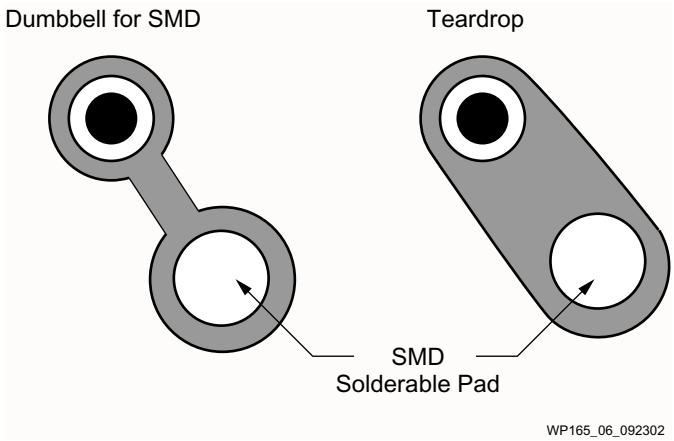

Figure 6: **SMD Via and Pad**

In Table 3, a summary of attributes and concerns between SMD and NSMD package options is offered for reference.

Table 3: **NSMD and SMD Tradeoffs**

Type	Attributes	Concerns
SMD	Use of teardrop is possible, leading to better adhesion, better mechanical strength of pad to base, good stringer connection. Good for boards subject to more flexing. Better heat resistance, can handle multiple reflow/rework with less damage. Mount height for the same pad metal size is generally higher for SMD pad. NSMD pads are generally made slightly smaller for this consideration to achieve the same height with the same solder volume.	Soldermask "bite" into solder is considered as a preflaw and potentially serve as stress concentration point. Due to larger initial pad size requirement, this is believed to encroach on available space for routing. Mask definition and thus tolerances for these solderable openings are considered poor.
NSMD	Copper/metal dimensions are typically better controlled than soldermask. Above point leads to better hot air solder leveled surfaces – better uniformity and yields. Stress concentration issue perceived in the SMD case does not apply here. Well established and more usage.	Adhesion can be an issue in small pads subject to certain extreme bending conditions. The size and number of the traces joining the pad should be controlled. Multiple trace connection to a pad should be discouraged to avoid the pad become a pseudo SMD on the trace joining side.

NSMD pad is becoming the de-facto standard for the BGA PCB business. Unless mounting on thinner boards that may be subjected to bending, use of NSMD is generally recommended

Conclusion

Xilinx packaging leadership addresses the industry demand for reduction in both system costs and size. Xilinx offers 0.5-mm pitch CSP BGA packages that dramatically reduce board real estate and increase I/O counts for CoolRunner-II CPLDs.

Designed with proven mainstream manufacturing flows optimized to handle these low-pitch packages, Xilinx CoolRunner-II CPLD CSPs provide the following advantages for customers:

- Meeting the JEDEC Level-3 Moisture Resistance specification
  - Enabling customers to maintain standard manufacturing flow/cycle time
- Lower thermal resistance translating to better thermal performance
  - Eliminating cost for additional board-level cooling components (reduce power supply requirements and external cooling fans or ventilation)
- Better board-level reliability
  - Providing higher system reliability and reduced cost for required rework
- Pin-out compatibility across the CoolRunner-II family
  - Enabling customers to use the lowest cost package/device combination once the design is finalized
- Better routability
  - Allowing customers to reduce overall system cost by reducing the number of layers needed per board and using standard board manufacturing technology

Combining these leading-edge CSP packaging advantages with the high-performance and low power operation of the Xilinx CoolRunner-II CPLD produces the ideal solution for reliable designs in next-generation, high-performance systems.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/24/02	1.0	Initial Xilinx release.