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Programmable Logic Solutions for Next Generation Serial Backplanes

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For years, bandwidth performance improvements in telecom, datacom, and computing systems backplanes were accomplished by widening buses and increasing signal clock rates. This was sufficient until recently, and now data rates exceeding 622 Mbps and reaching 1 to 3.125 Gbps range, across 20 inches or more of backplane trace, have made it challenging to pass data reliably over parallel buses. As a result, characteristics such as signal skew and loading, which were non-issues before, are suddenly problematic. Consequently, designers are forced to shift from parallel buses to more advanced serial interconnects.

However, even serial technologies have limitations, especially at data rates beyond the one Gbps level, where new problems arise. Limitations include reflections due to impedance mismatches along the signal path, signal attenuation from backplane materials, and added noise due to crosstalk and Inter Symbol Interference (ISI). Backplane designers need to be aware of these issues and compensate accordingly to ensure that the Bit Error Rate (BER), which is a measure of backplane robustness, is less than 10^{-12}. This challenging task becomes even more critical as system throughput requirements approach 40 Gbps and beyond.

Fortunately, backplane designers can reduce the effects of the signal degradation phenomena by several means, such as:

- using better backplane material (e.g., FR-4, Rogers)
- using better connector types
- improving layout trace to reduce the number of PCB layers and reduce crosstalk
- implementing different signaling schemes
- using signal conditioning techniques

In addition, you can improve the signal integrity of a multi-gigabit serial link by selecting the appropriate SerDes device, which consists of a transmitter, receiver, clock/data recovery (CDR), SerDes, integrated termination resistors, programmable output swing, and transmit pre-emphasis.

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Standards for Serial Backplanes

The large investment required to develop your own proprietary serial backplane subsystem has led to the organization of consortia, such as the PCI Industrial Computer Manufacturers Group (PICMG), who develop specifications for standardized backplane architectures. PICMG is a consortium of over 600 companies who collaboratively develop open specifications for high performance telecommunications and industrial computing backplane applications. PICMG participants include vendors of telecommunications equipment, ICs, boards and systems, chassis, connector, power supplies, software and computer OEMs. PICMG has recently produced a series of specifications called Advanced Telecom Computing Architecture (PICMG 3.X AdvancedTCA™) for next-generation carrier grade telecommunications equipment, with a new form factor and based on switched fabric architectures which include dual star, dual-dual star and mesh topologies. The base specification, PICMG 3.0, was adopted at the end of the 2002 calendar year. Additional specifications in the series include PICMG 3.1 for Ethernet fabric, PICMG 3.2 for Infiniband, PICMG 3.3 for StarFabric Interconnect and PICMG 3.4 for PCI Express™ architecture.

Xilinx Solutions for Serial Backplanes

Xilinx has made significant efforts in making serial technology available in our FPGAs and in developing solutions such as IP cores, reference designs and tools to help our customers "get over the hump" and gain the benefits of serial technology as easily and quickly as possible. More details about the Xilinx serial backplane solutions are described below.

Virtex-II Pro

The Virtex-II Pro FPGA family, introduced in March 2002, is the first family of Xilinx devices to have embedded serial I/O technology. This family of devices consists of ten members with densities up to 125,000 logic cells (13 million system gates). The family includes up to four IBM PowerPC™ processors, up to 24 Rocket I/O™ multi-gigabit transceivers, up to ten megabits of embedded memory, embedded software design tools, and operating system support. Virtex-II Pro devices are delivered on 300 mm wafers employing 130-nanometer copper process technology and 1.2 volts.

The Rocket I/O supports 622 Mbps to 3.125 Gbps per transceiver, allows 75 Gbps aggregate baud rate and can drive signals over 40" over FR4 material at 3.125 Gbps. Virtex-II Pro addresses a number of emerging high-speed serial standards, supporting ten Gigabit Ethernet with XAUI, PCI Express, Serial ATA, and so on. With up to 1200 SelectIO™-Ultra user I/O (single ended and differential), Virtex-II Pro supports 840 Mbps LVDS and high speed single-ended standards such as XSBI and SFI-4. Virtex-II Pro also supports XCITE technology, which helps eliminate external termination resistors.

Aurora

Aurora is a scalable, lightweight, link-layer protocol that you can use to move data across point-to-point serial links at a baud rate of up to 75 Gbps and is available now. It is an open protocol that can be implemented in any silicon device/technology. Aurora provides a transparent interface to upper layers of proprietary or industry standard protocols such as Ethernet or TCP/IP. This allows designers of next generation communication and computing systems to achieve higher connectivity performance while preserving software infrastructure investment.

Mesh Technology on Xilinx

Mesh Technology on Xilinx (MTX) includes hardware and software reference designs and a BERT testing toolkit developed by Xilinx for enabling rapid development of full-mesh, serial backplane systems.

The PICMG 3.0, 2.5G Full Mesh Reference Design (FMR) is a reference board that you can use as a development platform for PICMG 3.x line cards supporting port rates to 2.5 Gbps. The heart of the reference design is the Virtex-II Pro device, which serves as the interface to the full-mesh backplane. The Virtex-II Pro's on-chip RocketIO MGTs allow all FMR cards on a full mesh backplane to have direct, high-speed serial links to each other. The FMR also allows application flexibility by reserving an area of the board for a pluggable "personality module" (PM). You can use the PM to implement any application-specific line card and easily connect to the FMR through the included headers. PICMG 3.0 also specifies card and shelf management functionalities that are also implemented in the FMR. Availability of the reference design is targeted for first quarter 2004.

The Mesh Fabric Reference Design is a fully functional IP reference design that provides a building block for creating Virtex-II Pro-based mesh switch fabric interfaces. You can use the fabric reference design in a single Virtex-II Pro or in several daisy-chained Virtex-II Pro devices, allowing up to 256 RocketIO serial channels. Figure 1 shows the concept of the mesh fabric interface and the daisy-chain scheme.

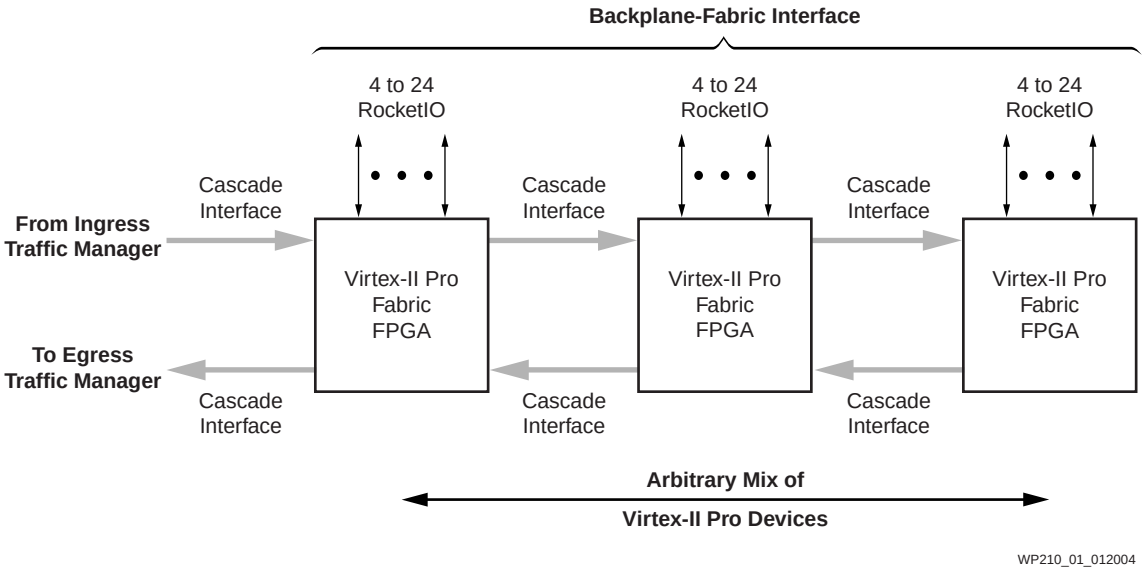

Figure 1: **The mesh fabric reference design can be implemented in a single FPGA or multiple, daisy-chained FPGAs allowing scalability**

By having the flexibility of daisy-chaining devices of different densities, you can choose an appropriate Logic-to-RocketIO ratio. For example, more logic may be useful in a design where additional network processing functions are needed on top of those provided by an ASSP or ASIC. Flexible traffic scheduling is also made possible with the support of up to 16 priority levels and multiple scheduling algorithms on egress. Availability of the reference design is targeted for first quarter 2004.

Figure 2 illustrates an example system with line cards that use the Virtex-II Pro and the full mesh IP as the backplane interface.

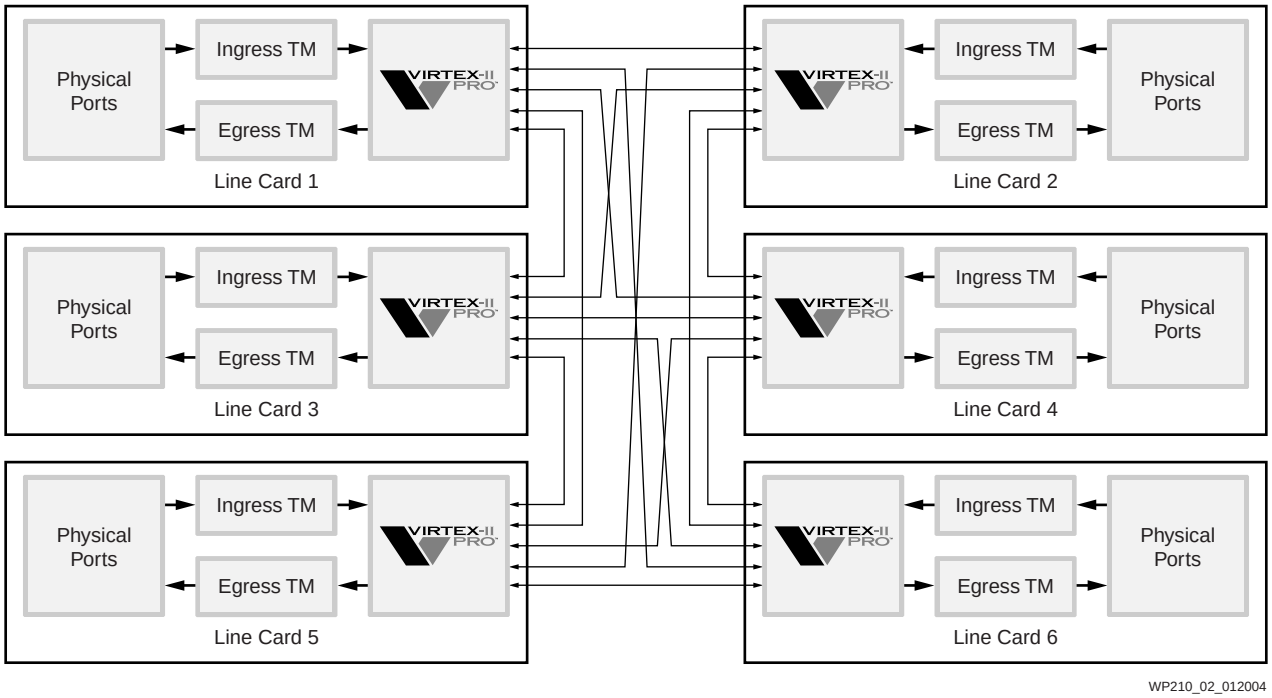

Figure 2: **In a Virtex-II Pro-based full mesh backplane, serial channels and distributed switch functions are implemented using RocketIOs and logic resources using Mesh Fabric IP reference design**

GigaBERT is an IP toolkit that enables easy and comprehensive BERT testing of Virtex-II Pro-based, full mesh fabric channels. Using GigaBERT, you can configure each RocketIO on each FMR connected to a backplane as either a BERT tester or as a far end loopback. In effect, a scheme for simultaneous BERT testing of all links in a full mesh fabric can be accomplished. Furthermore, GigaBERT's flexibility enables you to quickly and easily create a BERT stress test to check for signal integrity in specific configurations. Availability of the toolkit is targeted for first quarter 2004.

Legacy Backplanes Support (Differential and Single-ended I/O)

Xilinx FPGAs are also ideal for customers who still need to support their differential or single-ended legacy bus architectures as they transition to serial architectures. For the highest performance differential solution, you can use the Virtex-II Pro to achieve LVDS rates up to 840 Mbps. For low cost LVDS, Spartan-3 supports up to 622 Mbps. Together these devices provide a complete differential I/O solution with coverage of all the popular standards such as LVDS, Extended LVDS, Bus LVDS, Ultra LVDS, LVPECL, LDT, and RSDS. For legacy designs that use older single-ended signaling standards, the Xilinx SelectIO technology available in Virtex-II Pro and Spartan-3 FPGAs allows the most comprehensive support, including support for LVTTL, LVCMOS, PCI/PCI-X, GTL, HSTL, and SSTL signaling standards. As a result, Virtex-II Pro and Spartan-3 FPGAs provide you with everything you need for supporting legacy backplane interfaces.

Conclusion

In conclusion, designers of high-end telecom, datacom, and computing platforms have looked towards serial I/O technologies to address the continuously increasing performance requirements of next generation systems. Furthermore, to help reduce the difficulty of developing proprietary backplanes, consortia such as the PICMG have stepped up to the plate

and are defining serial backplane standards. Whether it is proprietary or standards based, the Virtex-II Pro FPGA with embedded multi-gigabit serial transceivers provides the technology to enable serial backplanes including advanced, full-mesh architectures. Additionally, our growing portfolio of IP cores, Reference Designs, Toolkits for serial backplanes such as Aurora, Mesh Fabric IP, the PICMG Full Mesh line card, and GigaBERT have lead to shorter time-to-knowledge and ultimately shorter time-to-market. For more details on the Xilinx solution for serial backplanes, go to http://www.xilinx.com/esp/backplanes.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/17/04	1.0	Initial Xilinx release.