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Estimating Actual Output Timing Without Board Simulation

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This document can help designers obtain more accurate I/O timing data without the need for board-level IBIS or SPICE simulations. Until recently, Xilinx specified outputs into a lumped capacitive load. However, since rise and fall times force board interconnect to be considered transmission lines, a lumped capacitive load is no longer relevant (see the **TechXclusives** document on this for more detail). Ideally, designers should simulate the interconnects using SPICE or IBIS with any of the commercial simulators available. This is recommended not only to produce more accurate timing results, but also to ensure that signal integrity issues do not cause functionality problems or long term failures by exceeding the manufacturers' overshoot specifications. This is especially true when interfacing with some of the newer memory technologies that have very fast rise/fall times. Xilinx has worked with Mentor Graphics to supply a reduced functionality version of their board simulation package, HyperLynx, which is free for download **here**. For those who cannot run simulations, the following information makes it easier to approximate clock-to-output timing (Tco).

Using the Table(s) to Calculate Clock-to-Output (Tco) Time

Five things are needed to estimate Tco timing: FPGA clock-to-output timing (Tco), I/O standard, number of loads, configuration of loads, and approximate board trace length. Although the worst case FPGA Tco is available from the data sheet, a more accurate place to get this data is from the software timing tools (Post-Place & Route Static Timing Report in Project Navigator or the `twx/twr` file created using `trce` on the command line). Assuming I/O offset constraints were defined in a constraint file (**`.ucf`** or **`.ncf`** file), the data sheet section of the `twr/twx` should list input setup and hold time and output delay time for all I/O pins. The Tco section should look similar to Table 1:

Table 1: **Clock IO_CLK5 to Pad**

Destination	clk (edge) to PAD	Internal Clock(s)	Clock Phase
SYNC_IN_D[0]	2.156 (R)	clk_50	0.000
SYNC_IN_D[10]	2.093 (R)	clk_50	0.000
SYNC_IN_D[11]	2.103 (R)	clk_50	0.000
SYNC_IN_D[12]	2.111 (R)	clk_50	0.000
SYNC_IN_D[13]	2.114 (R)	clk_50	0.000
SYNC_IN_D[14]	2.134 (R)	clk_50	0.000
SYNC_IN_D[15]	2.136 (R)	clk_50	0.000
SYNC_IN_D[16]	2.076 (R)	clk_50	0.000

Example 1

For the first example, SYNC_IN_D[0] value of 2.156 ns is used. The I/O standard is typically known up front; but if not known, it can be looked up in either the pad file or map report. In this case, it is assumed LVTTL 12 ma slow.

The next thing to determine is the configuration of loads. Although there are an infinite number of ways to configure loads, creating a table for estimating actual clock-to-output timing requires the problem to be bounded. This document covers three possible configurations: point-to-point, star, and daisy chain.

Because the point-to-point configuration can be considered a star or daisy chain configuration with one load, it is not discussed separately and is included with the other two configurations.

Figure 1 is a HyperLynx screen shot showing a two-load star configuration.

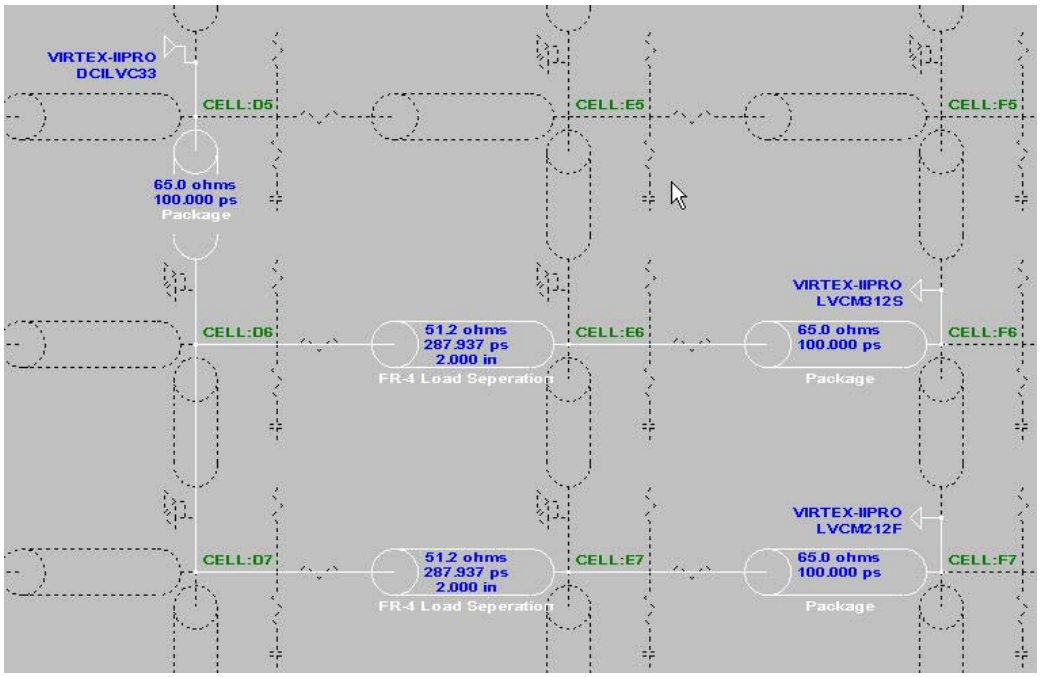

Figure 1: **Two-Load Star Configuration**

The top left of the schematic shows a Virtex-II Pro LVDCI_33 output driving a 65 ohm, 100 ps block representing the package trace. It then branches to two separate 51 ohm, 287 ps blocks representing two inches of board trace. Each of the two traces connects to 65 ohm, 100 ps blocks representing the receiver package traces, and then terminates to Virtex-II Pro LVCMOSS_33 receivers. Since the numbers in both the static timing report and the data sheet take into account the package delay, the 200 ps of package delay would normally have to be subtracted from the actual results.

Making an approximation table for the star configuration is difficult to impossible due to the interaction between the different legs. In the majority of applications where the driver feeds multiple loads on completely separate traces, the traces lengths are not identical. Unfortunately, the length of the other traces can dramatically affect the delay number. For example, in a four-load star configuration with the 6" of trace on the measured leg, the delay adder can vary from 3 ns to 4.6 ns as the length of the other three legs is varied from 2" to 6". Consequently, there are no star configuration tables in this document.

Last but not least is the daisy chain configuration. Figure 2 is an example HyperLynx screen shot of a two-load daisy chain configuration:

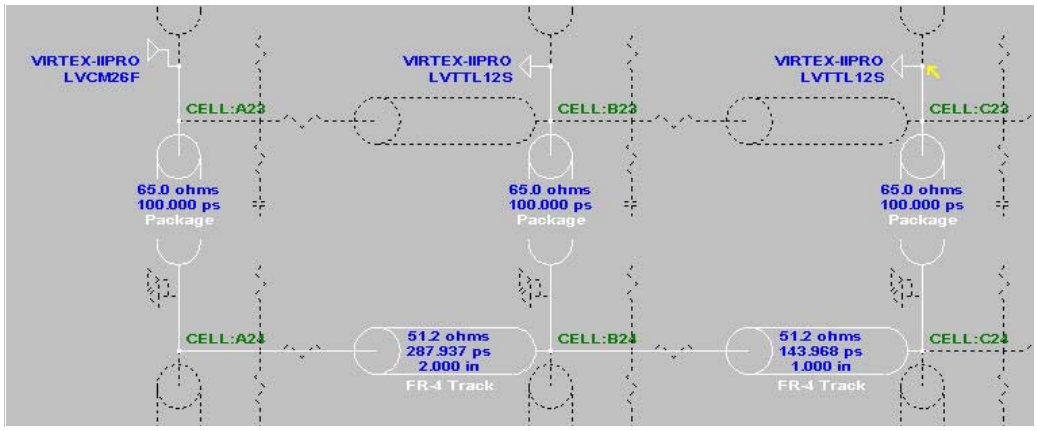

Figure 2: **Two-Load Daisy Chain Configuration**

As shown in Figure 2, all measurements were taken assuming two inches of trace between the source and the first load and one inch of trace between each subsequent load. For this example, a point-to-point configuration is assumed.

The last data required is the approximate board trace length. It is assumed that there are 10 inches of trace between the FPGA and the receiving device. From the Daisy Chain Data Results Table (Table 2), LVTTL 12 ma, slow slew rate, one load, the rising edge number is .61 ns. Since the table only accounts for two inches of board trace, the eight-inch difference needs to be accounted for. The Board Propagation Delay Table (Table 3) can be used to determine that eight additional inches of trace corresponds to roughly 1152 ps of additional delay. Everything adds up to:

Total Delay (Tco) = FPGA Delay + output loading delay + extra board trace delay

= 2.156 ns + 0.61 ns + 1.152 ns

= 3.92 ns

Accounting for output loading delays and board propagation delays added 1.76 ns to the clock-to-output delay. Depending on the circuit's clock frequency and the setup time of the downstream device, this might or might not be significant. The output loading and trace delays were verified in HyperLynx and matched the estimated results.

Example 2

For the second example, a daisy chain configuration, four loads, and a worst-case board trace length of eight inches to the farthest load is assumed. From the Daisy Chain Results Data Table (Table 2), LVTTL 12 ma, slow slew rate, four loads, the rising edge number is 1.66 ns. Since the table accounts for only two inches of trace going to the loads and one inch of trace between each of the four loads for a total of five inches of trace, the three-inch difference needs to be accounted for. The Board Propagation Delay Table (Table 3) can be used to determine that three additional inches of trace correspond to roughly 432 ps of additional delay. Everything adds up to:

Total Delay (Tco) = FPGA Delay + output loading delay + extra board trace delay

= 2.156 ns + 1.66 ns + 0.432 ns

= 4.25 ns

Accounting for output loading delays and board propagation delays added 2.1 ns to the clock-to-output delay. The output loading and trace delay were directly simulated in HyperLynx and came out to 2.11 ns.

Daisy Chain Delay Table

Table 2 was developed using Mentor HyperLynx version 7.1 and the IBIS data available on the Xilinx web page as of July 1, 2004. All simulations were done using the same I/O standard on both the input and output.

Table 2: **Daisy Chain Results Data**

IO Standard Drive Strength	Rise/Fall 1 Load Slow Slew	Rise/Fall 2 Loads Slow Slew	Rise/Fall 4 Loads Slow Slew	Rise/Fall 1 Load Fast Slew	Rise/Fall 2 Loads Fast Slew	Rise/Fall 4 Loads Fast Slew
LVTTL24	0.55/0.54	0.88/0.92	1.49/1.55	0.49/0.49	0.80/0.83	1.43/1.50
LVTTL16	0.55/0.59	0.90/0.97	1.53/1.62	0.51/0.50	0.81/0.87	1.45/1.52
LVTTL12	0.61/0.73	1.01/1.20	1.66/1.93	0.51/0.56	0.87/0.95	1.50/1.62
LVTTL8	0.80/0.95	1.38/1.88	2.36/3.70	0.54/0.66	0.96/1.10	1.62*/1.83*
LVTTL6	0.80/1.50	1.41/2.50	2.33/4.27	0.54/0.90	1.04/1.13	1.79*/1.89*
LVTTL4	1.51/2.01	2.59/3.52	4.16/6.75	0.90/1.98	2.70/2.97	4.14/7.10
LVTTL2	1.54/3.73	2.63/6.79	4.26/12.95	0.89/3.73	2.71/6.93	4.10/13.27
LVCMOS33 24 ma	0.51/0.54	0.82/0.91	1.41/1.53	0.46/0.47	0.76/0.77	1.41/1.42
LVCMOS33 12 ma	0.54/0.69	0.93/1.31	1.58/1.79	0.53/0.54	0.85/0.91	1.50/1.55
LVCMOS33 6 ma	1.00/1.09	1.65/2.12	3.21/3.74	0.37/0.56	0.80/1.18*	1.51*/3.76*
LVCMOS25 24 ma	0.53/0.52	0.88/0.86	1.50/1.48	0.48/0.49	0.77/0.80	1.43/1.44
LVCMOS25 12 ma	0.57/0.62	0.96/1.00	1.59/1.66	0.51/0.51	0.85/0.87	1.50/1.51
LVCMOS25 6 ma	0.81/0.95	1.40/1.68	2.32/3.48	0.54/0.64	0.95/1.05	1.61*/ 1.77*
LVDCI33 Inp. Ref. 1.4	0.56/0.64	0.97 /1.07	1.61*/1.80*			
LVDCI25 Inp Ref 1.25	0.55/0.61	0.95 /1.01	1.62*/1.73*			

Notes:

1. Units are nanoseconds.
2. Stars are bad! Numbers with stars went through the input receiver threshold multiple times (non-monotonic rise/fall time). On a clock line, this would typically cause circuit failures. On a data line in a synchronous system, this is non ideal but could still work if the circuit was designed with an abundance of setup and hold time margin.
3. All Rise/Fall Times are Delta's measured from output of a driver node with no load to the input of the receiver node.
4. It is assumed that the I/O standard applies to both the output and input
5. The receiver input threshold voltage used for measurements were:

   LVTTL = 1.4V
   LVCMOS33 = 1.6V
   LVCMOS25 = 1.25V
   LVDCI33 = 1.4V
   LVDCI25 = 1.25V.
6. For LVDCI33 and LVDCI25, although the numbers were put in the slow slew rate columns, there is no way to set either slew rate or drive strength when using DCI.

Board Propagation Delay Table

The board propagation delay times are shown in Table 3.

Table 3: **Board Propagation Delay Table**

Trace Length (inches)	Delay (ps)
1	144
2	288
3	432
4	576
5	720
6	864
7	1008
8	1152

Notes:
1. The delays are based on the FR4 track stackup shown in Figure 3.

Simulation Reference Information

The FR-4 Track Stackup used for the simulations is shown in Figure 3.

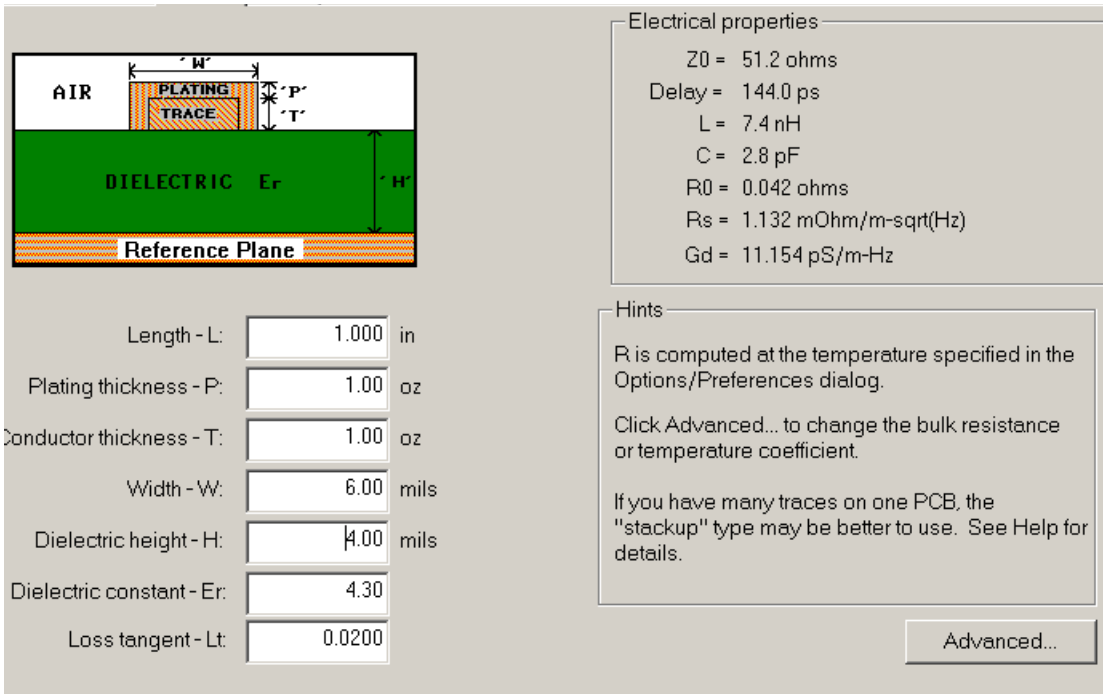

Figure 3: **FR-4 Stackup for Microstrip**

Example Waveforms

In Figure 4, the red trace is the baseline output with no load. The yellow trace is one load, the purple two, and the magenta three. Besides the four-load trace flattening out at around 1V, the waveforms look good.

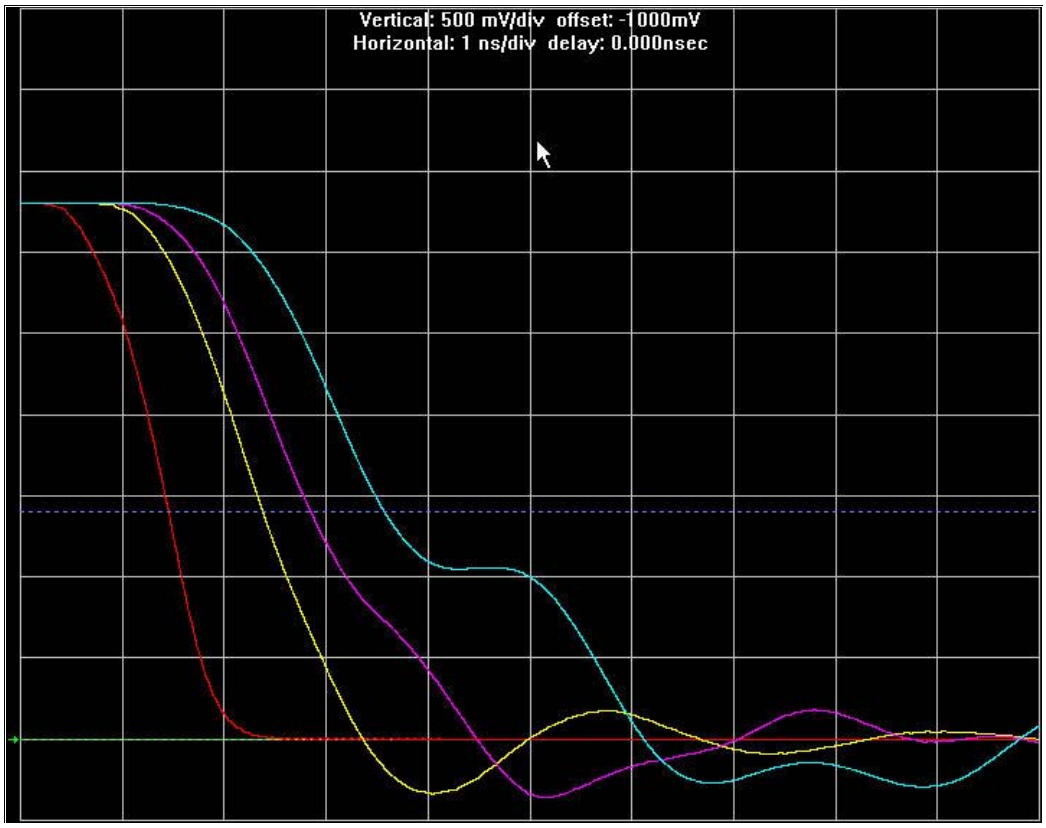

Figure 4: **Daisy Chain Simulation, LVCMOS33 12 ma Slow Slew**

In Figure 5, the two and four load (purple and magenta) traces could fail in normal operation due to the non-monotonic fall time causing the downstream input receiver to trigger twice.

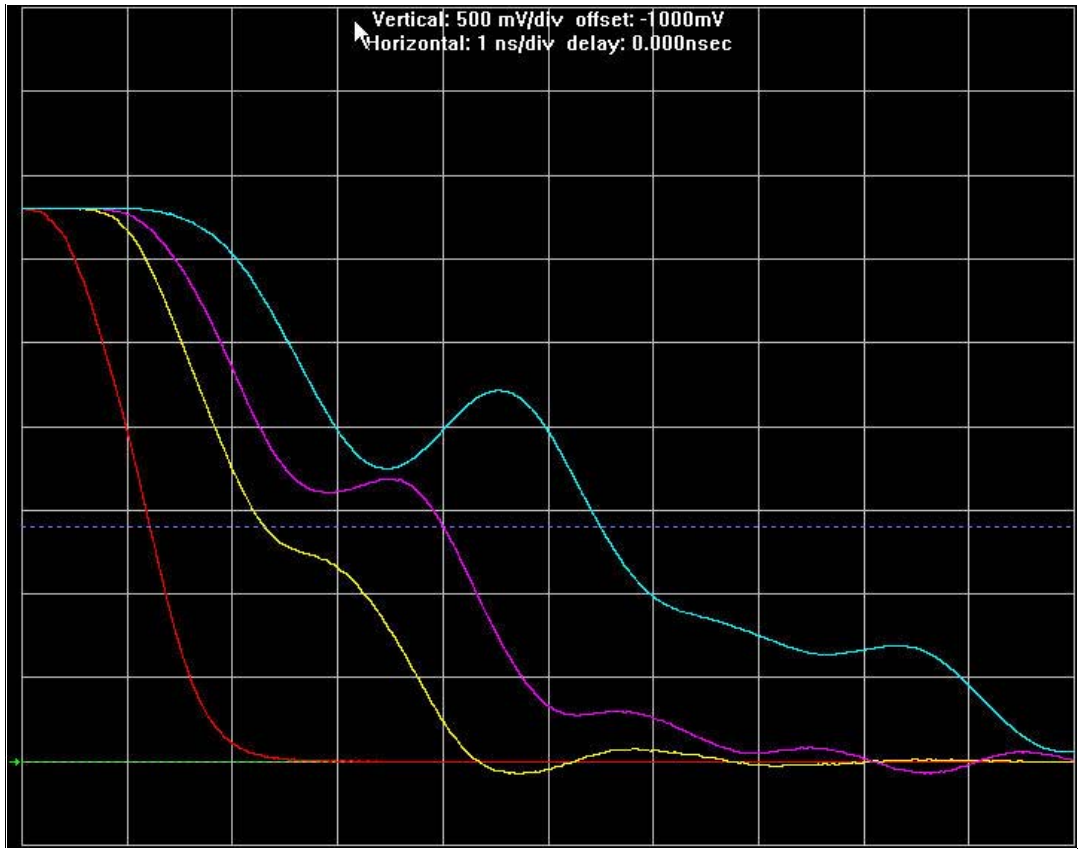

Figure 5: **Daisy Chain Configuration, LVCMOS33 6 ma Fast Slew**

Summary

The use of the table data and techniques described in the examples allow a designer without board simulation tools to more accurately predict FPGA system Tco (clock-to-output) timing. Xilinx still recommends that designers do IBIS or SPICE board-level simulation whenever possible.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
12/23/04	1.0	Initial Xilinx release.