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What are OFFSET Constraints?

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A fundamental timing constraint is the OFFSET constraint. This paper discusses the overall purpose of OFFSET constraints, the specific paths that are covered by OFFSET constraints, and the differences between the OFFSET IN and OFFSET OUT constraints. Additionally, examples of timing reports are included with the common application of the OFFSET IN and OFFSET OUT constraints.

Why Use OFFSET Constraints?

The OFFSET constraint is a fundamental timing constraint. OFFSET constraints are used to define the timing relationship between an external clock pad and its associated data-in or data-out pad. This relationship is also known as constraining the *Pad-to-Setup* or *Clock-to-Out* paths on the device. These constraints are important for specifying timing interfaces with external components.

Pad to Setup or OFFSET IN BEFORE constraint is used to ensure that the external clock and external input data meet the setup time on the internal flip-flop.

Clock-to-Out or OFFSET OUT AFTER constraint is used to control the setup/hold requirement of the downstream devices, as well as the external output data pad and the external clock pad.

The OFFSET IN BEFORE and OFFSET OUT AFTER constraints allows you to specify the internal data delay from the input pads or to the output pads with respect to the clock. Alternatively, the OFFSET IN AFTER and OFFSET OUT BEFORE constraints allows you to specify external data and clock relationship for the timing on the path to

the input pads and to the output pads for the Xilinx device. The timing software determines the internal requirements without requiring a FROM PADS TO FFS or FROM FFS TO PADS constraint. See Figure 1 and Figure 2.

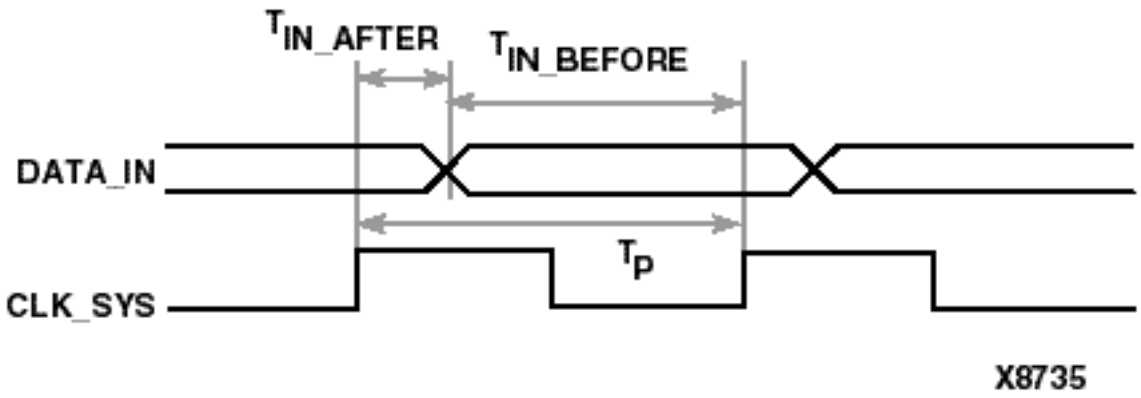


Figure 1: **Timing Reference Diagram of OFFSET IN Constraint**

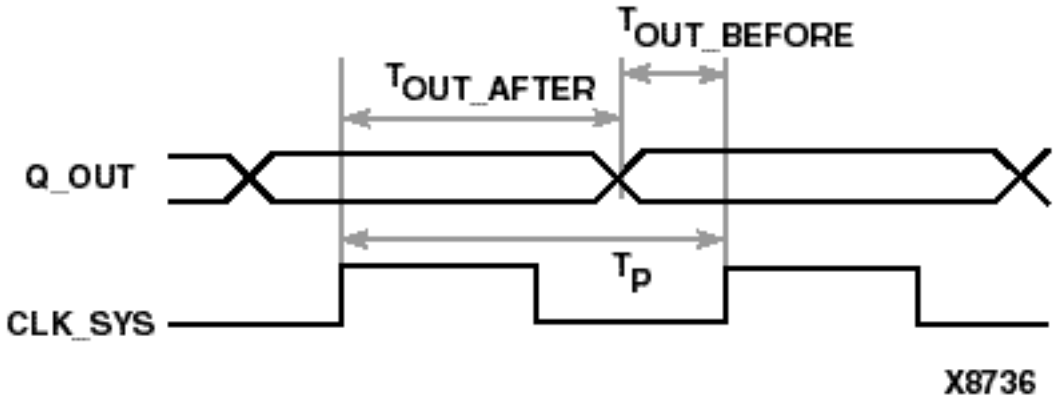


Figure 2: **Timing Reference Diagram of OFFSET OUT Constraint**

You can use these FROM:TO constraint options in the following situations:

- Calculate whether a setup time is violated at a flip-flop whose data and clock inputs are derived from external nets
- Specify the delay of an external output net derived from the Q output of an internal flip-flop that is clocked from an external device pin

The OFFSET constraint provides the following advantages:

- Includes clock path delay in the analysis for each individual synchronous element
- Includes paths for all synchronous element types (FFS, RAMS, LATCHES, and etc.)
- Utilizes a global syntax that allows all inputs or outputs to be constrained with respect to an external clock
- Analyzes setup and hold time violation on inputs

The OFFSET constraint automatically accounts for the following clocking path delays:

- Provides accurate timing information and uses the jitter defined on the associated PERIOD constraint
- Increases the amount of time for input signals to arrive at synchronous elements (clock and data paths are in parallel)
  - Subtracts the clock path delay from the data path delay for inputs
- Reduces the amount of time for output signals to arrive at output pins (clock and data paths are in series)
  - Adds the clock path delay to the data path delay for outputs
- Includes clock phase introduced by a DLL/DCM for each individual synchronous element defined by the associated PERIOD constraint
- Includes clock phase introduced by a rising or falling clock edge

The initial clock edge for analysis of OFFSET constraints is defined by the HIGH/LOW keyword of the PERIOD constraint:

- HIGH keyword => the initial clock edge is rising
- LOW keyword => the initial clock edge is falling

What Paths are Covered by OFFSET Constraints?

The OFFSET constraints cover the following and are shown in Figure 3:

- From input pads to synchronous elements (OFFSET IN)
- From synchronous elements to output pads (OFFSET OUT)

If the clock that clocks a synchronous element does not come through an input pad – for example, it is derived from another clock – then the OFFSET constraint will fail to return any paths during timing analysis.

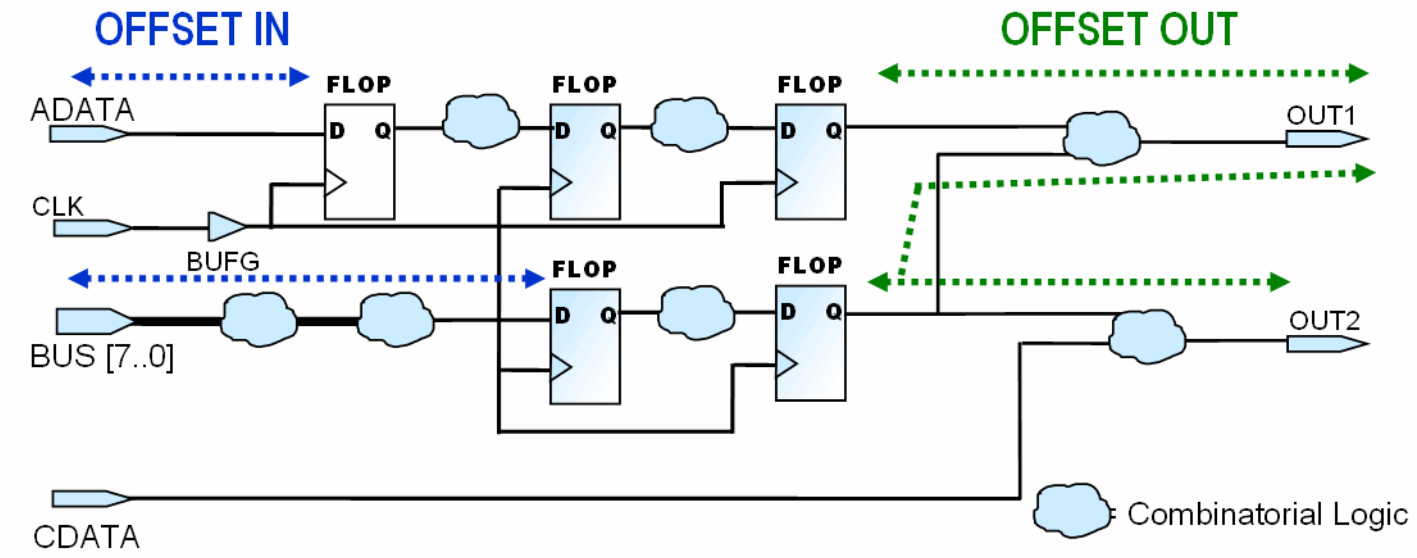


Figure 3: **Circuit Diagram of OFFSET Constraints**

The OFFSET constraint is analyzed with respect to only a single clock edge. If the OFFSET constraint is used to analyze multiple clock phases or clock edges, as in

source synchronous designs or Dual-Data Rate application, then the OFFSET constraint must be manually adjusted by the clock phase.

The OFFSET constraint does not optimize paths clocked by an internally generated clock. You can use FROM:TO or multi-cycle constraints for these paths, taking into account the clock delay. To obtain an I/O timing analysis on internal clocks or derived clocks, you can use the following options:

- Create a FROM:TO or multi-cycle constraint on these paths
- Determine if the internal clock is related to an external clock signal:

  Change the requirement based upon the relationship between the two clocks. For example, when the internal clock is a "divide by two" version of the external clock, and the original requirement of the OFFSET OUT with the internal clock was 10 ns, then the requirement of the OFFSET OUT with the external clock is 20 ns.

You can specify OFFSET constraints in three levels of coverage, as follows:

- A Global OFFSET applies to all inputs or outputs for a specific clock
- A Group OFFSET identifies a group of input or outputs clocked by a common clock that have the same timing requirement
- A Net-Specific OFFSET specifies the timing by each input or output

OFFSET constraints with a more specific scope override a more general scope.

A group OFFSET overrides a global OFFSET specified for the same I/O. Net-specific OFFSET overrides both global and group OFFSET. This priority rule allows you to start with global OFFSETs, and then to create group or net-specific OFFSET constraint for I/O with special timing requirements.

Use global and group OFFSET constraints to reduce memory usage and runtime. Using wildcards in net-specific OFFSET constraint creates multiple net-specific OFFSET constraints, not a group OFFSET constraint.

A group OFFSET constraint can include both a register group and a pad group. Group OFFSET allows you to group pads or registers to use the same requirement. The register group can be used to identify path source or destination that has different requirements from or to a single pad on a clock edge. You can use the pad group to identify path sources or destinations that have different requirements from or to a group of pads on the same clock edge. You can group and constrain the pads and registers all at once, which is useful if a clock is used on the rising and falling edge for inputs and outputs.

The rising and falling groups require different group OFFSET constraints. In Figure 4, registers A, B, and C are different time groups (TIMEGRP AB = RISING FFS; TIMEGRP C = FALLING FFS;), even though these registers have the same data and clock source. This allows you to perform two different timing analyses for these registers.

```
NET CLK PERIOD = 20nS;
OFFSET = IN 4nS BEFORE CLK TIMEGRP AB;
OFFSET = IN 6nS BEFORE CLK TIMEGRP C;
```

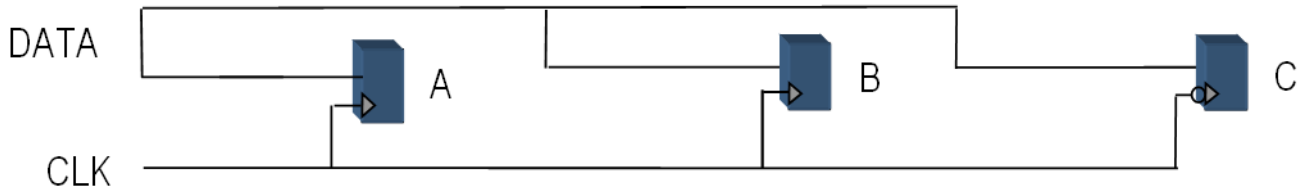


Figure 4: **OFFSET with Different TIMEGRPs**

For CPLD designs, the clock inputs referenced by the OFFSET constraints must be explicitly assigned to a global clock pin (using either a BUFG symbol or applying the BUFG=CLK constraint to an ordinary input). Otherwise, the OFFSET constraint will not be used during timing driven optimization of the design.

What is the OFFSET IN Constraint?

The OFFSET IN constraint is used to define the Pad-To-Setup timing requirement. The OFFSET IN is an external clock-to-data relationship specification. It takes into account the clock delay, clock edge, and DLL/DCM introduced clock phase when analyzing the setup requirement (data_delay + setup – clock_delay – clock_arrival). Clock arrival takes into account any clock phase generated by the DLL/DCM or clock edge.

If the timing report does not display a clock arrival time, then the timing analysis tools did not analyze a PERIOD constraint for that specific synchronous element.

When creating pad-to-setup requirements, make sure to incorporate any phase or PERIOD adjustment factor into the value specified for an OFFSET IN constraint. For the following example, refer to the schematic in Figure 3. If the net from the CLK90 pin of the DLL/DCM clocks your register, then the OFFSET value should be adjusted by a quarter of the PERIOD constraint value. For example, if the PERIOD constraint value is 20 ns and is from the CLK90 of the DCM, the OFFSET IN value should be adjusted by an additional 5 ns:

Original Constraint: NET "PAD_IN" OFFSET = IN 10 BEFORE "PADCLKIN";

Modified Constraint: NET "PAD_IN" OFFSET = IN 15 BEFORE "PADCLKIN";

Note: The clock net name required for OFFSET constraints is the clock net name attached to the IPAD. In this case, it is "PADCLKIN", not "CLK90".

OFFSET IN BEFORE

The OFFSET IN BEFORE constraint defines the time available for data to propagate from the pad and setup at the synchronous element. You can visualize this as the time that the data arrives at the edge of the device before the next clock edge arrives at the device. This “OFFSET = IN 2 ns BEFORE clock_pad” constraint reads that the data

will be valid at the input data pad, some time period (2 ns) BEFORE the reference clock edge arrives at the clock pad. The tools automatically calculate and control internal data and clock delays to meet the flip-flop setup time. See Figure 1 and Figure 5.

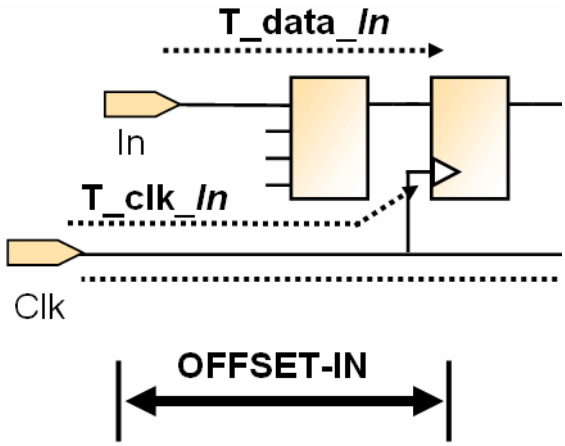


Figure 5: **Circuit Diagram with Calculation Variables for OFFSET IN BEFORE Constraints**

The following equation defines the setup relationship:

TData + TSetup - TClock <= Toffset_IN_BEFORE

The OFFSET IN requirement value is used as a setup time requirement of the FPGA during the setup time analysis. The VALID keyword is used in conjunction with the requirement to create a hold-time requirement during a hold-time analysis. The VALID keyword specifies the duration of the incoming data valid window, and the timing analysis tools perform a hold-time analysis. By default, the VALID value is equal to the OFFSET time requirement, which specifies a zero hold-time requirement. See Figure 6.

The following equation defines the hold relationship:

TClock – Tdata + Thold <= Toffset_IN_BEFORE_VALID

The following are examples of the OFFSET IN with the VALID keyword:

- TIMEGRP DATA_IN OFFSET IN = 1 VALID 3 BEFORE CLK TIMEGRP FF_RISING;
- TIMEGRP DATA_IN OFFSET IN = 4 VALID 3 BEFORE CLK TIMEGRP FF_FALLING;

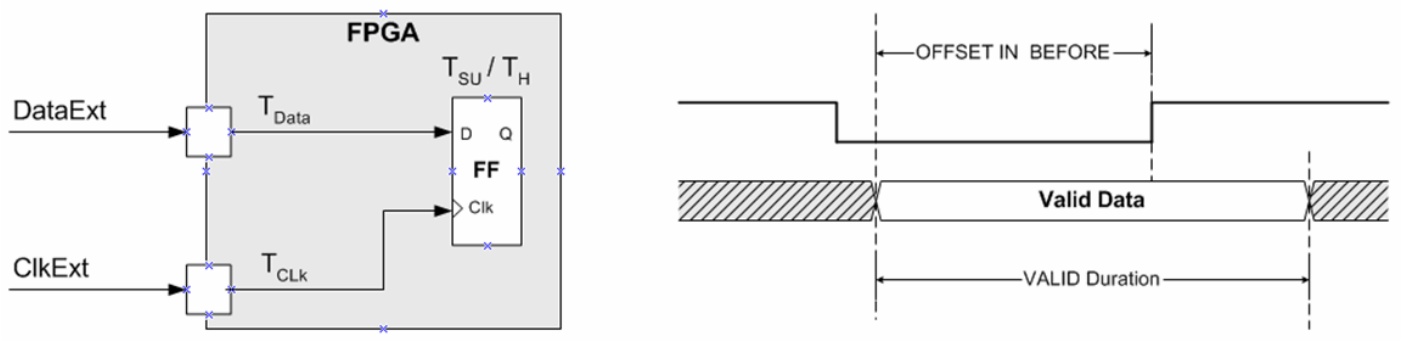


Figure 6: **OFFSET IN Constraint with VALID Keyword**

The OFFSET Constraint is analyzed with respect to the rising clock edge, which is specified with the HIGH keyword of the PERIOD constraint. The OFFSET HIGH/LOW keyword can be used to override the HIGH/LOW keyword defined by the PERIOD constraint. This is extremely useful for DDR design, with a 50% duty cycle, when the signal is capturing data on the rising and falling clock edges or producing data on rising and falling clock edges. For example, if the PERIOD constraint has the HIGH keyword and the OFFSET has the LOW keyword, the falling edged synchronous elements will have the clock arrival time set to zero.

The following is an example of the OFFSET IN with the HIGH/LOW keyword:

TIMEGRP DATA_IN OFFSET IN = 1 VALID 3 BEFORE CLK LOW;

The equation for external setup included in the OFFSET IN analysis of the FPGA is Data Delay plus the Flip-Flop Setup time minus the prorated version of the Clock Path Delay. The longer the clock path delay, the smaller the external setup time. The prorated clock path delay is used to obtain an accurate setup time analysis. The general prorating factors are 85% for Global Routing and 80% for Local Routing.

> The prorated clock path delays are not used for device families that are older than Virtex™-II.

The equation for external hold included in the OFFSET IN analysis of the FPGA is: Clock Path Delay plus Flip-Flop Hold time minus the prorated version of the Data Delay. If the data delay is longer than the clock delay, the end result is a smaller hold time. The prorated data delays are similar to the prorated values in the setup analysis.

> The prorated data delays are not used for device families older than Virtex-II.

Simple Example

A simple example of the OFFSET IN constraint has an initial clock edge at 0 ns based upon the PERIOD constraint. The timing report displays the initial clock edge as the clock arrival time. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example report is shown below.

> If the timing report does not display a clock arrival time, then the timing analysis tools did not recognize a PERIOD constraint for that particular synchronous element.

In Figure 7, the OFFSET requirement is 3 ns before the initial clock edge. The equation used in timing analysis is as follows:
Slack = (Requirement - (Data Path - Clock Path - Clock Arrival))

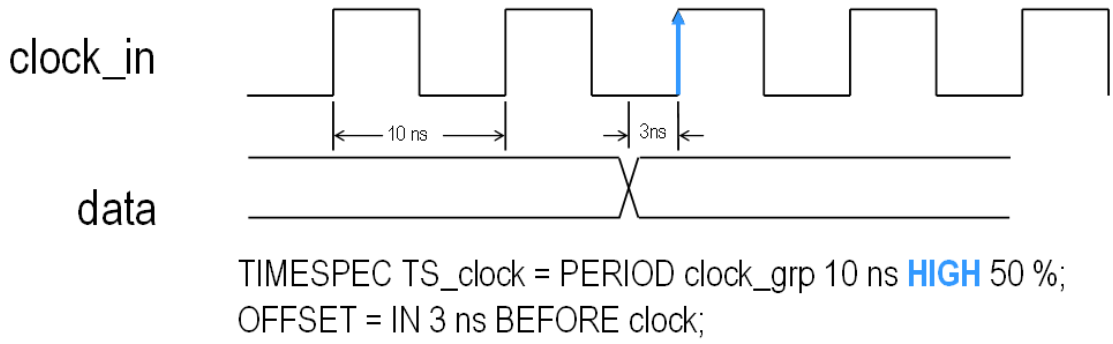


Figure 7: **Timing Diagram of Simple OFFSET IN Constraint**

Timing Report Example

```
Slack:                  -0.191ns (requirement -(data path - clock path - clock arrival + uncertainty))
  Source:                 reset (PAD)
  Destination:            my_oddrA_ODDR_inst/FF0 (FF)
  Destination Clock:      clock0_ddr_bufg rising at 0.000ns
  Requirement:            3.000ns
  Data Path Delay:        2.784ns (Levels of Logic = 1)
  Clock Path Delay:       -0.168ns (Levels of Logic = 3)
  Clock Uncertainty:      0.239ns

  Data Path: reset to my_oddrA_ODDR_inst/FF0
    Location              Delay type       Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
    K14.I                 Tiopi              0.747    reset
                                                      reset
                                                      reset_IBUF
    OLOGIC_X1Y188.SR      net (fanout=40)    1.136    reset_IBUF
    OLOGIC_X1Y188.CLK     Tosrck             0.901    OutAz_0_OBUF
                                                      my_oddrA_ODDR_inst/FF0
    ------------------------------------------------  ---------------------
    Total                                    2.784ns (1.648ns logic, 1.136ns route)
                                                     (59.2% logic, 40.8% route)

  Clock Path: clock0 to my_oddrA_ODDR_inst/FF0
    Location              Delay type       Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ------------------------------------------------  -------------------
E19.I                 Tiopi            0.639       clock0
                                                   clock0
                                                   MY_ddr_dcm/CLKIN_IBUFG_INST
    DCM_ADV_X0Y4.CLKIN    net (fanout=1)     0.903   MY_ddr_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y4.CLKFX    Tdmcko_CLKFX      -5.568      MY_ddr_dcm/DCM_ADV_INST
                                                      MY_ddr_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y19.I0     net (fanout=1)     1.368      MY_ddr_dcm/CLKFX_BUF
    BUFGCTRL_X0Y19.O      Tbgcko_O           0.644   MY_ddr_dcm/CLKFX_BUFG_INST
                                                      MY_ddr_dcm/CLKFX_BUFG_INST
    OLOGIC_X1Y188.CLK     net (fanout=24)    1.846      clock0_ddr_bufg
    ------------------------------------------------  ---------------------
    Total                                   -0.168ns (-4.285ns logic, 4.117ns route)
```

Two-Phase Example

A two-phase or both clock edges example of the OFFSET IN constraint has an initial clock edge that correlates to the two edges of the clock. The first clock edge is at 0 ns based upon the PERIOD constraint, and the second clock edge is at half the PERIOD constraint. The timing report displays the clock arrival time for each edge of the clock.

The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below. In this example, the PERIOD constraint has the clock arrival on the falling edge, based upon the LOW keyword. So, the clock arrival time for the falling edge synchronous elements will be a zero and the rising edge synchronous elements will be at half the PERIOD constraint. If both edges are used, as in Dual-Data Rate, then two OFFSET constraints are created; one for each clock edge. In Figure 8, the OFFSET requirement is 3 ns before the initial clock edge. If the PERIOD constraint had the HIGH keyword, the LOW keyword on the OFFSET IN, the following constraints would produce the same example report:

- TIMESPEC TS_clock = PERIOD clock 10 ns HIGH 50%;
- OFFSET = IN 3 ns BEFORE clock LOW

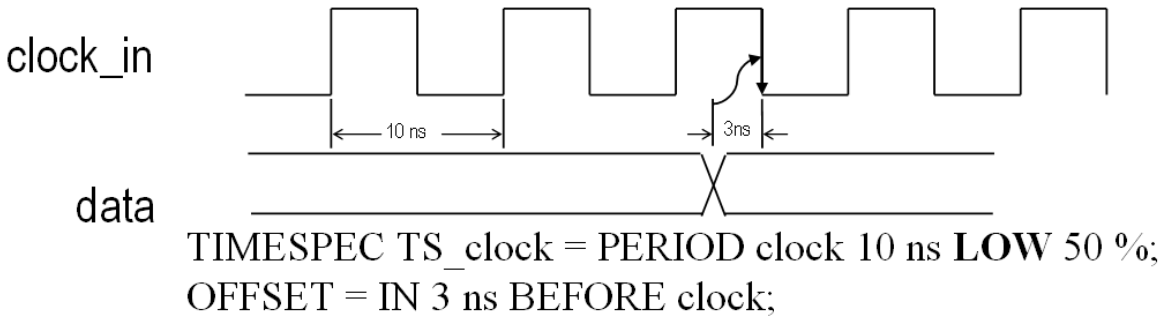


Figure 8: **Timing Diagram with Two-Phase OFFSET IN Constraints**

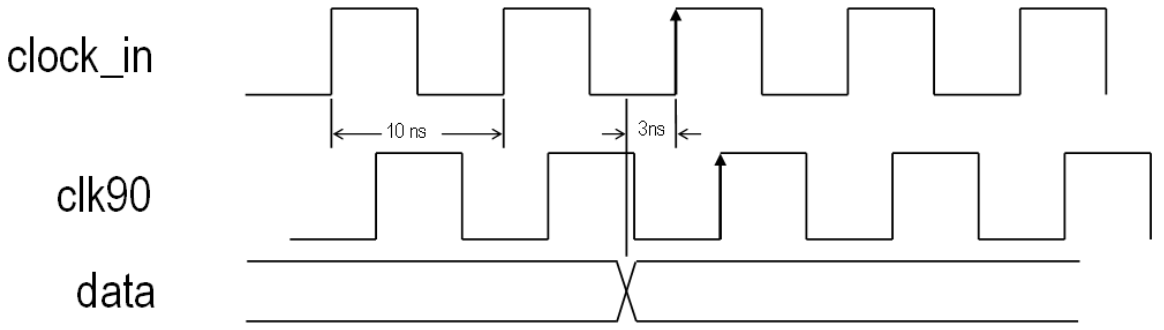
Timing Report Example

```
Slack:                  0.231ns (requirement - (data path - clock path - clock arrival + uncertainty))
  Source:                 DataD<9> (PAD)
  Destination:            TmpAa_1 (FF)
  Destination Clock:      clock0_ddr_bufg falling at 0.000ns
  Requirement:            3.000ns
  Data Path Delay:        2.492ns (Levels of Logic = 2)
  Clock Path Delay:       -0.038ns (Levels of Logic = 3)
  Clock Uncertainty:      0.239ns

  Data Path: DataD<9> to TmpAa_1
    Location              Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    R9.I                  Tiopi              0.709      DataD<9>
                                                        DataD<9>
                                                        DataD_9_IBUF
    SLICE_X67Y142.F4      net (fanout=1)     1.606      DataD_9_IBUF
    SLICE_X67Y142.CLK     Tas                0.177      TmpAa<1>
                                                        SumAa<1>1
                                                        TmpAa_1
    -------------------------------------------------  ---------------------------
    Total                                    2.492ns (0.886ns logic, 1.606ns route)
```

```
                                                (35.6% logic, 64.4% route)

Clock Path: clock0 to TmpAa_1
  Location             Delay type      Delay(ns)  Physical Resource
                                                  Logical Resource(s)
  -------------------------------------------------  -------------------
  E19.I                Tiopi           0.639      clock0
                                                  clock0
                                                  MY_ddr_dcm/CLKIN_IBUFG_INST
  DCM_ADV_X0Y4.CLKIN   net (fanout=1)  0.903      MY_ddr_dcm/CLKIN_IBUFG_OUT
  DCM_ADV_X0Y4.CLKFX   Tdmcko_CLKFX   -5.568      MY_ddr_dcm/DCM_ADV_INST
                                                  MY_ddr_dcm/DCM_ADV_INST
  BUFGCTRL_X0Y19.I0    net (fanout=1)  1.368      MY_ddr_dcm/CLKFX_BUF
  BUFGCTRL_X0Y19.O     Tbgcko_O        0.644      MY_ddr_dcm/CLKFX_BUFG_INST
                                                  MY_ddr_dcm/CLKFX_BUFG_INST
  SLICE_X67Y142.CLK    net (fanout=24) 1.976      clock0_ddr_bufg
  -------------------------------------------------  ---------------------------
  Total                                -0.038ns (-4.285ns logic, 4.247ns route)
```

Phase-Shifted Example

A DCM phase-shifted clock, CLK90, example of the OFFSET IN constraint has an initial clock edge at 0 ns based upon the PERIOD constraint. Since the clock is phase-shifted by the DCM, the timing report displays the clock arrival time as the phase-shifted amount. If the CLK90 output is used, then the phase-shifted amount will be a quarter of the PERIOD. In this example, the PERIOD constraint has the initial clock arrival on the rising edge, but the clock arrival value is at 2.5 ns. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below. In Figure 9, the OFFSET requirement is 3 ns before the initial clock edge.



TIMESPEC TS_clock = PERIOD clock_grp 10 ns **HIGH** 50 %;
OFFSET = IN 3 ns BEFORE clock;

Figure 9: **Timing Diagram for Phase-shifted Clock In OFFSET IN Constraint**

Timing Report Example

```
Slack:                -2.308ns (requirement -(data path - clock path - clock arrival + uncertainty))
  Source:               reset (PAD)
  Destination:          my_oddrA_ODDR_inst/FF0 (FF)
  Destination Clock:    clock90_bufg rising at 2.500ns
  Requirement:          3.000ns
  Data Path Delay:      2.784ns (Levels of Logic = 1)
  Clock Path Delay:     -0.168ns (Levels of Logic = 3)
  Clock Uncertainty:    0.239ns

  Data Path: reset to my_oddrA_ODDR_inst/FF0
    Location             Delay type       Delay(ns)  Physical Resource
                                                     Logical Resource(s)
    -------------------------------------------------  -------------------
    K14.I                Tiopi             0.747     reset
                                                     reset
                                                     reset_IBUF
    OLOGIC_X1Y188.SR     net (fanout=40)   1.136     reset_IBUF
    OLOGIC_X1Y188.CLK    Tosrck            0.901     OutAz_0_OBUF
                                                     my_oddrA_ODDR_inst/FF0
    -------------------------------------------------  ---------------------------
    Total                                  2.784ns (1.648ns logic, 1.136ns route)
                                                    (59.2% logic, 40.8% route)

  Clock Path: clock0 to my_oddrA_ODDR_inst/FF0
    Location             Delay type       Delay(ns)  Physical Resource
                                                     Logical Resource(s)
    -------------------------------------------------  -------------------
    E19.I                Tiopi             0.639     clock0
                                                     clock0
                                                     MY_ddr_dcm/CLKIN_IBUFG_INST
    DCM_ADV_X0Y4.CLKIN   net (fanout=1)    0.903     MY_ddr_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y4.CLKFX   Tdmcko_CLKFX     -5.568     MY_ddr_dcm/DCM_ADV_INST
                                                     MY_ddr_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y19.I0    net (fanout=1)    1.368     MY_ddr_dcm/CLKFX_BUF
    BUFGCTRL_X0Y19.O     Tbgcko_O          0.644     MY_ddr_dcm/CLKFX_BUFG_INST
                                                     MY_ddr_dcm/CLKFX_BUFG_INST
    OLOGIC_X1Y188.CLK    net (fanout=24)   1.846     clock0_ddr_bufg
    -------------------------------------------------  ---------------------------
    Total                                 -0.168ns (-4.285ns logic, 4.117ns route)
```

Fixed Phase-Shifted Example

A DCM fixed phase-shifted clock example of the OFFSET IN constraint has an initial clock edge at 0 ns based upon the PERIOD constraint. Since the clock is phase-shifted by the DCM, the timing report displays the clock arrival time as the phase-shifted amount. If the CLK0 output is phase-shifted by a user-specified amount, then the

phase-shifted amount will be a percentage of the PERIOD. In this example, the PERIOD constraints has the initial clock arrival on the rising edge, but the clock arrival value is at the fixed phase-shifted amount, as seen in the example timing report. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below. In Figure 10, the OFFSET requirement is 3 ns before the initial clock edge.

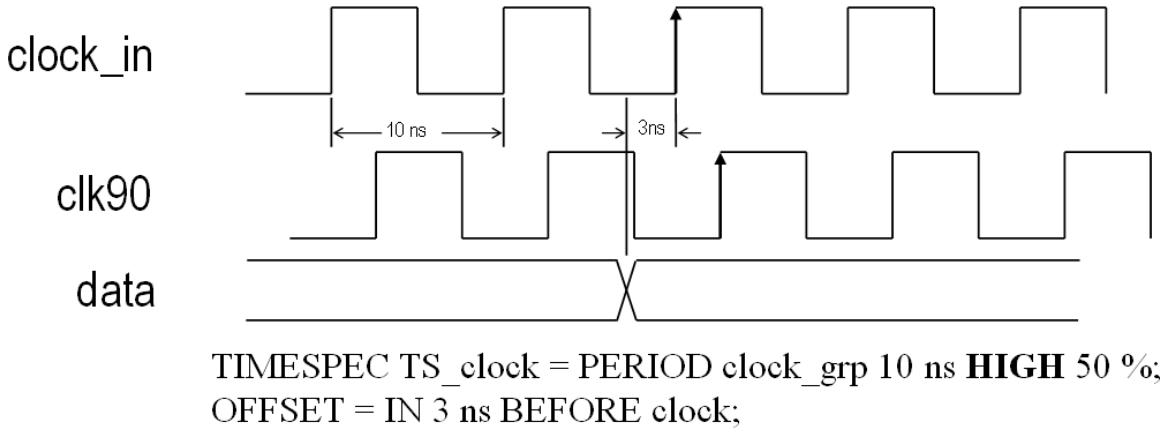


Figure 10: **Timing Diagram of Fixed Phase-shifted Clock in OFFSET IN Constraint**

Timing Report Example

```
Slack:                  -4.269ns (requirement -(data path - clock path - clock arrival + uncertainty))
  Source:                 DataD<9> (PAD)
  Destination:            TmpAa_1 (FF)
  Destination Clock:      clock1_fixed_bufg rising at 4.500ns
  Requirement:            3.000ns
  Data Path Delay:        2.492ns (Levels of Logic = 2)
  Clock Path Delay:       -0.038ns (Levels of Logic = 3)
  Clock Uncertainty:      0.239ns

  Data Path: DataD<9> to TmpAa_1
    Location              Delay type       Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    -------------------------------------------------  -------------------
    R9.I                  Tiopi             0.709     DataD<9>
                                                      DataD<9>
                                                      DataD_9_IBUF
    SLICE_X67Y142.F4      net (fanout=1)    1.606     DataD_9_IBUF
    SLICE_X67Y142.CLK     Tas               0.177     TmpAa<1>
                                                      SumAa<1>1
                                                      TmpAa_1
    -------------------------------------------------  ---------------------------
    Total                                   2.492ns (0.886ns logic, 1.606ns route)
                                                    (35.6% logic, 64.4% route)
```

```
Clock Path: clock0 to TmpAa_1
  Location             Delay type       Delay(ns)  Physical Resource
                                                   Logical Resource(s)
  -------------------------------------------------  -------------------
  E19.I                Tiopi              0.639    clock0
                                                   clock0
                                                   MY_ddr_dcm/CLKIN_IBUFG_INST
  DCM_ADV_X0Y4.CLKIN   net (fanout=1)     0.903    MY_ddr_dcm/CLKIN_IBUFG_OUT
  DCM_ADV_X0Y4.CLKFX   Tdmcko_CLKFX      -5.568    MY_ddr_dcm/DCM_ADV_INST
                                                   MY_ddr_dcm/DCM_ADV_INST
  BUFGCTRL_X0Y19.I0    net (fanout=1)     1.368    MY_ddr_dcm/CLKFX_BUF
  BUFGCTRL_X0Y19.O     Tbgcko_O           0.644    MY_ddr_dcm/CLKFX_BUFG_INST
                                                   MY_ddr_dcm/CLKFX_BUFG_INST
  SLICE_X67Y142.CLK    net (fanout=24)    1.976    clock0_ddr_bufg
  -------------------------------------------------  ---------------------------
  Total                                  -0.038ns (-4.285ns logic, 4.247ns route)
```

Dual-Data Rate Example

A Dual-Data Rate example of the OFFSET IN constraint has an initial clock edge at 0 ns and half the PERIOD constraint, which correlates to the two clock edges. The timing report displays the clock arrival time for each edge of the clock. Since the data is being clocked in on both edges of the clock, the clock arrival time for the falling edge needs to be managed. The timing analysis tools do not automatically adjust any of the clock phases during analysis, so the constraints must be manually adjusted. The timing analysis tools offer two options to manage the falling edge clock arrival time. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below.

The first option is to create two time groups, one for rising edge synchronous elements and the second for the falling edge synchronous elements. Then create an OFFSET IN constraint for each time group, the second OFFSET IN constraint will have a different requirement. The falling edge OFFSET IN constraint requirement should be the "original requirement" minus half of the PERIOD constraint. So, if you have the original requirement as 3 ns with a PERIOD of 10 ns, the falling edge OFFSET IN constraint requirement is -2 ns. This will compensate for the clock arrival time associated with the falling edge synchronous elements. The negative value is legal in the constraints language.

The second option is to create one time group and one corresponding OFFSET IN constraint with the original constraint requirement. The only addition is the LOW keyword (if the PERIOD constraint has the HIGH keyword). If the PERIOD constraint has the LOW keyword, then the OFFSET constraint would use the LOW keyword. This option can only be used if the duty cycle on the clock is 50/50.

In this example the PERIOD constraint has the clock arrival on both the rising edge and falling edge, so the clock arrival value is 0 ns and 5 ns. During the timing analysis, the difference between the rising and falling edges of the clock is added to the falling-edge-data-path analysis, so you need to subtract that difference from the original requirement. In Figure 11, the OFFSET requirement is 3 ns before the initial clock edge.

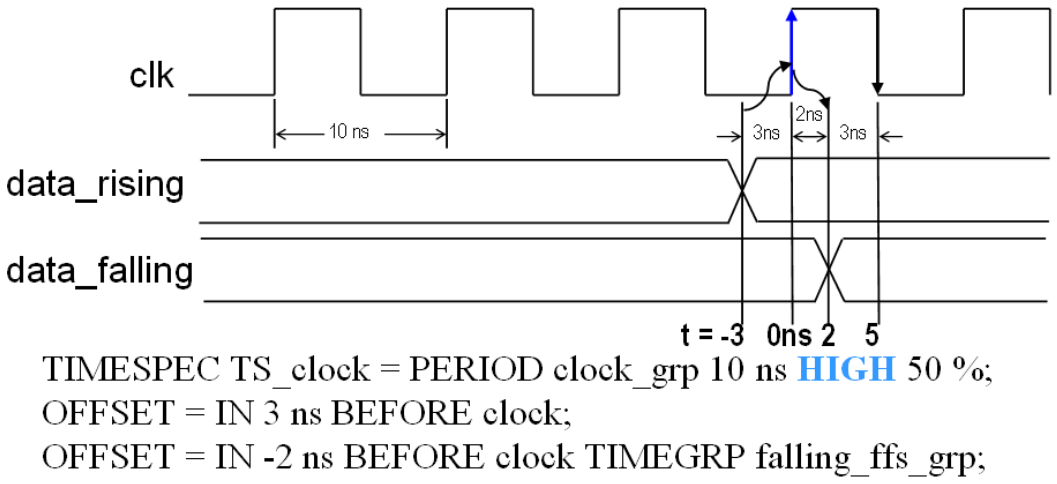


Figure 11: **Timing Diagram for Dual Data Rate in OFFSET IN Constraint**

Timing Report Example for OFFSET = IN 3 ns BEFORE Clock

```
Slack:                  0.101ns (requirement - (data path - clock path - clock arrival + uncertainty))
  Source:                 DataA<3> (PAD)
  Destination:            TmpAa_3 (FF)
  Destination Clock:      clock0_ddr_bufg rising at 0.000ns
  Requirement:            3.000ns
  Data Path Delay:        2.654ns (Levels of Logic = 2)
  Clock Path Delay:       -0.006ns (Levels of Logic = 3)
  Clock Uncertainty:      0.239ns

  Data Path: DataA<3> to TmpAa_3
    Location              Delay type         Delay(ns)  Physical Resource
                                                        Logical Resource(s)
    -------------------------------------------------  -------------------
    AF20.I                Tiopi               0.762    DataA<3>
                                                       DataA<3>
                                                       DataA_3_IBUF
    SLICE_X69Y140.F4      net (fanout=2)      1.715    DataA_3_IBUF
    SLICE_X69Y140.CLK     Tas                 0.177    TmpAa<3>
                                                       SumAa<3>1
                                                       TmpAa_3
    -------------------------------------------------  ---------------------------
    Total                                     2.654ns (0.939ns logic, 1.715ns route)
                                                      (35.4% logic, 64.6% route)

  Clock Path: clock0 to TmpAa_3
    Location              Delay type          Delay(ns)  Physical Resource
                                                         Logical Resource(s)
```

```
    ----------------------------------------------------  -------------------
    E19.I                 Tiopi                 0.639     clock0
                                                          clock0
                                                          MY_ddr_dcm/CLKIN_IBUFG_INST
    DCM_ADV_X0Y4.CLKIN    net (fanout=1)        0.903     MY_ddr_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y4.CLKFX    Tdmcko_CLKFX         -5.568     MY_ddr_dcm/DCM_ADV_INST
                                                          MY_ddr_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y19.I0     net (fanout=1)        1.368     MY_ddr_dcm/CLKFX_BUF
    BUFGCTRL_X0Y19.O      Tbgcko_O              0.644     MY_ddr_dcm/CLKFX_BUFG_INST
                                                          MY_ddr_dcm/CLKFX_BUFG_INST
    SLICE_X69Y140.CLK     net (fanout=24)       2.008     clock0_ddr_bufg
    ----------------------------------------------------  ---------------------------
    Total                                      -0.006ns (-4.285ns logic, 4.279ns route)
```

Timing Report Example for OFFSET = IN -2 ns BEFORE Clock

```
Slack:                -2.755ns (requirement -(data path - clock path - clock arrival + uncertainty))
  Source:               DataA<3> (PAD)
  Destination:          TmpAa_3 (FF)
  Destination Clock:    clock0_ddr_bufg falling at 5.000ns
  Requirement:          -2.000ns
  Data Path Delay:      2.654ns (Levels of Logic = 2)
  Clock Path Delay:     -0.006ns (Levels of Logic = 3)
  Clock Uncertainty:    0.239ns

  Data Path: DataA<3> to TmpAa_3
    Location              Delay type       Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ----------------------------------------------  -------------------
    AF20.I                Tiopi              0.762     DataA<3>
                                                      DataA<3>
                                                      DataA_3_IBUF
    SLICE_X69Y140.F4      net (fanout=2)     1.715     DataA_3_IBUF
    SLICE_X69Y140.CLK     Tas                0.177     TmpAa<3>
                                                      SumAa<3>1
                                                      TmpAa_3
    ----------------------------------------------  ---------------------------
    Total                                    2.654ns (0.939ns logic, 1.715ns route)
                                                     (35.4% logic, 64.6% route)

  Clock Path: clock0 to TmpAa_3
    Location              Delay type         Delay(ns)  Physical Resource
                                                      Logical Resource(s)
    ----------------------------------------------  -------------------
    E19.I                 Tiopi                0.639     clock0
                                                      clock0
                                                      MY_ddr_dcm/CLKIN_IBUFG_INST
```

```
DCM_ADV_X0Y4.CLKIN    net (fanout=1)       0.903     MY_ddr_dcm/CLKIN_IBUFG_OUT
DCM_ADV_X0Y4.CLKFX    Tdmcko_CLKFX        -5.568     MY_ddr_dcm/DCM_ADV_INST
                                                     MY_ddr_dcm/DCM_ADV_INST
BUFGCTRL_X0Y19.I0     net (fanout=1)       1.368     MY_ddr_dcm/CLKFX_BUF
BUFGCTRL_X0Y19.O      Tbgcko_O             0.644     MY_ddr_dcm/CLKFX_BUFG_INST
                                                     MY_ddr_dcm/CLKFX_BUFG_INST
SLICE_X69Y140.CLK     net (fanout=24)      2.008     clock0_ddr_bufg
-----------------------------------------------  ---------------------------
Total                                     -0.006ns (-4.285ns logic, 4.279ns route)
```

OFFSET IN AFTER

The OFFSET IN AFTER constraint describes the time used by the data external to the FPGA. OFFSET IN subtracts this time from the PERIOD declared for the clock to determine the time available for the data to propagate from the pad to the setup at the synchronous element. You can visualize this time as the difference of data arriving at the edge of the device after the current clock edge arrives at the edge of the device. This “OFFSET = IN 2 ns AFTER clock_pad” constraint reads that the data to be registered in the FPGA is available on the FPGA’s input pad, some time period (2ns), AFTER the reference clock edge is recognized by the upstream device. To adhere to the OFFSET constraint syntax, assume no skew on CLK between the devices (see Figure 1). The following equation defines this relationship:

TData + TSetup - TClock <= TPeriod – Toffset_IN_AFTER

A PERIOD or FREQUENCY constraint is required for OFFSET IN constraints with the AFTER keyword.

What is the OFFSET OUT Constraint?

The OFFSET OUT constraint is used to define the clock-to-pad timing requirements. The OFFSET OUT constraint is an external clock-to-data specification and takes into account the clock delay, clock edge, and DLL/DCM introduced clock phase when analyzing the clock-to-out requirements (clock_delay + clock_to_out + data_delay + clock_arrival). Clock arrival time takes into account any clock phase generated by the DLL/DCM or clock edge. If the timing report does not display a clock arrival time, then the timing analysis tools did not analyze a PERIOD constraint for that specific synchronous element.

When you create clock-to-pad requirements, be sure to incorporate any phase or PERIOD adjustment factor into the value specified for an OFFSET OUT constraint. For the following example, refer to Figure 2. If your register is clocked by the net from the CLK90 pin of the DLL, which has a PERIOD of 20 ns, the OFFSET value should be adjusted by 5 ns less than the original constraint:

Original Constraint: NET "PAD_OUT" OFFSET = OUT 15 AFTER "PADCLKIN";

Modified Constraint: NET "PAD_OUT" OFFSET = OUT 10 AFTER "PADCLKIN";

OFFSET OUT AFTER

The OFFSET OUT AFTER constraint defines the time available for the data to propagate from the synchronous element to the pad. You can visualize this time as the data leaving the edge of the device after the current clock edge arrives at the edge of the device. This “OFFSET = OUT 2 ns AFTER clock_pad” constraint reads that the

data to be registered in the downstream device is available on the FPGA's data output pad, some time period (2 ns), AFTER the reference clock pulse is recognized by the FPGA, at the clock pad. See Figure 2 and Figure 12.

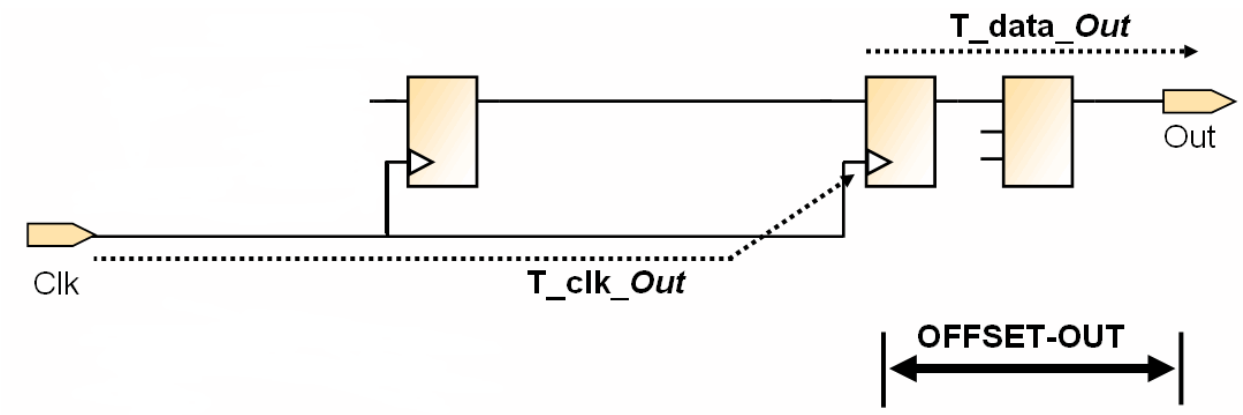


Figure 12: **Circuit Diagram with Calculation Variables for OFFSET OUT AFTER Constraints**

The following equation defines this relationship:

TQ + TClock2Out + TClock <= Toffset_OUT_AFTER

The analysis of this constraint involves ensuring that the maximum delay along the reference path (CLK_SYS to COMP) and the maximum delay along the data path (COMP to Q_OUT) do not exceed the specified offset.

The OFFSET HIGH/LOW keyword can be used to override the HIGH/LOW keyword defined by the PERIOD constraint. This is very useful for DDR design, with a 50% duty cycle, when the signal is capturing data on the rising and falling clock edges or producing data on a rising and falling clock edges. For example, the PERIOD constraint has the HIGH keyword and the OFFSET has the LOW keyword, the falling edged synchronous elements will have the clock arrival time set to zero.

The following is an example of the OFFSET OUT with the HIGH/LOW keyword:

TIMEGRP DATA_OUT OFFSET OUT = 10 AFTER CLK LOW;

Simple Example

A simple example of the OFFSET OUT constraints has the initial clock edge at 0 ns based upon the PERIOD constraint. The timing report displays the initial clock edge as the clock arrival time. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below.

If the timing report does not display a clock arrival time, then the timing analysis tools did not recognize a PERIOD constraint for that particular synchronous element.

In Figure 13, the OFFSET requirement is 3 ns. The equation used in timing analysis is as follows:
Slack = (Requirement - (Clock Arrival + Clock Path + Data Path))

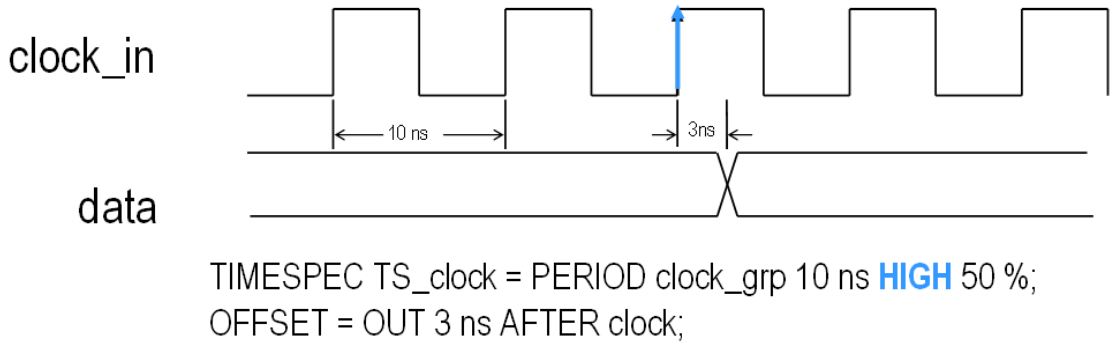


Figure 13: **Timing Diagram of simple OFFSET OUT Constraint**

Timing Report Example

```
Slack:                  -0.865ns (requirement -(clock arrival + clock path + data path + uncertainty))
  Source:                 OutD_7 (FF)
  Destination:            OutD<7> (PAD)
  Source Clock:           clock3_std_bufg rising at 0.000ns
  Requirement:            3.000ns
  Data Path Delay:        3.405ns (Levels of Logic = 1)
  Clock Path Delay:       0.280ns (Levels of Logic = 3)
  Clock Uncertainty:      0.180ns

  Clock Path: clock3 to OutD_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D20.I                Tiopi                 0.775   clock3
                                                       clock3
                                                       MY_Std_dcm/CLKIN_IBUFG_INST
    DCM_ADV_X0Y6.CLKIN   net (fanout=1)        1.035   MY_Std_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y6.CLK0    Tdmcko_CLK           -6.420   MY_Std_dcm/DCM_ADV_INST
                                                       MY_Std_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y26.I0    net (fanout=1)        1.718   MY_Std_dcm/CLK0_BUF
    BUFGCTRL_X0Y26.O     Tbgcko_O              0.700   MY_Std_dcm/CLK0_BUFG_INST
                                                       MY_Std_dcm/CLK0_BUFG_INST
    OLOGIC_X2Y187.CLK    net (fanout=9)        2.472   clock3_std_bufg
    -------------------------------------------------  ---------------------------
    Total                                      0.280ns (-4.945ns logic, 5.225ns route)

  Data Path: OutD_7 to OutD<7>
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
```

```
-------------------------------------------------  -------------------
OLOGIC_X2Y187.OQ     Tockq                 0.406   OutD_7
                                                   OutD_7
D4.O                 net (fanout=1)        0.002   OutD_7
D4.PAD               Tioop                 2.997   OutD<7>
                                                   OutD_7_OBUF
                                                   OutD<7>
-------------------------------------------------  ---------------------------
Total                                      3.405ns (3.403ns logic, 0.002ns route)
                                                   (99.9% logic, 0.1% route)
```

Two-Phase Example

A two-phase (use of both edges) example of the OFFSET OUT constraint has the initial clock edge that correlates to the two edges of the clock. The first clock edge is at 0 ns based upon the PERIOD constraint and the second clock edge is at half the PERIOD constraint. The timing report displays the clock arrival time for each edge of the clock. In this example, the PERIOD constraint has the clock arrival on the falling edge, based upon the LOW keyword. Consequently, the clock arrival time for the falling edge synchronous elements will be zero and the rising edge synchronous elements will be at half the PERIOD constraint. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below. In Figure 14, the OFFSET requirement is 3 ns.

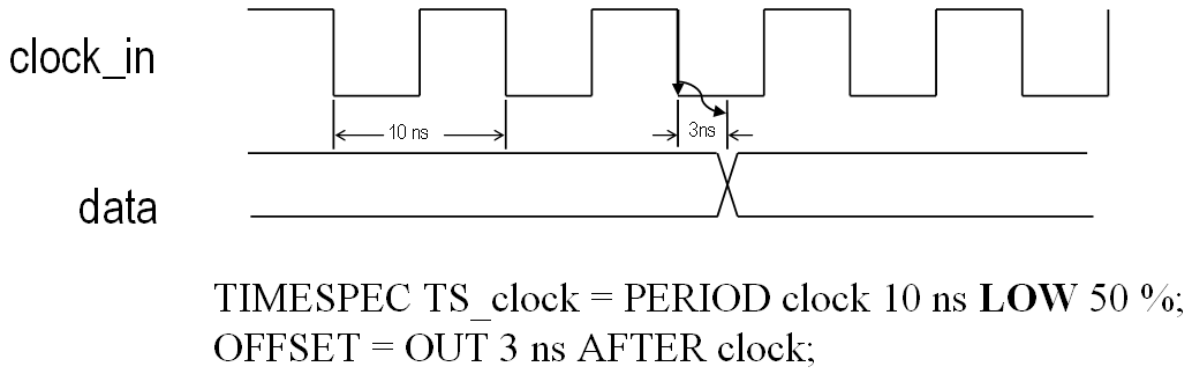


Figure 14: **Timing Diagram of Two-Phase in OFFSET OUT Constraint**

Timing Report Example

```
Slack:                  -0.865ns (requirement -(clock arrival + clock path + data path + uncertainty))
  Source:                 OutD_7 (FF)
  Destination:            OutD<7> (PAD)
  Source Clock:           clock3_std_bufg falling at 0.000ns
  Requirement:            .3.000ns
  Data Path Delay:        3.405ns (Levels of Logic = 1)
  Clock Path Delay:       0.280ns (Levels of Logic = 3)
  Clock Uncertainty:      0.180ns


  Clock Path: clock3 to OutD_7
```

```
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  D20.I                Tiopi                 0.775   clock3
                                                     clock3
                                                     MY_Std_dcm/CLKIN_IBUFG_INST
  DCM_ADV_X0Y6.CLKIN   net (fanout=1)        1.035   MY_Std_dcm/CLKIN_IBUFG_OUT
  DCM_ADV_X0Y6.CLK0    Tdmcko_CLK           -6.420   MY_Std_dcm/DCM_ADV_INST
                                                     MY_Std_dcm/DCM_ADV_INST
  BUFGCTRL_X0Y26.I0    net (fanout=1)        1.718   MY_Std_dcm/CLK0_BUF
  BUFGCTRL_X0Y26.O     Tbgcko_O              0.700   MY_Std_dcm/CLK0_BUFG_INST
                                                     MY_Std_dcm/CLK0_BUFG_INST
  OLOGIC_X2Y187.CLK    net (fanout=9)        2.472   clock3_std_bufg
  -------------------------------------------------  ---------------------------
  Total                                      0.280ns (-4.945ns logic, 5.225ns route)

Data Path: OutD_7 to OutD<7>
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  OLOGIC_X2Y187.OQ     Tockq                 0.406   OutD_7
                                                     OutD_7
  D4.O                 net (fanout=1)        0.002   OutD_7
  D4.PAD               Tioop                 2.997   OutD<7>
                                                     OutD_7_OBUF
                                                     OutD<7>
  -------------------------------------------------  ---------------------------
  Total                                      3.405ns (3.403ns logic, 0.002ns route)
                                                     (99.9% logic, 0.1% route)
```

Phase-Shifted Example

A DCM phase-shifted, CLK90, example of the OFFSET OUT constraint has the initial clock edge at 0 ns based upon the PERIOD constraint. Since the clock is phase-shifted by the DCM, the timing report displays the clock arrival time as the phase-shifted amount. If the CLK90 output is used, then the phase-shifted amount will be a quarter of the PERIOD. The clock arrival time corresponds to the phase shifting amount, which is 2.5 ns in this case. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below. In Figure 15, the OFFSET requirement is 5 ns.

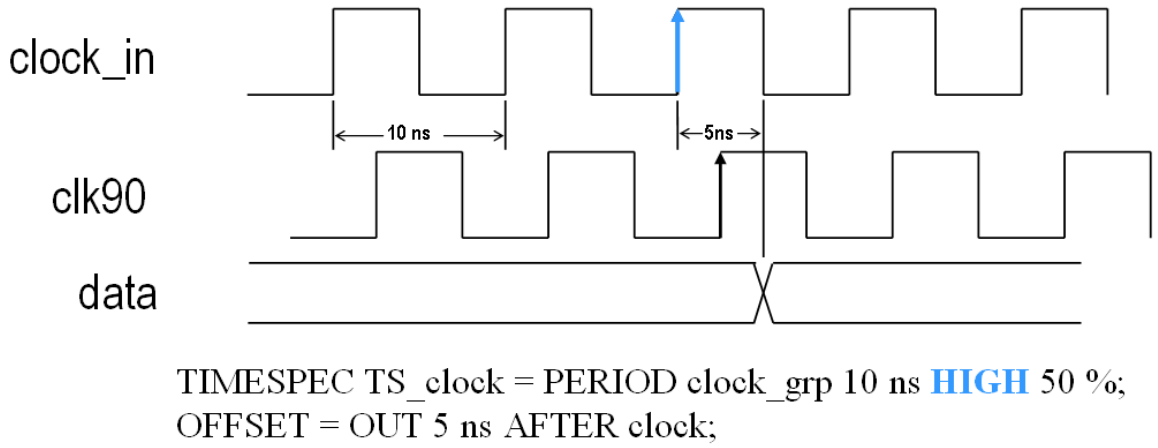


Figure 15: **Timing Diagram of Phase-shifted Clock in OFFSET OUT Constraint**

Timing Report Example

```
Slack:                  -1.365ns (requirement -(clock arrival + clock path + data path + uncertainty))
  Source:                 OutD_7 (FF)
  Destination:            OutD<7> (PAD)
  Source Clock:           clock3_std_bufg rising at 2.500ns
  Requirement:            5.000ns
  Data Path Delay:        3.405ns (Levels of Logic = 1)
  Clock Path Delay:       0.280ns (Levels of Logic = 3)
  Clock Uncertainty:      0.180ns

  Clock Path: clock3 to OutD_7
    Location             Delay type         Delay(ns)  Physical Resource
                                                       Logical Resource(s)
    -------------------------------------------------  -------------------
    D20.I                Tiopi                 0.775   clock3
                                                       clock3
                                                       MY_Std_dcm/CLKIN_IBUFG_INST
    DCM_ADV_X0Y6.CLKIN   net (fanout=1)        1.035   MY_Std_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y6.CLK0    Tdmcko_CLK           -6.420   MY_Std_dcm/DCM_ADV_INST
                                                       MY_Std_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y26.I0    net (fanout=1)        1.718   MY_Std_dcm/CLK0_BUF
    BUFGCTRL_X0Y26.O     Tbgcko_O              0.700   MY_Std_dcm/CLK0_BUFG_INST
                                                       MY_Std_dcm/CLK0_BUFG_INST
    OLOGIC_X2Y187.CLK    net (fanout=9)        2.472   clock3_std_bufg
    -------------------------------------------------  ---------------------------
    Total                                      0.280ns (-4.945ns logic, 5.225ns route)

  Data Path: OutD_7 to OutD<7>
    Location             Delay type         Delay(ns)  Physical Resource
```

```
                                                    Logical Resource(s)
--------------------------------------------------  -------------------
OLOGIC_X2Y187.OQ     Tockq                 0.406    OutD_7
                                                    OutD_7
D4.O                 net (fanout=1)        0.002    OutD_7
D4.PAD               Tioop                 2.997    OutD<7>
                                                    OutD_7_OBUF
                                                    OutD<7>
--------------------------------------------------  ---------------------------
Total                                      3.405ns (3.403ns logic, 0.002ns route)
                                                    (99.9% logic, 0.1% route)
```

Fixed Phase-Shifted Example

A DCM fixed phase-shifted example of the OFFSET OUT constraint has the initial clock edge at 0 ns, based upon the PERIOD constraint. Since the clock is phase-shifted by the DCM, the timing report displays the clock arrival time as the phase-shifted amount. If the CLK0 output is phase-shifted by a user-specified amount, then the phase-shifted amount will be a percentage of the PERIOD. In this example, the PERIOD constraint has the initial clock arrival on the rising edge, but the clock arrival value is at the fixed phase-shifted amount (as seen in the example timing report). The clock arrival time corresponds to the phase-shifting amount. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below. In Figure 16, the OFFSET requirement is 5 ns.

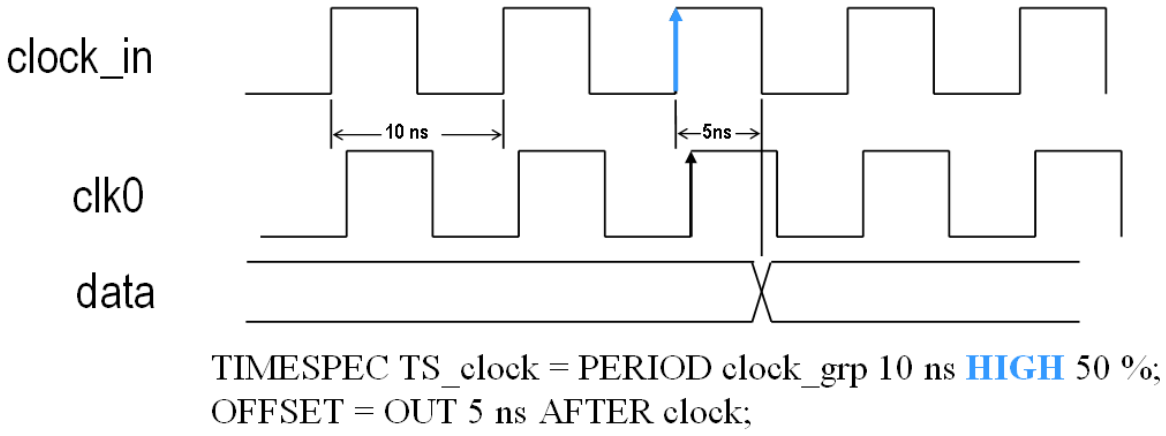


Figure 16: **Timing Diagram of Fixed Phase-shifted Clock in OFFSET OUT Constraint**

Timing Report Example

```
Slack:                  0.535ns (requirement - (clock arrival + clock path + data path + uncertainty))
  Source:                 OutD_7 (FF)
  Destination:            OutD<7> (PAD)
  Source Clock:           clock3_std_bufg rising at 0.600ns
  Requirement:            5.000ns
  Data Path Delay:        3.405ns (Levels of Logic = 1)
  Clock Path Delay:       0.280ns (Levels of Logic = 3)
```

```
Clock Uncertainty:     0.180ns

Clock Path: clock3 to OutD_7
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  D20.I                Tiopi                 0.775   clock3
                                                     clock3
                                                     MY_Std_dcm/CLKIN_IBUFG_INST
  DCM_ADV_X0Y6.CLKIN   net (fanout=1)        1.035   MY_Std_dcm/CLKIN_IBUFG_OUT
  DCM_ADV_X0Y6.CLK0    Tdmcko_CLK           -6.420   MY_Std_dcm/DCM_ADV_INST
                                                     MY_Std_dcm/DCM_ADV_INST
  BUFGCTRL_X0Y26.I0    net (fanout=1)        1.718   MY_Std_dcm/CLK0_BUF
  BUFGCTRL_X0Y26.O     Tbgcko_O              0.700   MY_Std_dcm/CLK0_BUFG_INST
                                                     MY_Std_dcm/CLK0_BUFG_INST
  OLOGIC_X2Y187.CLK    net (fanout=9)        2.472   clock3_std_bufg
  -------------------------------------------------  ---------------------------
  Total                                      0.280ns (-4.945ns logic, 5.225ns route)

Data Path: OutD_7 to OutD<7>
  Location             Delay type         Delay(ns)  Physical Resource
                                                     Logical Resource(s)
  -------------------------------------------------  -------------------
  OLOGIC_X2Y187.OQ     Tockq                 0.406   OutD_7
                                                     OutD_7
  D4.O                 net (fanout=1)        0.002   OutD_7
  D4.PAD               Tioop                 2.997   OutD<7>
                                                     OutD_7_OBUF
                                                     OutD<7>
  -------------------------------------------------  ---------------------------
  Total                                      3.405ns (3.403ns logic, 0.002ns route)
                                                     (99.9% logic, 0.1% route)
```

Dual-Data Rate Example

A dual-data rate example of the OFFSET OUT constraint has the initial clock edge at 0 ns and half the PERIOD constraint, which correlates to the two edges of the clock. The timing report will display the clock arrival time for each edge of the clock. Since the data is being clocked in on both edges of the clock, the clock arrival time for the falling edge needs to be managed. The timing analysis tools do not automatically adjust any of the clock phases during analysis, so the constraints must be manually adjusted. The timing analysis tools offer two options to manage the falling edge clock arrival time. The resulting timing report displays the data path, the clock path, and the clock arrival time (shown in bold). An example timing report is shown below.

The first option is to create two time groups, one for rising edge synchronous elements and the second for the falling edge synchronous elements. Then create an OFFSET OUT constraint for each time group, the second OFFSET OUT constraint will have a different requirement. The falling edge OFFSET OUT constraint requirement should

be the "original requirement" plus half the PERIOD constraint. So, if you have the original requirement as 3 ns with a PERIOD of 10, the falling edge OFFSET OUT constraint requirement is 8 ns. This will compensate for the clock arrival time associated with the falling edge synchronous elements.

The second option is to create one time group and one corresponding OFFSET OUT constraint with the original constraint requirement. The only addition is the LOW keyword (if the PERIOD constraint has the HIGH keyword). If the PERIOD constraint has the LOW keyword, then the OFFSET constraint has the LOW keyword. This option can only be used if the duty cycle on the clock is 50/50.

During the timing analysis, the difference between the rising and falling edges of the clock is subtracted from the falling-edge-data-path analysis, and that difference is added to the original requirement. In Figure 17, the OFFSET requirement is 3 ns.

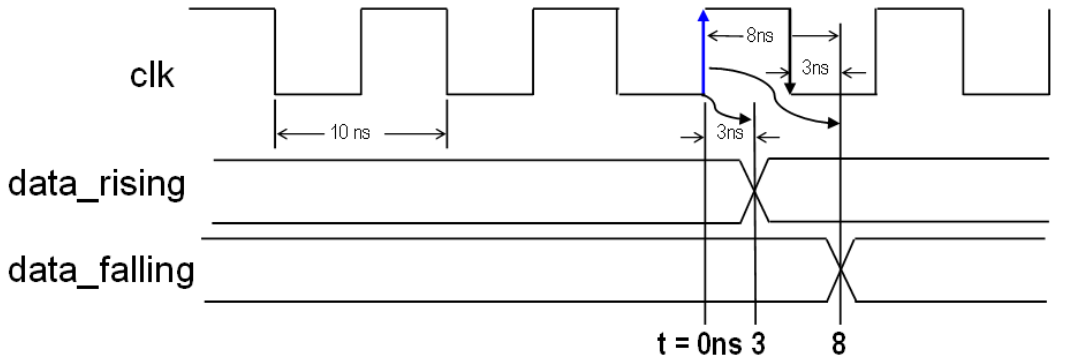


Figure 17: **Timing Diagram of Dual Data Rate in OFFSET OUT Constraint**

Timing Report Example of OFFSET = OUT 3 ns AFTER Clock

```
Slack:                  -0.783ns (requirement -(clock arrival + clock path + data path + uncertainty))
  Source:                 OutA_4 (FF)
  Destination:            OutA<4> (PAD)
  Source Clock:           clock0_ddr_bufg rising at 0.000ns
  Requirement:            3.000ns
  Data Path Delay:        3.372ns (Levels of Logic = 1)
  Clock Path Delay:       0.172ns (Levels of Logic = 3)
  Clock Uncertainty:      0.239ns

  Clock Path: clock0 to OutA_4
    Location              Delay type      Delay(ns)  Physical Resource
                                                     Logical Resource(s)
    ------------------------------------------------  -------------------
    E19.I                 Tiopi             0.768    clock0
                                                     clock0
                                                     MY_ddr_dcm/CLKIN_IBUFG_INST
```

```
    DCM_ADV_X0Y4.CLKIN   net (fanout=1)     0.982    MY_ddr_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y4.CLKFX   Tdmcko_CLKFX      -6.260    MY_ddr_dcm/DCM_ADV_INST
                                                     MY_ddr_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y19.I0    net (fanout=1)     1.487    MY_ddr_dcm/CLKFX_BUF
    BUFGCTRL_X0Y19.O     Tbgcko_O           0.700    MY_ddr_dcm/CLKFX_BUFG_INST
                                                     MY_ddr_dcm/CLKFX_BUFG_INST
    OLOGIC_X2Y83.CLK     net (fanout=26)    2.495    clock0_ddr_bufg
    ------------------------------------------------  ---------------------------
    Total                                   0.172ns (-4.792ns logic, 4.964ns route)

  Data Path: OutA_4 to OutA<4>
    Location             Delay type       Delay(ns)  Physical Resource
                                                     Logical Resource(s)
    ------------------------------------------------  -------------------
    OLOGIC_X2Y83.OQ      Tockq             0.406     OutA_4
                                                    OutA_4
    AG6.O                net (fanout=1)    0.002     OutA_4
    AG6.PAD              Tioop             2.964     OutA<4>
                                                     OutA_4_OBUF
                                                     OutA<4>
    ------------------------------------------------  ---------------------------
    Total                                   3.372ns (3.370ns logic, 0.002ns route)
                                                    (99.9% logic, 0.1% route)
```

Timing Report Example of OFFSET = OUT 8 ns AFTER Clock

```
Slack:                -0.783ns (requirement -(clock arrival + clock path + data path + uncertainty))
  Source:               OutA_4 (FF)
  Destination:          OutA<4> (PAD)
  Source Clock:         clock0_ddr_bufg falling at 5.000ns
  Requirement:          8.000ns
  Data Path Delay:      3.372ns (Levels of Logic = 1)
  Clock Path Delay:     0.172ns (Levels of Logic = 3)
  Clock Uncertainty:    0.239ns

  Clock Path: clock0 to OutA_4
    Location             Delay type       Delay(ns)  Physical Resource
                                                     Logical Resource(s)
    ------------------------------------------------  -------------------
    E19.I                Tiopi              0.768    clock0
                                                     clock0
                                                     MY_ddr_dcm/CLKIN_IBUFG_INST
    DCM_ADV_X0Y4.CLKIN   net (fanout=1)     0.982    MY_ddr_dcm/CLKIN_IBUFG_OUT
    DCM_ADV_X0Y4.CLKFX   Tdmcko_CLKFX      -6.260    MY_ddr_dcm/DCM_ADV_INST
                                                     MY_ddr_dcm/DCM_ADV_INST
    BUFGCTRL_X0Y19.I0    net (fanout=1)     1.487    MY_ddr_dcm/CLKFX_BUF
    BUFGCTRL_X0Y19.O     Tbgcko_O           0.700    MY_ddr_dcm/CLKFX_BUFG_INST
```

```
                                                    MY_ddr_dcm/CLKFX_BUFG_INST
  OLOGIC_X2Y83.CLK     net (fanout=26)     2.495    clock0_ddr_bufg
  ------------------------------------------------  --------------------------
  Total                                     0.172ns (-4.792ns logic, 4.964ns route)

Data Path: OutA_4 to OutA<4>
  Location             Delay type       Delay(ns)  Physical Resource
                                                    Logical Resource(s)
  ------------------------------------------------  -------------------
  OLOGIC_X2Y83.OQ      Tockq             0.406     OutA_4
                                                    OutA_4
  AG6.O                net (fanout=1)    0.002     OutA_4
  AG6.PAD              Tioop             2.964     OutA<4>
                                                    OutA_4_OBUF
                                                    OutA<4>
  ------------------------------------------------  --------------------------
  Total                                     3.372ns (3.370ns logic, 0.002ns route)
                                                    (99.9% logic, 0.1% route)
```

OFFSET OUT BEFORE

The OFFSET OUT BEFORE constraint defines the time used by the data external to the FPGA. OFFSET subtracts this time from the clock PERIOD to determine the time available for the data to propagate from the synchronous element to the pad. You can visualize this time as the data leaving the edge of the device before the next clock edge arrives at the edge of the device. This "OFFSET = OUT 2 ns BEFORE clock_pad" constraint reads that the data to be registered in the downstream device is available on the FPGA's output pad, some time period, BEFORE the clock pulse is recognized by the downstream device. To adhere to the OFFSET constraint syntax, assume no skew on CLK between the devices (see Figure 3). The following equation defines this relationship:

TQ + TClock2Out + TClock <= TPeriod – Toffset_OUT_BEFORE

The analysis of the OFFSET OUT constraint involves ensuring that the maximum delay along the reference path (CLK_SYS to COMP) and the maximum delay along the data path (COMP to Q_OUT) do not exceed the clock period minus the specified offset.

A PERIOD or FREQUENCY is required for OFFSET OUT constraints with the BEFORE keyword.

OFFSET Constraint Syntax

This syntax is simple and easy to understand. For more information, refer to the Constraints Guide in the OFFSET constraints section.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/27/2006	1.0	Initial Xilinx release.