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AccelDSP IP Explorer

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Developing DSP algorithms for silicon requires careful selection of IP blocks and their macro-architecture specifications in the context of the target application. AccelDSP™ Synthesis Tool with IP-Explorer technology eliminates the trial-and-error from using IP blocks by allowing the tool automatically to select from various macro-architectures depending on unique design and system requirements.

Introduction

Developing DSP algorithms for silicon requires careful selection of IP blocks and their macro-architecture specifications in the context of the target application. For example, there are three commonly used methods to implement basic trigonometric functions in hardware including:

1. Bipartite Tables
2. Linearly Interpolated LUT
3. CORDIC

Each has a specific hardware advantage depending on the design context. Bipartite tables are a good choice when the input values require relatively small word lengths, while linearly interpolated Lookup Tables (LUT) are a better choice for slightly larger input word lengths. The CORDIC algorithm is optimal for applications that require large word lengths for the inputs when performance is not a consideration. When performance is a consideration the CORDIC algorithm can be implemented using parallelism and pipeline stages.

The graph in Figure 1 compares the area of these methods over a range of input word lengths.

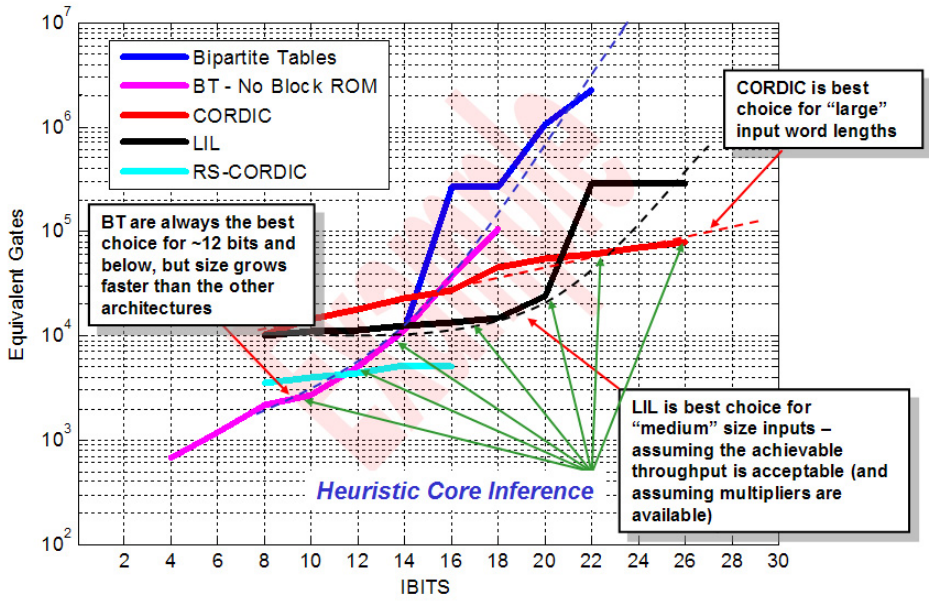

Figure 1: **Area vs. Input Word Length**

Knowing how to build and when to use each of these cores is a complex task, but necessary to achieve an optimal hardware solution.

IP Explorer Technology

AccelDSP Synthesis Tool with IP-Explorer technology eliminates the trial-and-error process from using IP blocks by allowing the tool to select from various macro-architectures depending on the unique design and system requirements. AccelWare™ DSP IP Toolkits provide a set of IP generators that produce architecture specific synthesizable MATLAB for common built-in functions, such as sine, cosine, log, and divide. These hardware architectures, developed by a team of DSP hardware design

experts, are characterized, in terms of their area and performance, for each supported FPGA technology using over 6000 designs.

During the DSP Synthesis process IP Explorer analyzes each use of these functions, against the overall system area and performance requirements, to determine its unique optimal hardware solution. Once determined, the appropriate IP core is automatically inserted into the design (Figure 2).

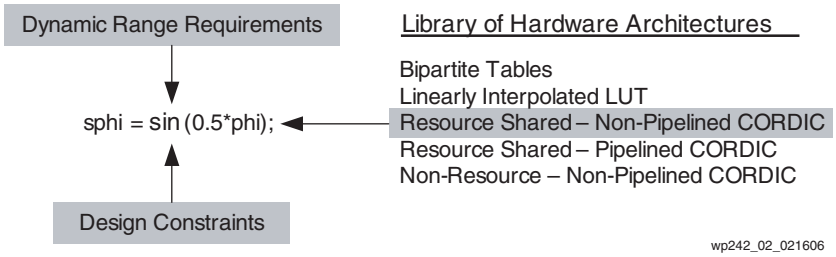

Figure 2: **Design Context-Based Automatic IP Insertion**

Designing at a Higher Level

IP Explorer raises the abstraction level of DSP hardware design significantly closer to that of DSP algorithm development. Basic MATLAB language primitives form the foundation of this abstraction pyramid by providing the ability to model any function or algorithm at a low level. AccelDSP IP Explorer elevates this abstraction level significantly by providing the ability to target the MATLAB standard library of pre-configured DSP building blocks and functions directly into hardware (Figure 3).

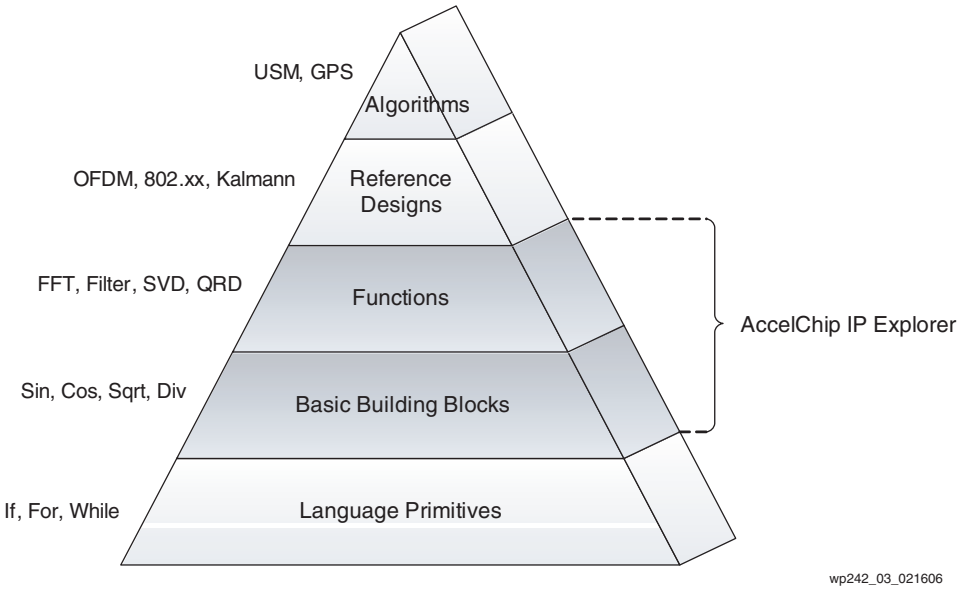

Figure 3: **DSP Design Abstraction Pyramid**

Design Example

To illustrate the effect that IP Explorer has on a design, consider the following example of a Euler to Quaternion angle conversion algorithm that performs a sine and cosine operation on three input angles. In this example, each input has a word length of 12 bits (Figure 4).

```
function [q]= euler2quat(phi,theta,psi)

sphi = sin(0.5*phi);
cphi = cos(0.5*phi);
stheta = sin(0.5*theta);
ctheta = cos(0.5*theta);
spsi = sin(0.5*psi);
cpsi = cos(0.5*psi);

q(1) =sphi*stheta*spsi+cphi*ctheta*cpsi;
q(2) =sphi*ctheta*cpsi-cphi*stheta*spsi;
q(3) =cphi*stheta*cpsi+sphi*ctheta*spsi;
q(4) =cphi*ctheta*spsi-sphi*stheta*cpsi;
```

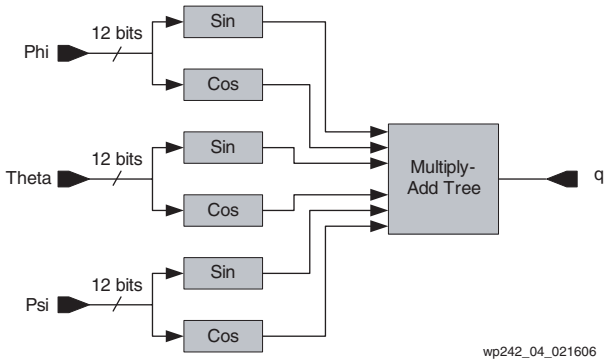

Figure 4: **Euler-to-Quaternion Angle Converter Block Diagram**

Let's compare a typical approach which is to design a single implementation of the trig function, based on the CORDIC method and instantiate it multiple times vs. IP Explorer. Table 1 shows the area and performance results for both approaches:

Table 1: **Comparison of Area and Performance Results**

Sin/Cosine Architecture	Area (LUTs)	Performance
Six CORDIC architectures	2670	8.4 MSPS
Selected by IP Explorer	1287	100 MSPS

IP Explorer selected a bipartite table approach because the input bit widths were reasonably small and to leverage the built-in DSP blocks of the targeted FPGA device. This would not have been the optimal choice for an ASIC. Not only has the task of designing hardware for the sine and cosine functions been eliminated, but a 33 percent area savings and 12X performance advantages have been realized.

Summary

IP Explorer represents a truly unique advancement in the development of DSP hardware. By providing a seamless path to hardware for the key DSP building blocks, hardware design has moved significantly closer to the abstraction level enjoyed by algorithm developers using MATLAB.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/19/06	1.0	Initial Xilinx release.