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# Xilinx Tailors Four Tool Flows to Customer Design Disciplines in ISE Design Suite 11.1

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With the introduction of the Xilinx® ISE® Design Suite 11.1, Xilinx is taking a bold new step to refine design methodologies and better serve the diverse skill sets of customers creating innovations with Xilinx FPGA targeted design platforms. With ISE Design Suite 11.1, Xilinx is concurrently launching four new tool flow offerings specifically tailored to the needs of logic designers, embedded developers, DSP algorithm developers, and system integrators.

Traditionally, Xilinx customers have been logic designers—typically electrical engineers well-versed in hardware design and hardware description languages (HDLs). However, over the last eight years, as each generation of Virtex® and Spartan® FPGAs have provided exponential increases in logic cells and hard and soft embedded processors (MPUs as well as DSPs), Xilinx has seen a rapid increase in embedded software/hardware engineers, DSP algorithm developers, and systems integrators using our devices to create advanced systems on chip. That is, not only are multi-disciplinary design teams using our devices; in many cases, individuals who have little or no knowledge of HDL-based design are today implementing their system designs in Xilinx FPGAs.

Prior to the ISE Design Suite 11.1 release, Xilinx offered *all* of our customers a smorgasbord of tools and IP. Each customer picked from the suite they felt they needed to program an FPGA. However, if a customer was unfamiliar with logic/connectivity design, it might not have been clear which of the many offerings to select and use. For example, customers who were not familiar with hardware debug might not have known about the benefits of the ChipScope™ Pro analyzer, which automates the debugging task —saving users a tremendous amount of design pain.

To help designers in each of these groups design more efficiently in a familiar, customizable environment, Xilinx is now offering four new configurations of the ISE Design Suite: Logic Edition, Embedded Edition, DSP Edition, and System Edition (see Figure 1).

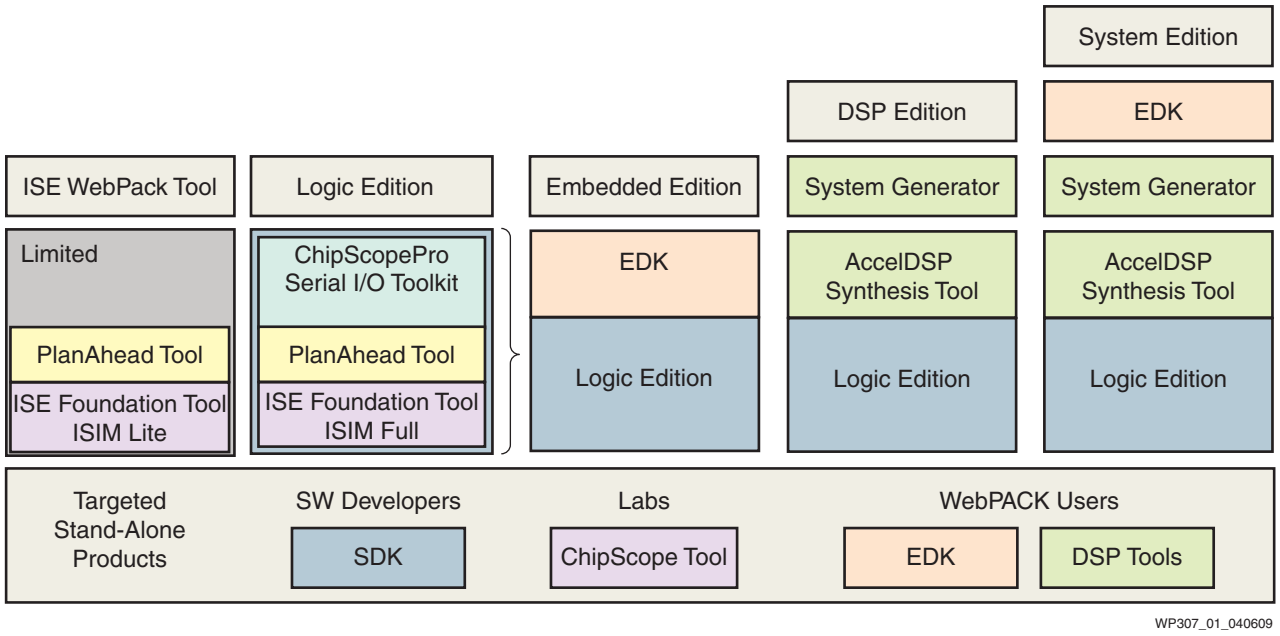


*Figure 1:* **New Tool Flows**

Xilinx performed a rigorous study with customers from each discipline to examine their design methodologies and see which tools, from Xilinx and third parties, these customers used to successfully implement their designs in Xilinx FPGAs.

From this research, the software design group at Xilinx created the four new configurations of the ISE Design Suite. These configurations help experienced customers optimize their tool purchases. They also help those who are new to designing with FPGAs to easily identify which tools can best suit their design needs. Each edition comes complete with the design creation, verification and implementation tools, and IP needed for a specific discipline.

Each of these new editions is customizable, so users can add other tools from Xilinx or third parties to these design flows if they choose. Xilinx is not dictating a user's flow, but establishing base flows that can be expanded and customized. Additionally, a design manager can select the right number and type of licenses that best suit the design team's needs and each design team member's skill set. For example, the new offerings allow the customer to add additional options, like the Xilinx Software Development Kit (SDK) for teams that have several SW developers writing code for a single FPGA instead of purchasing full Embedded Development Kits (EDK), as in the past.

This move to new ISE Design Suite editions is a key element to the Xilinx *targeted design platform* strategy, in which Xilinx is focused on providing the best FPGA silicon on the market, along with the best hardware- and software-design tools, IP, development boards, and support that customers need to be successful—allowing the customers to focus on the value-added parts of the design and getting innovations to market quickly. See WP306, *Introducing the Xilinx Targeted Design Platform: Fulfilling the Programmable Imperative*.

# The New ISE Design Suite Configurations

With the ISE Design Suite 11.1 release, Xilinx is offering four new configurations: Logic Edition, Embedded Edition, DSP Edition, and System Edition. Each flow includes tools as well as domain- and application-specific IP and reference designs.

In addition to offering the new ISE Design Suite configurations, Xilinx continues to offer ISE WebPACK™ software (a device-limited version of the Xilinx tool flow), SDK, the ChipScope Pro analyzer, EDK, and DSP (AccelDSP™ synthesis tool and System Generator for DSP) as stand-alone offerings that users can add to their flows.

# Logic Edition

The new Logic Edition is a complete flow for RTL-based design and includes features to improve runtime, memory usage, usability, power optimization, and accuracy—yielding up to a 10% dynamic power reduction, 28% better memory usage, and a 2x improvement in place and route compile times compared with the previous version.

Logic Edition serves as the foundation technology for each of the Xilinx designer edition flows, and as a stand-alone suite, it includes all the tools familiar to traditional Xilinx customers.

Logic Edition is composed of ISE Foundation™ software, PlanAhead™ design analysis tool, ChipScope Pro analyzer with the Serial I/O toolkit, ISE Simulator, and CORE Generator™ tool IP.

## Logic Edition: Create a Design

In the Logic Edition flow, users start a project by opening the ISE Project Navigator in ISE Foundation. From that tool, they can launch the CORE Generator interface and select the IP cores best suited to their design. They then use the HDL editor in the ISE Project Navigator to write an HDL representation of their design. The CORE Generator software includes hundreds of domain- and application-specific cores to allow users to quickly include pre-designed functions into their designs so they can concentrate the bulk of their design effort on the value-added portions of their design. In the ISE Design Suite 11.1 tools, Xilinx added new IP for the video

market and versioning data for all Xilinx cores to allow users to monitor which cores are new and which ones Xilinx is phasing out.

Designers can then use the Xilinx Memory Interface Generator (MIG) tool in the ISE Design Suite software to generate memory controllers and interfaces for Xilinx FPGAs. The MIG tool generates unencrypted Verilog or VHDL design files, UCF constraints, simulation files, and implementation script files to simplify the design process. In the last release of ISE Design Suite software, MIG users had to be aware of the placement, routing, and timing constraints when making pin assignment changes to memory blocks. In ISE Design Suite 11.1, Xilinx improved the tools: the place and route engine automatically implements the design (the user no longer needs to manually change the placement and routing constraints) when there are pin assignment changes to a memory interface. In addition, users get predictable timing for the PCIe® interface cores when integrated into the design. The tool currently supports DDR3 SDRAM, DDR2 SDRAM, DDR SDRAM, QDRII SRAM, and DDRII SRAM, and RLDRAM II.

After users select their blocks and create an HDL representation of their design, they can synthesize their design, perform floorplanning, and proactively perform pin assignment.

For logic synthesis, ISE Design Suite software includes the built-in XST synthesis engine. In ISE Design Suite 11.1, XST synthesis runs 1.6 times faster on average than the previous version.

All ISE software edition bundles, including the ISE WebPACK tool come with complete versions of PlanAhead software for no additional cost. The PlanAhead tool is a full-featured design analysis cockpit, providing critical features for advanced FPGA implementation management, such as I/O pin assignment, floorplanning, design analysis, and implementation. The PlanAhead tool is now invoked from within Project Navigator for pin planning and floorplanning processes as well as a stand-alone executable for advanced implementation and debug features.

In ISE Design Suite 11.1, users have access to the ChipScope Pro debugging tool core insertion features from within the PlanAhead tool, which includes a new wizard feature that allows users to easily insert test monitor logic throughout their designs that will allow them to more easily monitor signals and find errors using the ChipScope Pro tool later in the process.

Designers can use the PlanAhead software pin layout capability to perform pin assignment and then send the pin placement to their PCB designers to get an early start on PCB development.

Logic Edition users can also use the TimeAhead feature in the PlanAhead software at all phases of the design process to obtain real-time place and route estimates of how a given floorplan arrangement will affect their timing budget. After the users derive a rough floorplan, they can use the implementation run feature. This feature drives the ISE software's place and route engine to create an implementation (or several variant implementations) of the user’s design to try various layout schemes and ultimately derive the most efficient layout in terms of cell utilization, power conservation, and design performance. In their layout, the users can then locate areas that create timing violations, move functions and blocks around to optimize their design, fix the timing problems, and quickly re-run implementations to compare results.

## Logic Edition: Verify the Design with ISE Design Suite

Logic Edition also includes a broad set of analysis and test tools to help users verify the functionality, timing, and power consumption of their designs.

For logic simulation, Logic Edition includes the ISim simulator. Mentor Graphics ModelSim Xilinx Edition (MXE-III), Cadence NCSim, and Synopsys VCS simulators can also be used. In the ISE 11.1 software, ISim runs two times faster than the previous version of ISim, 10.1 (service pack 3). The Logic Edition of ISE software also includes the faster SecureIP simulation models to model the dedicated blocks. ISim also now includes an oscilloscope-like waveform viewer and navigation, the ability to write Switching Activity Interchange Format (SAIF) for power estimation in Xilinx XPower tools, and the ability to import and export user waveform settings.

For power analysis, Logic Edition includes the XPower Estimator and Analyzer tools. Users first outline the power consumption goals of their designs by completing the XPower Estimator's spreadsheet with data on frequency, device utilization, and I/O types. After they have placed and routed their designs, the users can have their simulator generate a VCD files and use the XPower Analyzer to ensure their designs are meeting their power goals.

In Logic Edition, the ChipScope Pro tool, allows users to insert a logic analyzer, bus analyzers, and virtual I/O low-profile software cores directly into their designs. Once the user inserts the analyzer IP, any internal signal or node can be viewed, including embedded or soft processors, in a manner similar to an external oscilloscope.

ISE 11.1 software also includes the ChipScope Pro Serial I/O Toolkit as a standard feature in all ISE Design Suite Editions. The tool allows users to setup and debug Virtex-4 FX, Virtex-5 LXT, Virtex-5 SXT, Virtex-5 FXT, and Virtex-5 TXT FPGA serial I/O channels, measure bit-error ratios on multiple channels, adjust high-speed serial transceiver parameters in real-time while serial I/O channels are interacting with the rest of the system. The tool also includes a built-in pattern generator and pattern receiver with all the standard serial I/O data packets.

## Logic Edition: Implement the Design with ISE Design Suite

Logic Edition also includes improved placement and routing engines.

Xilinx has added a new built-in activity estimation engine to the implementation tool flow, which automatically identifies power hungry blocks during the implementation phase of the design. After identifying power hungry blocks, the tool performs a re-synthesis in which it recompiles the logic in those blocks to reduce the number of switching elements in the blocks.

Xilinx also added new power optimization features to the placement and routing engines in ISE software. The ISE 11.1 software placer now includes a new clock gating feature, which, with the user's guidance, uses a global clock buffer to replace high fanout register clock enables. The feature in turn reduces routing capacitance and minimizes wire length, which reduces the device's overall dynamic power consumption by up to 10%.

In addition to the power savings features, ISE 11.1 software's place and route engines run 2X faster than the 10.1 release while the incremental implementation engines in SmartGuide provide up to a 2X additional runtime advantage. In addition, Xilinx added multi-threaded placement support for the Linux version of the place and route engines to take advantage of multi-core processor workstations so users can further speed up place and route run times.

Xilinx also upgraded SmartXplorer in ISE 11.1 software so that it now supports compute farm systems to allow designers to perform multiple implementation runs across a network of computing hosts. SmartXplorer supports submission to load sharing facility (LSF) and Sun Grid Engine (SGE) distributed computing farms. PlanAhead software also supports submission of implementation runs to multiple Linux hosts for parallel execution.

# Embedded Edition

In the new Embedded Edition, Xilinx bundles its popular Embedded Developers Kit (EDK) with Logic Edition (Figure 2). Embedded Edition targets customers who want to utilize the flexibility of an embedded processor in their design. Xilinx offers two processor options for optimal design flexibility: the soft MicroBlaze™ processor 32-bit core and the PowerPC®440 embedded processor core. In addition, Embedded Edition supplies the necessary drivers, software applications, and debug capabilities that embedded systems designers are accustomed to. Also new in ISE Design Suite 11.1 software, in response to customer requests, Xilinx is offering the Software Development Kit (SDK) portion of EDK in a stand-alone licensing configuration at a reduced price for software focused designers.

Embedded Edition software highlights include:

- SDK, a stand-alone configuration for users focused on embedded software application development and debug that simplifies the user interface and provides a considerably smaller disk footprint as compared to previous versions of EDK.
- Dual processor design creation automation using Base System Builder (BSB).
- A new version of the MicroBlaze processor (7.20) that offers greater optimization when designing with Xilinx targeted design platforms.

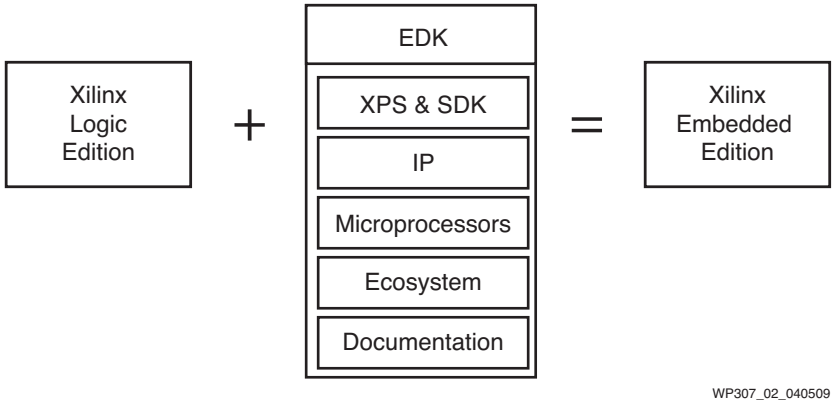


*Figure 2:* **Embedded Edition**

## Using EDK in Embedded Edition to Program Processors

The EDK is composed of the Xilinx Platform Studio (XPS) and SDK tools, embedded IP, microprocessor cores, documentation, and interfaces to third parties such as Wind River and Monta Vista.

In the Embedded Edition flow, users first create and enter the RTL of their designs into Project Navigator. When they want to add microprocessor cores to their design (either MicroBlaze soft processors or the embedded PowerPC processors in Virtex-4 and Virtex-5 devices), they activate the XPS tool.

XPS includes a sophisticated wizard utility, BSB, that allows users, through a series of mouse-clicks, to select which microprocessor (up to two) they want in their design. They can easily select their desired peripheral set and design topology. The BSB then automatically generates a complete working embedded system, including both the hardware and software platforms that can be easily implemented using XPS. The tool then automatically implements them. The previous version of BSB only allowed users to implement a single processor and its peripherals at a time. The version of BSB in ISE Design Suite 11.1 software allows users to implement single or dual processor designs, including their associated peripherals.

In greater depth, BSB takes users through several windows in which, through a series of mouse clicks, users specify the development board they are using. Users can then choose to implement a single or dual processor architecture in their design. They can specify if they want the processors to use their FPUs, the targeted processor and bus performance, and the memory allocation/requirements (which in some cases requires extra FPGA resources) for each processor. The users can then select which MPU peripherals they would like to add to each processor and specify if they want a given peripheral dedicated to a single processor or shared by both processors. Once they specify all those features, they can then view, augment, and implement the design in XPS as desired. XPS provides detailed control of connectivity, meaning various views of the design including a block diagram and system assembly view. XPS allows users to conduct detailed analysis and hand tailoring of blocks in their design. When they are satisfied with their design, they can have XPS automatically implement their design (XPS will automatically run the ISE tools in the background). XPS also automatically includes necessary drivers for all the hardware components of the design.

A new feature in Platform Studio allows users to export their design in an XML file for SDK. The XML file contains a description of the hardware, memory map, and peripherals in the design, and the data sheets for all the hardware peripherals.

When users import this XML file into SDK, the design comes up in an industry-standard Eclipse-based software development environment (not in a hardware-design-centric GUI), which most software developers are familiar with and use today for developing application software.

Using SDK, users also define what OS they are going to use from a pull-down menu. The tool then compiles the OS, along with the drivers for the design's hardware peripherals. Users can then launch a software project in the tool, create software applications, perform software debug, profile, and download application code to the processor(s). SDK also includes a series of test applications—among the many are Dhrystone, several memory and peripheral tests, and Xilkernel demo scheduler.

Platform Studio has been enhanced to offer revision tracking with this release. This provides designers with the capability to incrementally change their design with the assurance that they can go back to previous versions if necessary.

# DSP Edition

The new DSP Edition is composed of the Xilinx DSP bundle (System Generator development environment and AccelDSP synthesis tool) on top of the Xilinx Logic Edition. See Figure 3.

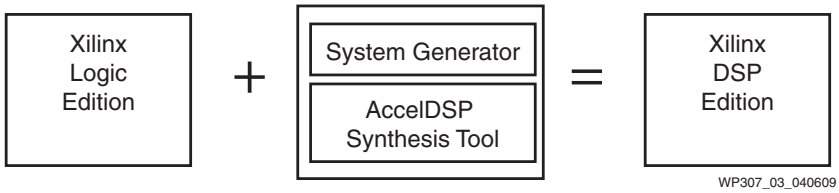


*Figure 3:* **DSP Edition**

DSP Edition is targeted at algorithm developers who want to implement their complex algorithms in Xilinx FPGAs. Since the flow is highly automated, users do not need to be familiar with HDLs.

In the flow, algorithm developers first create their algorithms and behavioral models of those algorithms in the MATLAB® software environment from The MathWorks. They then test those behavioral models in the MathWorks' Simulink® product, tweaking the algorithm with iterations between MATLAB and Simulink software until their algorithm is behaving as expected. Once it is, they can use the Xilinx DSP Edition to optimize and implement their algorithms in a Xilinx FPGA.

From DSP Edition, algorithm developers use System Generator to replace the behavioral blocks that make up all, most, or some of the algorithm. These blocks contain optimized IP from the Xilinx CORE Generator library, or the users can replace all or some of the blocks with their own HDL, using a custom black box. If they have created a custom algorithm in MATLAB software but do not have a VHDL representation of the algorithm, the algorithm developers can use the AccelDSP synthesis tool to automatically synthesize that custom algorithm into VHDL and also create a new System Generator block. That block can then be placed with the other blocks in their System Generator design. After all the algorithm blocks are populated in System Generator, the users can push a button and System Generator automatically runs the ISE software place and route tools beneath the hood and implements the hardware representation of the algorithm in the FPGA. Thus, in a matter of minutes, algorithm developers can implement their algorithm in a Xilinx FPGA to see how it runs in real hardware.

DSP Edition links with Simulink software. This allows the algorithm developers to re-use the testbench developed to test their algorithm in the Simulink and MATLAB environments, which ensures the version of the hardware algorithm and software algorithm behave the same. Algorithm developers can also use the combination of DSP Edition and Simulink and MATLAB software to perform co-simulation while they troubleshoot and tweak their algorithms for optimal performance and functionality. For example, if in the development process, algorithm developers discover one of their many behavioral blocks needs to be adjusted, they can run their known good blocks in the FPGA to speed up verification as they iterate between tweaking and testing the troublesome block. The hardware co-simulation runs up to 1,000 times faster than the pure software based simulation; the more complex the algorithm, the greater the speed up in hardware vs. software.

In ISE Design Suite 11.1 software, the System Generator tool runs on Linux in addition to Microsoft Windows.

## System Edition

System Edition includes every tool in the Xilinx arsenal and is targeted at designers and design teams who use every aspect of Xilinx devices. Where Embedded Edition

includes Logic Edition plus EDK, and DSP Edition includes Logic Edition plus the Xilinx DSP Bundle, System Edition includes Logic Edition plus EDK *and* the Xilinx DSP Bundle.

All the tools in the System Edition flow include the same ISE Design Suite 11.1 software updates described in previous sections and improved interoperability between the Logic, Embedded, and DSP tool flows.

# WebPACK Tool

In addition to introducing the new editions in the ISE Design Suite 11.1 software release, Xilinx also updated its free downloadable ISE WebPACK tool. Where the 10.1 release of ISE WebPACK included a limited version of PlanAhead, the ISE 11.1 WebPACK tool now includes all the utilities of the full version of PlanAhead (as described previously in Logic Edition) but supports a limited number of devices.

# Stand-Alone Tools

While Xilinx is now offering customers new configurations of ISE software tailored to their needs, some customers might want to purchase extra licenses of some of the tools in those flows. Therefore, in addition to offering Logic Edition, Embedded Edition, DSP Edition, and System Edition, customers can now separately license the SDK, ChipScope Pro analyzer, EDK tools, and Xilinx DSP Tools Bundle (which includes System Generator plus the AccelDSP synthesis tool) as stand-alone tools.

This SDK version includes just the embedded software tools and is targeted for design team members who want to focus on embedded applications development, profiling, and debugging. DSP Edition customers, who perhaps also want to do a bit of embedded software development for their designs, will find it useful too, and can leverage the new integration between System Generator and SDK available in ISE Design Suite 11.1 software. SDK as a stand-alone tool has a much smaller hard drive footprint since it does not include any of the FPGA logic implementation or simulation tools.

For example, if users want to add embedded applications development functionality to their design flow, they can buy EDK as a stand-alone tool. Similarly, if they want to add DSP algorithm development to their flow, they can license the Xilinx DSP Tools Bundle.

# ISE Design Suite Licensing

With the release of the ISE 11.1 Design Suite, Xilinx is releasing new licensing schemes for its tools. Prior to this release, Xilinx tool licensing was user based. That is, each user needed a license to use the tools, and a floating license was not offered for any of the tools.

Starting with ISE Design Suite 11.1 software, Xilinx now offers the tools in two configurations: node locked, in which a license is locked to a single computer, and floating, in which a license resides on a customer's network server. Node locked allows customers to download a license of any of the Xilinx tools to a particular workstation. Multiple users can use the Xilinx software running on that single workstation. The floating license allows users to download a single license to their server and have designers anywhere in the world use that license one at a time.

Xilinx is offering the stand-alone tools in node locked and floating configurations, as well. See Table 1.

*Table 1:* **Features of the New Tool Flow Offerings**

| Features | ISE WebPACK (Device Limited) | Logic Edition | Embedded Edition | DSP Edition | System Edition |
|---|---|---|---|---|---|
| ISE Foundation with ISE Simulator (ISim) | ✓ | ✓ | ✓ | ✓ | ✓ |
| PlanAhead Design and Analysis Tool | ✓ | ✓ | ✓ | ✓ | ✓ |
| ChipScope Pro and the ChipScope Pro Serial I/O Toolkit | | ✓ | ✓ | ✓ | ✓ |
| Embedded Development Kit (EDK) | | | ✓ | | ✓ |
| Software Development Kit (SDK) | | | ✓ | | ✓ |
| Xilinx DSP Bundle including System Generator for DSP and the AccelDSP Synthesis Tool | | | | ✓ | ✓ |

# Conclusion

To better serve the diverse skill sets of customers creating innovations with Xilinx FPGA targeted design platforms, Xilinx is taking a bold new step to refine design methodologies. ISE Design Suite 11.1 software offers four new tool flow offerings specifically tailored to the needs of logic designers, embedded developers, DSP algorithm developers, and system integrators.

# Revision History

The following table shows the revision history for this document:

| Date | Version | Description of Revisions |
|---|---|---|
| 04/27/09 | 1.0 | Initial Xilinx release. |

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