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ISE Design Suite 11.1: Creating the First User-Specific FPGA Design Environments

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The release of ISE® Design Suite 11.1 is an important milestone in the evolution of FPGA design environments at Xilinx because it marks the first appearance of a series of tool suites each uniquely assembled and configured to serve the needs and preferences of different designer profiles (personas). This fundamental shift in philosophy is part of a strategic initiative at Xilinx to create *targeted design platforms*—simpler, smarter, and more strategically viable design platforms for the creation of FPGA solutions in a variety of industries. Thus, before looking specifically into the new capabilities and benefits offered in this ISE release, it is important to understand the basic motivation behind the creation of targeted design platforms and their role in the definition and delivery of future technology releases from Xilinx.

The Targeted Design Platform - A Backdrop and Summary

The flexibility afforded by Xilinx FPGAs to design, implement, and modify on-chip, system-level hardware has never been more vital than in today's pressurized global environment, and never for a broader cross section of industries, companies, and engineers. Caught between two perpetually juxtaposed forces—mounting business challenges and evolving product requirements—Xilinx customers are finding it necessary to use the increased maneuverability provided by Xilinx FPGAs to circumvent obstacles that might otherwise lead to debilitating compromises, insufferable delays, escalating costs, and unacceptable risks. In short, the *programmable revolution* brought about by the invention of the FPGA over 25 years ago has today become a *programmable imperative*.

Developing more effective ways to help customers keep pace with the rapidly changing business and product requirements requires significant and on-going advances by Xilinx in two essential categories:

- Programmable silicon innovations at every process node that deliver industry-leading value for every key figure of merit against which FPGAs are measured: price, power, performance, density, features, and programmability.
- Simpler, smarter, and more market- and user-specific design platforms—what Xilinx calls *targeted design platforms*.

Xilinx targeted design platforms are integrated collections of silicon (FPGAs), tools, boards, IP, reference designs, and software that Xilinx has expressly and strategically assembled to target the requirements and preferences of the four primary user profiles in its customer base and selected growth markets for the customers' designs. Xilinx conceived the targeted design platform after working for nearly a decade to increase the viability and reception of its FPGAs within the embedded and DSP engineering communities.

Over that time, Xilinx and its substantial ecosystem community collaborated to amass the largest collection of tools, market-specific IP, reference designs, software training, and engineering support services available from any FPGA vendor. The challenge was to find a way to deliver the appropriate combination of these platform elements to a fundamentally diverse set of users. The creation of targeted design platforms simplifies this process (see Figure 1).

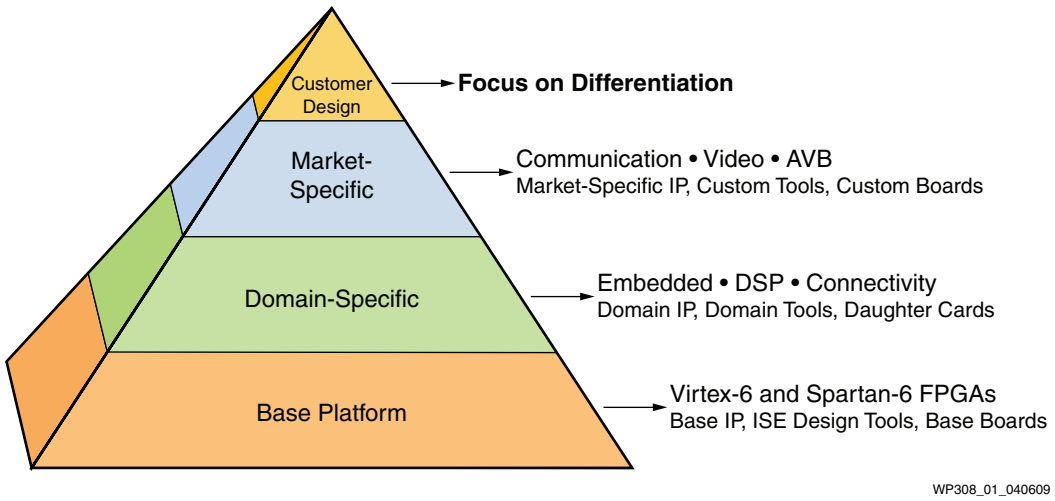

Figure 1: **Targeted Design Platforms**

Xilinx targeted design platforms enable customers to spend less time developing the infrastructure of an application and more time creating their unique value in the design. Platform elements that are broadly appropriate or necessary for all FPGA designers appear in the base platform for each new FPGA. Those elements that offer value to an engineer in a given domain only, i.e., logic/connectivity, embedded, DSP, or system designers, are delivered as domain-specific platforms.

Most of the IP and reference designs in the Xilinx repository are particular to a specific market (e.g., automotive, consumer, mil/aero, communications, AVB, and ISM) and are therefore best delivered in market-specific platforms, many of which are designed and implemented in collaboration with the Xilinx third-party ecosystem. In essence, targeted design platforms simplify the delivery of the right platform elements, to the right engineer, working in the right market. Equally important, they start the engineer much farther along in the development process, enabling more effort to be focused on creating differentiated value and less on preliminary or set-up design work.

For more information on targeted design platforms, see WP306, *Introducing the Xilinx Targeted Design Platform: Fulfilling the Programmable Imperative*.

Having thus established the context and motivation for the creation of targeted design platforms, a closer look can now be taken at the way in which ISE Design Suite 11.1 benefits from and contributes to the power of this innovative strategy.

New in ISE Design Suite 11.1

ISE Design Suite 11.1 is truly a next-generation advance in Xilinx FPGA design environments, architected from the ground up to fulfill three distinct but interrelated objectives:

- Improve designer productivity
- Reduce time to design completion
- Improve quality of results

Although the number of changes represented by this release are too numerous to cover exhaustively, a look at the more significant improvements illustrates the enormous benefits this tool suite delivers to Xilinx customers as they strive to fulfill the programmable imperative for themselves.

Greater Designer Productivity

Domain-specific targeted design platforms represent a significant breakthrough in productivity enhancement that will continue paying dividends for decades to come. Considering the breadth of capabilities that advanced programmable devices can deliver today, it is no longer feasible for one design flow or environment to fit every designer's needs. System designers, algorithm designers, software developers, and logic designers each represent a different user profile with unique requirements for a design methodology and associated design environment.

With the ISE Design Suite 11.1 release, this diverse set of designer profiles now has four domain-specific tool flows from which to choose: the Logic Edition, Embedded Edition, DSP Edition, and System Edition (see Figure 2).

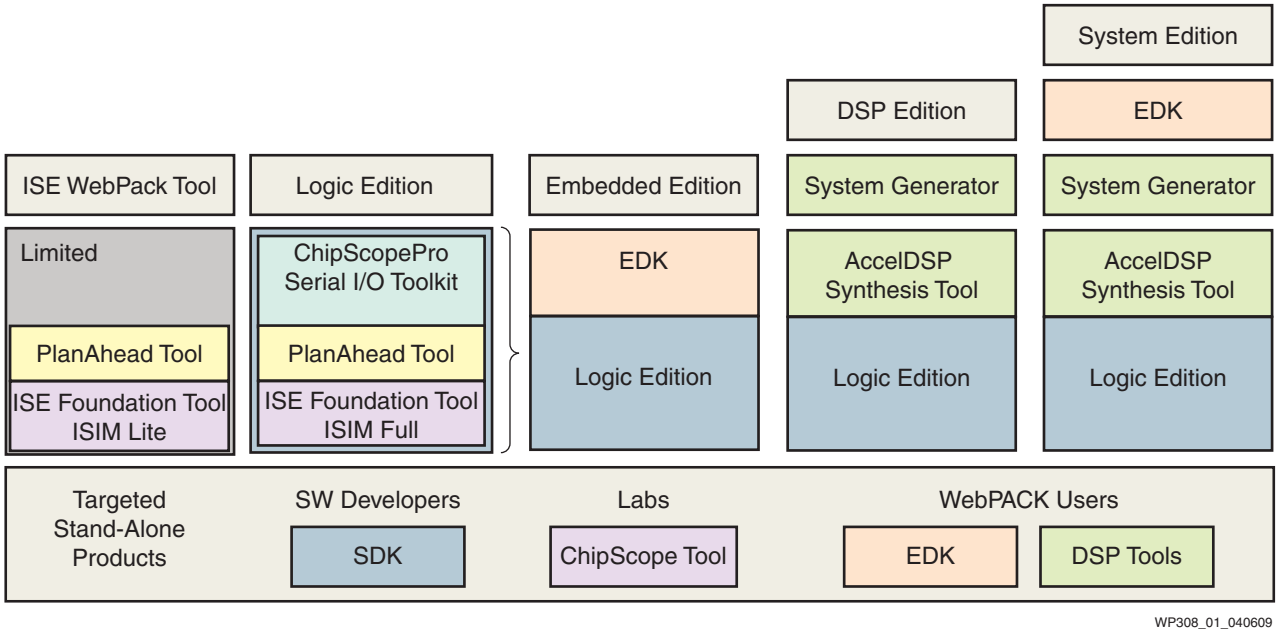

Figure 2: **ISE Design Suite 11.1 New Tool Flows**

In addition to the tool suite, each flow includes domain- and application-specific IP and reference designs. Xilinx will continue to offer customers its device-limited version of the Xilinx tool flow, the ISE WebPACK™ software. Customers can also purchase the Software Development Kit (SDK), ChipScope™ Pro analyzer, the Embedded Development Kit (EDK), and the Xilinx DSP Bundle, which includes AccelDSP™ synthesis tool and System Generator for DSP as stand-alone tools to add to their flows.

Other important changes that contribute to the enhanced productivity of ISE Design Suite 11.1 include:

- Improved interoperability between Project Navigator and System Generator for DSP, Platform Studio (EDK), and the CORE Generator™ system. These improvements include better handling of source and constraint files without specific interaction from the user, providing a more seamless design flow between base and domain specific tools.
- Greater integration between System Generator for DSP and SDK, the design environment for developing software for embedded processor(s), which enables algorithm developers to use the software development environment of SDK for the embedded portion of their design that runs on the embedded processor.
- The availability of the PlanAhead™ tool, now in all ISE Design Suite Editions, provides robust design analysis and floorplanning capabilities that enable designers to quickly analyze the design and the implementation results to uncover performance issues. This enables designers to easily apply floorplanning constraints to optimize design performance and to improve results consistency. The unique PlanAhead tool hierarchical capabilities enable designers to utilize block-based design techniques aimed at shortening design cycles, improving module level performance, and then maintaining that performance though subsequent iterations.

Faster Time to Design Completion

ISE Design Suite 11.1 optimizes each step within the design flow to deliver more implementation cycles (turns per day). Maximizing the number of turns per day is essential to reaching production more quickly. Here are highlights of some of the changes that provide the more dramatic benefits:

- Improvements in XST synthesis deliver an average of up to 2X faster compile times over ISE Design Suite 10.1.
- Support for multi-threaded place and route; SmartXplorer supports load sharing capabilities for farm systems (Load Sharing Facility and Sun Grid Engine).
- One-click insertion of ChipScope Pro tools using PlanAhead software allows users to insert ChipScope tool probe cores, using the rich graphical PlanAhead interface.
- Full access to PlanAhead software design and analysis tool simplifies pin planning for easy and early I/O assignment.
- A second-generation of SmartGuide™ technology allows users to limit re-implementation to only the effected areas for small design changes outside of the critical path. This exclusive Xilinx technology delivers the industry's fastest time for design iterations and greatly reduces design risk late in the process.
- Users can now create embedded designs with two embedded and/or soft core processors from within Base System Builder.
- Timing-driven place and route tools provide the most advanced technology to help customers meet their timing specifications more efficiently and more quickly. With support for physical synthesis optimizations, users can create a physically optimized design after synthesis that meets design performance goals in a single pass.
- SmartXplorer leverages distributed processing techniques to manage multiple implementation runs in an effort to achieve ideal design results. Through parallel efforts, SmartXplorer investigates the results of implementation runs to close in on optimal settings in far less time. SmartXplorer can be used to make better use of multiple compute platforms to more quickly achieve timing closure in a single platform environment. SmartXplorer, in combination with retiming in synthesis, helps designers improve performance by an average of 10%.
- Platform support has been expanded for System Generator for DSP with new support for Red Hat Enterprise Linux 4 WS (32 and 64 bit). Memory improvements deliver efficient compilation on standard platforms, with very large designs able to compile on mid-range workstations with 32-bit operating systems.
- System Generator is now integrated with XReports, and the AccelDSP synthesis tool has new reports to help designers improve their QoR more quickly.

Optimal Quality of Results

ISE Design Suite 11.1 provides tools and technologies to help users achieve optimal design results. With new access to the full PlanAhead design and analysis tool in all ISE Design Suite Editions, users have unparalleled visibility into their designs, enabling faster performance, greater device utilization, and higher design quality. Also, the improved EDK integration with the ISE software Project Navigator allows automatic handling of UCF information with Platform Studio. The improved interoperability of Project Navigator with EDK creates a more seamless development environment.

Additional areas where ISE Design Suite 11.1 provides improvements in quality of results include:

- Mapping from the AccelDSP synthesis tool to LogiCORE™ IP from the CORE Generator tool (when possible) during VHDL generation. This one change has produced dramatic improvements in F_{MAX}, greater than 2X.
- Logic re-synthesis that reduces the number of switching elements and clock gating in the placer for reduced power.
- Vector-less power estimation and estimation accuracy that simplify the process of developing an early and accurate power budget.
- Improved XST synthesis that provides better area utilization and faster performance.

Meeting Designers' Terms

Although the improvements to the ISE Design Suite are sufficiently numerous and beneficial by themselves, the real impact of these improvements is better understood when coupled with the power of targeted design platforms in practical applications. While the obvious benefit of user-targeted methodologies is that each user can develop market-specific applications in a domain-specific environment, the benefits associated with this capability become even more apparent and compelling in practice.

Consider for example the case where a team of four designers—one from each of the four domains, i.e., a logic designer, an embedded software engineer, a DSP designer, and a system architect, are all working on a video processing design. Coincidentally, along with all of the aforementioned improvements and changes, ISE Design Suite 11.1 includes a broad assortment of new and upgraded IP cores (see "Appendix A"), including a set of six new video and image processing functions:

- Defective Pixel Correction
- Color Filter Array Interpolation
- Color Correction Matrix
- Gamma Correction
- Color Space Converter
- Video Scalar

As is often the case, each designer on the team needs to use the same core in their design effort. The logic designer easily inserts the core into his design using the CORE Generator system and then develops the HDL code required to integrate the core into his design.

The DSP designer imports the same IP into System Generator for DSP. DSP designers can incorporate this IP core in an environment in which they are most comfortable and is best suited to their needs.

The system architect also uses the convenient CORE Generator system to access the Gamma Correction core. The CORE Generator tool generates a pcore that provides both the netlist for the core as well as the required documentation and driver files for the embedded software engineer. In the embedded methodology, this means that the hardware and software development efforts are now decoupled. The system architect can define how the pcore is connected to the embedded processor and provide that information to the embedded software engineer. This enables the embedded software engineer to begin his design and focus on how his software can add differentiation.

Summary

ISE Design Suite 11.1 introduces dramatic design environment changes that when combined with the inherent value of the targeted design platform, deliver unparalleled positive impact on designer productivity, time to design completion, and quality of design results.

Appendix A

The ISE Design Suite, with its four editions, provides the tools and IP needed for design creation, validation and implementation. Each edition also provides domain and market-specific IP to accelerate design completion. See Table 1 for examples of the IP available.

Table 1: **Tool Suite Information**

Tool Suite	Example Base Platform IP	Example Domain Specific Platform IP	Example Market Specific Platform IP
ISE Design Suite: Logic Edition • ISE Foundation™ with the ISE Design Suite Simulator • PlanAhead Design and Analysis Tool • ChipScope Pro and the ChipScope Pro Serial I/O Toolkit	Building Blocks • Memories and FIFOs • Arithmetic Operators (Adder, Accumulator, Multiplier, Complex Multiplier, etc.) Floating Point Operators	Connectivity • Standard bus interfaces such as PCI™ and PCI-X™ Networking Interfaces such as Ethernet, SPI-4.2, RapidIO, CAN, and PCI EXPRESS®	Automotive, Industrial, Scientific, and Medical • CAN, Ethernet AVB, FlexRay™, etc. • Image Processing Pipeline, Color Conversion Matrix, Color Filter Array Interpolation, etc.
	Debug and Verification • ChipScope Pro Integrated Controller • Integrated Logic Analyzer • Virtual Input/Output	DSP Functions • DDS Compiler, FIR Compiler, FFT, etc. Forward Error Correction IP such as Reed-Solomon Decoder and Encoder, Viterbi Decoder, etc.	Wired Telecommunications • Ten Gigabit Ethernet MAC, SPI-4.2, etc.
	FPGA Architecture Features • Clocking Wizard • Memory Interface Generator (MIG) • RocketIO™ Serial Transceivers • System Monitor Wizard		Wireless Telecommunications • 3GPP LTE Channel Encoder/Decoder, 3GPP Searcher, etc. • CPRI, OBSAI, and Serial Rapid IO

Table 1: **Tool Suite Information *(Cont'd)***

Tool Suite	Example Base Platform IP	Example Domain Specific Platform IP	Example Market Specific Platform IP
ISE Design Suite: DSP Edition • All tools, IP, and technologies in the ISE Design Suite: Logic Edition • System Generator for DSP • AccelDSP Synthesis Tool		DSP Functions • DDS Compiler, FIR Compiler, FFT, etc. Forward Error Correction IP such as Reed-Solomon Decoder and Encoder, Viterbi Decoder, etc.	Wireless Telecommunications Digital Up Converter, Digital Down Converter, etc.
ISE Design Suite: Embedded Edition • All tools, IP, and technologies in the ISE Design Suite: Logic Edition • Embedded Development Kit (EDK) with the Platform Studio • New "stand-alone" software development environment with Platform Studio SDK		Embedded Functions • MicroBlaze processor, Bus/Bridge IP: PLBv46, FSL, etc. • Peripheral IP: I2C controller, UART, USB2, Ethernet MAC, etc. • Memory Controllers: MultiPort, DDR2, etc.	Automotive, Industrial, Scientific, and Medical • CAN, Ethernet AVB, FlexRay, etc. Image Processing Pipeline, Color Conversion Matrix, Color Filter Array Interpolation, etc.

For a complete list of available IP, see xilinx.com/ipcenter.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
04/27/09	1.0	Initial Xilinx release.

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