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Jitter: Variations in the Significant Instants of a Clock or Data Signal

By: Austin Lesea

Jitter is a significant factor in the design of communications links. This white paper examines the causes of jitter and discusses some techniques of measuring jitter. It also provides methods of managing jitter in digital systems.

Introduction

The International Telecommunication Union (ITU) defines jitter as the variations in the significant instants of a clock or data signal. The term refers to phase variations with respect to a perfect reference that occur in a clock or data signal as a result of noise, patterns, or other causes with a frequency of variation greater than a few tens of Hertz. (Slower changes in phase due to temperature, voltage, and other physical changes are usually referred to as "wander.")

A more useful measure of jitter in a digital system is the period jitter. The period jitter is usually measured as the difference between the longest period and the shortest period. The period jitter is needed to ensure that there is adequate setup time for all of the signals.

Causes of Jitter

A perfect oscillator has rising edges occurring at precise moments in time that never vary. This is impossible in practice because even the best rubidium, cesium, or hydrogen maser oscillators are constructed from real electronics and have sources of noise and other imperfections.

A high-quality, low-phase-noise crystal oscillator has a jitter of less than 35 ps period jitter, accumulated over many millions of clock edges. This means that the maximum period and the minimum period of the oscillator vary by no more than the peak-to-peak value. Lower jitter values are extremely difficult to achieve. Thus, higher jitter values are quite common.

Jitter is caused by thermal noise, instabilities in the oscillator electronics, and external interference through power or ground, and even through the output connections disturbing the oscillator. Oscillators are influenced by external magnetic or electric fields by contributing to jitter in their output. RF interference from nearby transmitters also contributes to jitter. A simple amplifier, inverter, or buffer adds jitter to a signal.

Poor signal integrity (SI) engineering that results in transmission line reflections, cross-coupling (crosstalk), and ground or V_{CC} bounce add jitter to a signal. Inadequate bypass or decoupling can lead to increased jitter. Poor power supplies and unstable phase-locked loops (PLLs) are also common contributors to jitter in a system. Anything that can add noise to a signal or change the reference of an input buffer (such as ground bounce) adds jitter to the resulting signal.

Measurement of Jitter

Jitter represents the result of a statistical measurement process. As a consequence, the longer jitter is measured, the larger the measured value gets. At some point, the jitter stops increasing due to short-term variations, and the measurement continues to increase due to the physical changes that are always occurring. To make sensible measurements in a limited amount of time, instruments rely on predicting the result either by fitting a Gaussian distribution to the measurement or by stating a confidence level. Millions of edges might have to be measured to be sure of the result. If the jitter is too large, it can lead to an error in the logic, which might have dire consequences. These problems can occur only once per day and can be extremely difficult to find. Instrumentation has its own error, and to measure sub-nanosecond jitter, the instrument requires picosecond measurement resolution and accuracy.

Figure 1 shows the typical clock jitter measured at an IOB output. The variations in every clock period sampled are plotted as a histogram of the number of periods with a given length. The figure is taken from a LeCroy oscilloscope and shows a total peak-to-peak (maximum to minimum) jitter of 530 ps over the 899.895k sampled clocks.
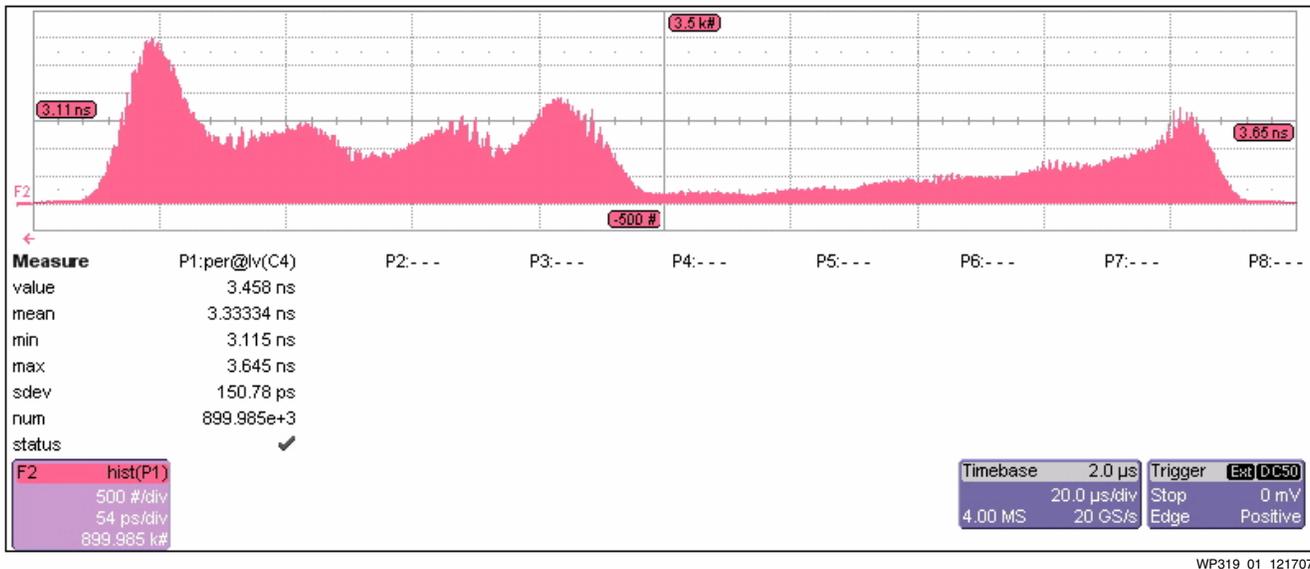

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Figure 1:   **Typical Clock Jitter Measured at an IOB Output**

There are three common types of jitter:

- *Period jitter* is defined as either the peak-to-peak, minimum and maximum, or average (RMS) of any and all periods measured, or as some combination of these three measures.

- *Cycle-to-cycle jitter* is defined as the peak-to-peak or average difference between adjacent cycles or periods.

- *ITU-T jitter* is defined as the worst-case peak-to-peak variation from any edge to a perfect reference in unit intervals (UI) where one UI is equal to the clock period. ITU-T jitter can exceed the value of a single period by many times because all of the edges can run too fast or too slow and the jitter can accumulate to a large value. For example, 10 UI for a 10 ns clock period over 10,000 clocks is a 100 ns variation from any edge to a perfect reference.

Period jitter is required to verify that timing constraints have been met. Cycle-to-cycle jitter is a variation of period jitter. ITU-T jitter is useful for predicting bit error rates on communications channels (wire, fiber, or radio).

Jitter is commonly characterized or measured by its peak-to-peak value, minimum and maximum values, RMS or one sigma value (a measure of power or energy), frequency spectrum, and by other statistical measures useful for determining the causes of jitter. Allen variance or time deviation is commonly used to help identify different physical causes of jitter.

Management of Jitter

PLLs are commonly used to remove jitter. If their loop gain and phase margin make them unstable, however, they can instead amplify jitter or add their own intrinsic jitter. Inadequate power supply rejection or coupling from other noise sources can also cause them to be sources of jitter.

A properly designed PLL can remove all objectionable jitter and provide a high-quality clock signal. Long loop time constants are necessary, resulting in increased wander and decreased jitter.

The basic rules of jitter management are:

• Start with the highest quality clock signal.

• Buffer that clock signal as few times as possible.

• Perform the necessary signal integrity engineering to assure a good match that is also low in crosstalk coupling.

• Bypass all devices as carefully as possible.

• Use ground and power planes without fail.

• Do not locate strong, fast outputs near the input nodes.

If an external cleanup PLL is required, perform the necessary Bode plot stability analysis to be certain that the PLL is a jitter attenuator, not a jitter amplifier.

Conclusion

In the past, with clock rates slower than 100 MHz, 200 ps of total peak-to-peak jitter from all sources was not even considered as part of the design. With clock periods of 2.0 ns (and shorter) possible in Virtex™-5 devices, even the most careful design might accumulate 10% of the period as jitter (200 ps) when all I/Os are switching, all logic is operating on the device, and all DCMs are in use.

Now that 10% of the period is lost to jitter, timing constraints must evaluate the critical path for constraints both 5% shorter and 5% longer than intended to verify the setup times of the design. Verification of jitter tolerance also has to be performed to ensure that the design is robust enough to operate with all of the expected variations in components, temperature, and voltage. To verify the timing margin, jitter should be added to the clock input until the design fails. The margin can then be verified to meet the system's specification. Jitter should be added through a sine wave modulation source and swept over the range of ~100 Hz to the clock frequency divided by 1000. Higher rates of jitter modulation might also be necessary. The jitter modulation frequency can be varied from the clock frequency divided by 1000 to the clock divided by 2. This range of possible test conditions can be used for a System Packet Interface Level 4 Phase 2 (SPI-4.2) Packet-Over SONET/SDH Level 4 (POS-PHY L4) design. Jitter is thus the next challenge to systems designers in the high-speed, ultra-deep-submicron world.

Additional Resources

The following sources can be consulted for more information about jitter measurement and analysis:

1. Trischitta, Patrick R., and Eve L. Varma. 1989. *Jitter in Digital Transmission Systems*: Artech House.

2. Takasaki, Yoshitaka. 1991. *Digital Transmission Design and Jitter Analysis*: Artech House.

3. Boulder Conferences: www.nist.gov/public_affairs/confpage/blconf.htm.

4. Wavecrest Corporation: www.wavecrest.com.

5. Tektronix Test and Measurement Equipment: www.tek.com.

6. Agilent Technologies: www.agilent.com.

7. LeCroy Oscilloscopes and Protocol Analyzers: www.lecroy.com.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/24/08	1.0	Initial Xilinx release. Based on a previously-published *Tech Xclusive* article by the same author.

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