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EasyPath-6 Technology: Fast, Simple, Risk-Free FPGA Cost Reduction

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Virtex®-6 FPGAs are the industry's leading platform for designing complex systems in the fields of wired and wireless communication, storage, computing, instrumentation, automotive, industrial, and medical. Virtex-6 FPGAs not only deliver the most attractive set of features and functionality and the fastest time to market advantage, they are also paired with EasyPath™-6 technology, the fastest path to cost reduction.

Introduction

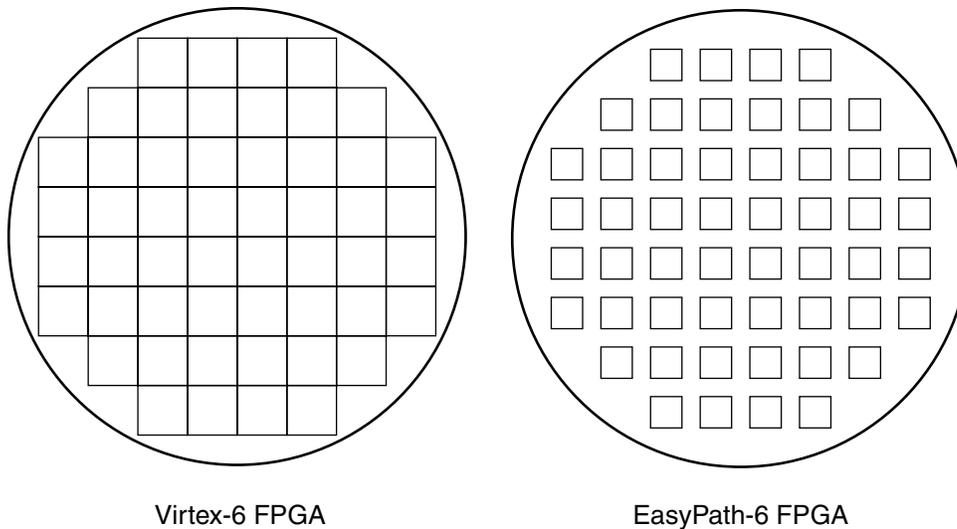
EasyPath-6 FPGAs are the industry's only design-specific FPGA solution to offer seamless cost reduction for complex platform FPGA designs. Unlike traditional approaches that require design conversion to structured ASICs or standard-cell ASICs, the EasyPath-6 technology cost reduction is automatic, immediate, and entirely risk-free.

The cost-reduced EasyPath-6 device is architecturally identical to the standard Virtex-6 FPGA in that it uses the same mask-set, process, and foundry. As a result, EasyPath-6 devices can offer, without any alterations, all complex functional blocks like serial transceivers, clock managers, block memory, distributed memory, and I/Os that support a multiplicity of standards as well as basic building blocks, including look-up tables, flip-flops, and the routing structure. The end result is cost-reduced silicon that matches all data sheet specifications and is identical in functionality and timing to the standard Virtex-6 FPGA.

Rapid Cost Reduction in Six Weeks

How does EasyPath-6 technology achieve cost savings in just six weeks without manufacturing new silicon? The simple answer is: through the reduction of effective die size. This technology is similar to gate arrays. In gate arrays, the base arrays have a lot of redundancy in terms of gates. Hence, the effective die size is determined by the total area of the used gates and the associated routing. Standard Virtex-6 FPGAs are designed with abundant routing and programmable multiplexers that connect the device's resources for unlimited programmability. The plentiful redundancy is necessary for achieving the flexibility associated with programmable logic. Design-specific testing of FPGA silicon unlocks the cost savings of this built-in redundancy.

[Figure 1](#) shows the number of FPGA die on a wafer versus the same wafer when tested with design-specific patterns, resulting in a smaller effective die size. [Figure 2](#) shows the yield gains due to die size reduction for a given defect density. While reduction of effective die size does not increase the number of gross die on a wafer, it increases the yield and hence delivers significant cost savings. [Figure 2](#) shows the yield improvement for die size reduction. The top-most curve is for the smallest die. The bottom-most curve is for the largest die.



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Figure 1: Smaller Effective Die Size with EasyPath-6 Technology

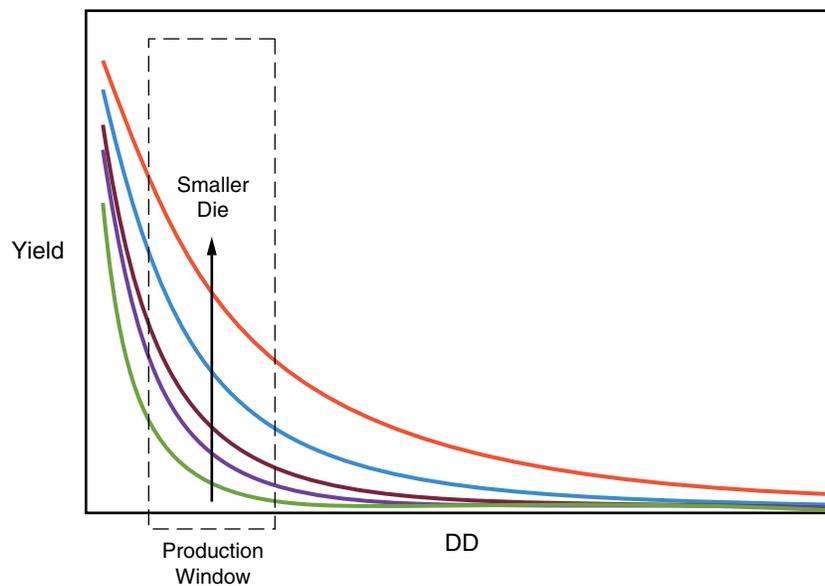


Figure 2: Yield Gains Due to Die Size Reduction

Delivering Lowest Total Cost

The benefits of delivering cost reduction without changing the silicon are far reaching. EasyPath-6 technology eliminates additional design constraints, additional engineering investment, and the cost and challenges of ensuring functionality and timing of the new silicon. Unlike a conversion into structured ASICs, there are no costs or challenges of re-qualification and re-certification. Most importantly, customers cite that the "opportunity cost" savings in using EasyPath-6 technology is the single biggest benefit because it enables them to deploy critical engineering resources on the next generation product rather than cost reduce the current generation of products.

Realizing cost savings with EasyPath-6 technology is simple. The designer can:

- Complete a Virtex-6 FPGA design without any ASIC constraints.
- Submit compiled design files for cost reduction.
- Receive cost reduced parts in six weeks—in production volumes.

EasyPath-6 Technology: Fast, Simple, and Risk-Free

EasyPath-6 technology improves the value proposition further by delivering cost savings in only six weeks. Unlike ASIC cost-reduction options, the cost-reduced EasyPath-6 devices are shipped in production volumes and not just prototypes. Consequently, customers using EasyPath-6 technology are able to respond to uncertain market forecasts in a rapid manner. The EasyPath-6 program also provides customers with the option to waive the minimum order quantity and thus customize their inventory to their end-market demands.

The Industry's Best FPGA Cost-Reduction Path

EasyPath-6 devices offer a truly innovative technology that leverages readily available redundancies in programmable FPGAs and delivers a cost-reduced solution—without introducing new silicon. EasyPath-6 device innovations continue to enable customers' success for years to come because the innovations continue to scale from one process node to another. In fact, EasyPath-6 technology continues to get more attractive as each generation of semiconductor devices pack more and more transistors.

Due to a combination of technology and market forces, programmable logic is increasingly more attractive for a large number of applications. While ASICs will always have their rightful place in the market, the combination of FPGA and EasyPath technologies provides an increasingly attractive solution for moderately high-volume applications.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
11/16/09	1.0	Initial Xilinx release.

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