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Xilinx DSP Design Platforms: Simplifying the Adoption of FPGAs for DSP

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With their inherent flexibility, FPGAs are ideal for high-performance or multi-channel digital signal processing (DSP) applications that can take advantage of hardware parallelism to achieve a single-chip solution—all at a lower cost and power consumption than multi-DSP implementations.

The transition to FPGA-based DSP hardware from DSP processors can involve acquiring a new set of design skills and a new understanding of hardware. For developers new to FPGAs or to DSP, this change can become a significant undertaking, which adds risk to design schedules. This white paper shows how the Spartan®-6 and Virtex®-6 FPGA DSP kits are designed to ease FPGA adoption and enable algorithm and hardware developers to quickly begin developing DSP applications on Xilinx® devices.

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Introduction

Xilinx FPGAs exceed the computational power of DSPs with their inherent parallelism, breaking the paradigm of sequential execution and accomplishing more per clock. Figure 1 shows why FPGAs are a popular choice for DSP hardware platforms when processing bandwidth requirements exceed 10 GMACs.

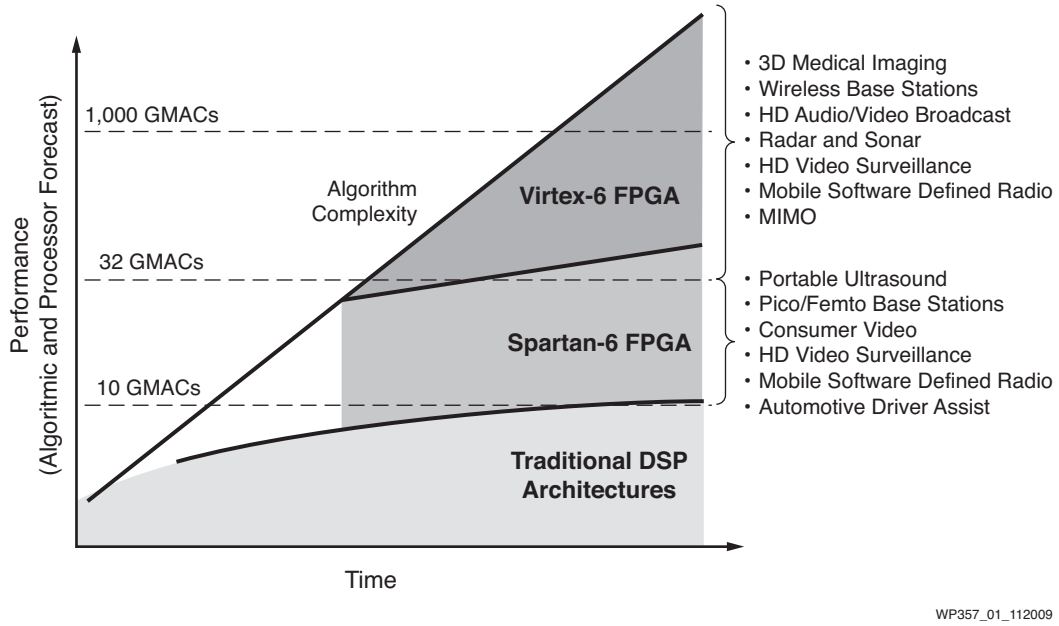

Figure 1: **The DSP Performance Gap**

Spartan-6 FPGA DSP Kit

At the core of the Spartan-6 FPGA DSP kit is the Avnet AES-S6DEV-SL150T-G development board, featuring the Spartan-6 LX150T device. This device is optimized with the right balance of connectivity, memory, and DSP hardware resources for DSP applications. The Spartan-6 LX150T FPGA is the largest Spartan-6 device and provides more than enough hardware resources for even the most demanding high-volume DSP applications. Highlights of this device include:

- 180 DSP48A1 slices
- 150K logic cells
- 266 block RAMs, 18 Kb each
- 8 low-power serial transceivers

The Spartan-6 FPGA DSP kit includes the following:

- Avnet AES-S6DEV-SL150T-G development board, featuring:
  - Dual FPGA mezzanine connector (FMC) slot
  - PCI Express® technology x1/x4
  - DDR3 SDRAM support
  - LCD panel interface
- One-year entitlement to the ISE® Design Suite: System Device Locked Edition
  - Includes System Generator for DSP and Embedded Development Kit (EDK)

- RTL and Simulink® software DSP reference designs
- Hardware setup guide
- Getting started guide with design tutorial
- Cables, power supply, and board documentation

Virtex-6 FPGA DSP Kit

The Virtex-6 FPGA DSP Kit features the Xilinx ML605 development board with the Virtex-6 LX240T device. This platform includes over 700 DSP48E1 slices that can deliver in excess of 400 GMACs of DSP processing bandwidth. This is the perfect development platform for high-performance wireless, aerospace, or defense applications. Highlights of the Virtex-6 LX240T device include:

- 769 DSP48E1 slices clocking at 600 MHz
- 241K logic cells
- 461 block RAMs, 32 Kb each
- 24 low-power serial transceivers

The Virtex-6 FPGA DSP kit includes the following:

- Xilinx ML605 development board, featuring:
  - Dual FMC slot
  - PCIe up to x4 Gen2
  - DDR3 SDRAM support
- One-year entitlement to the ISE Design Suite: System Device Locked Edition
  - Includes System Generator for DSP and EDK
- RTL and Simulink software DSP reference designs
- Hardware setup guide
- Getting started guide with design tutorial
- Cables, power supply, and board documentation

Targeted Reference Design for DSP

Each DSP kit comes with a targeted reference design for DSP that verifies the working hardware and provides a design example to demonstrate DSP design methodology. This design, tested by Xilinx for each kit release, is based on a Digital Up Converter (DUC)/Digital Down Converter (DDC) design, created using half-band finite impulse response (FIR) filters, a direct digital synthesis (DDS) block and a complex multiply operation. A block diagram of the DSP targeted reference design is shown in Figure 2.

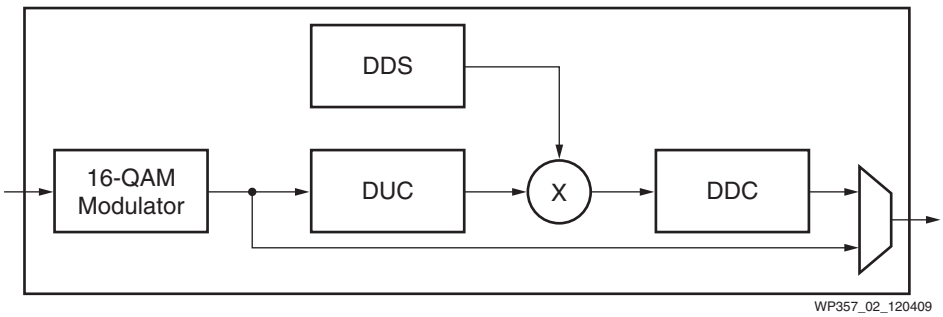

Figure 2: **Block Diagram of Xilinx FPGA DSP Kit Reference Design**

The straightforward nature of this design allows users to focus on design techniques and concepts. Complete reference designs are available from Xilinx for wireless, defense, and video applications that can be extended or modified using these design techniques.

Getting Started with FPGAs for DSP

Xilinx FPGA DSP kits help designers to quickly begin prototyping their applications on Xilinx FPGAs. Each kit comes with a step-by-step hardware and software setup guide that minimizes setup time. A graphical user interface is provided that guides new users through the three steps to getting started, namely:

1. Verify the working hardware by downloading and executing a precompiled design onto the development board.
2. Verify the working development tool flow by providing a step-by-step guide to recompiling the reference design using the ISE Design Suite: System Device Locked Edition and System Generator for DSP.
3. Provide instruction in DSP design through tutorials that extend the functionality of the reference design to show real-world design methodology.

Each of these phases helps new users build confidence in the supplied hardware, tool flow, and design methodology. By doing so, users are provided a solid foundation of experience that can be leveraged to begin building DSP applications.

Easing Adoption of FPGAs for Users New to Xilinx

Adoption of FPGAs for DSP is simplified for new users by supporting high-level design methodologies that do not require RTL design experience. Each kit comes with the ISE Design Suite: System Device Locked Edition, which includes System Generator for DSP. This software enables the use of the DSP-friendly MATLAB/Simulink software modeling environment for FPGA design. System Generator includes over one hundred DSP building blocks optimized by Xilinx that can be used to quickly create highly efficient DSP designs. The blocks also abstract users from the details of FPGA implementation by automatically generating and downloading the FPGA programming file from the Simulink software models.

Several step-by-step tutorials are provided to enable new users to quickly begin designing FPGAs, including:

- Verifying DSP hardware against algorithmic system models
- Designing and programming filter coefficients
- Using FPGA parallelism for greater cost/performance
- Accelerating development using Xilinx DSP IP compilers
- Trading off fidelity vs. hardware efficiency
- Performing hardware co-simulation from Simulink system models
- Incorporating a C synthesis to FPGA design flow
- Interfacing to real-world analog signals using digital-to-analog (DAC) or analog-to-digital (ADC) FMC mezzanine cards

Design Flow Options through High-Level Synthesis Partners

Additional design flow options are available through third-party providers of high-level synthesis tools. These tools offer additional design flows that appeal to developers with different backgrounds, skills sets, and legacy code. Xilinx has undergone an extensive certification process with key providers of high-level synthesis tools to ensure that they deliver high-quality results and ease of use for Xilinx customers. Companies such as AutoESL and Synfora have completed this certification process and offer platform support packages for the DSP development kits that include reference designs and tutorials specific to the Xilinx DSP kits.

Developing Efficient DSP Implementations for Hardware Experts

Developing efficient DSP applications on Xilinx FPGAs poses new challenges for seasoned FPGA experts new to the DSP realm. Often, hardware developers must trade off algorithm fidelity to achieve efficient hardware results. RTL reference designs and tutorials are provided that show how to quickly create high-quality designs using DSP IP compilers, such as the FIR compiler or Fast Fourier Transform (FFT) compiler. The reference designs provide design and verification methodologies that assist with the trade-off between algorithm fidelity and hardware results. Hardware designers learn how to verify their designs using high-level system models developed in MATLAB or Simulink software. Figure 3 shows how the Xilinx FIR compiler can be programmed with coefficients created using the MathWorks Filter Design Analysis (FDA) Tool.

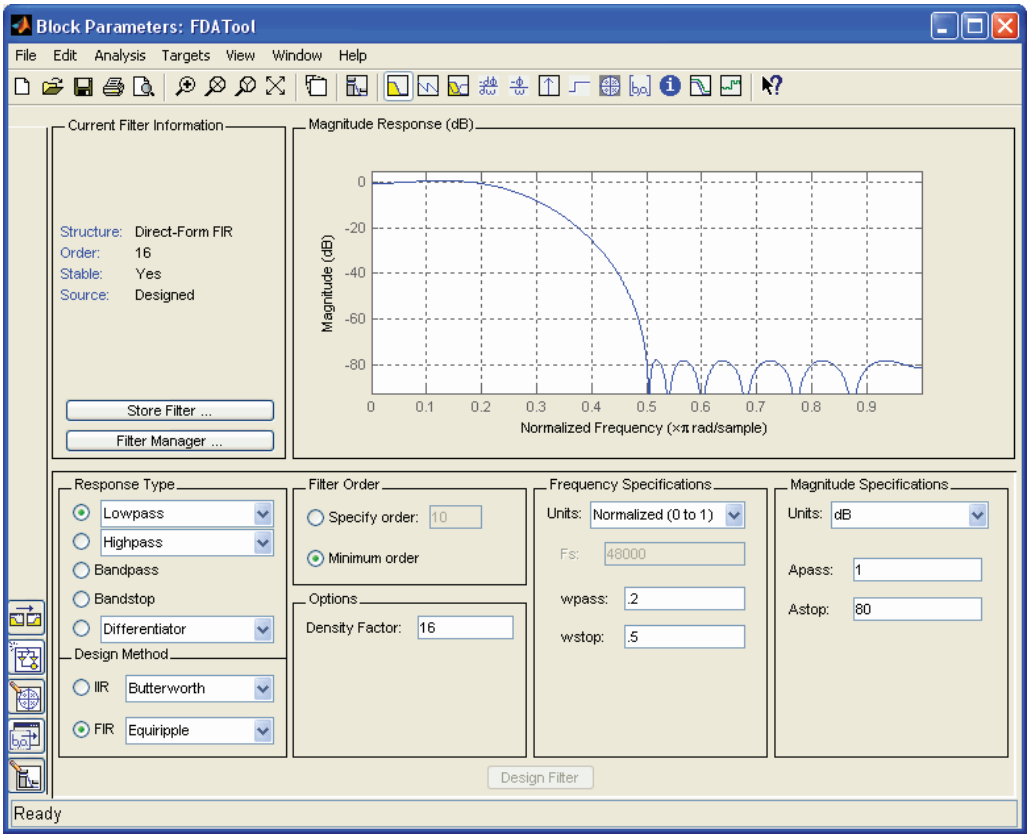

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Figure 3: **Programming the Xilinx FIR Compiler Using the MathWorks FDATool**

A wealth of Xilinx DSP IP is available for use in RTL design flows. The Xilinx DSP development kit describes how to parameterize and incorporate this IP into RTL designs and how best to take advantage of FPGA hardware flexibility to implement high-performance or multi-channel designs.

Interfacing to Analog Signals

DAC and ADC capability can be easily added to Xilinx DSP kits through Xilinx partners. Each kit supports two FMC connectors that can be used to add mezzanine cards that are available from Xilinx partners. Both development boards for the DSP kits include two mezzanine card connectors that support the FMC standard. This standard, defined by the VME International Trade Association (VITA) 57 standard enables the system designer to separate the FPGA computational and I/O transmission portions of a design. Partner-supplied DAC and ADC mezzanine cards that support the Xilinx DSP kits ship with a platform support package that includes interface logic and working examples. This platform support package provides an example design based on the DSP kit targeted reference design, as shown in Figure 4.

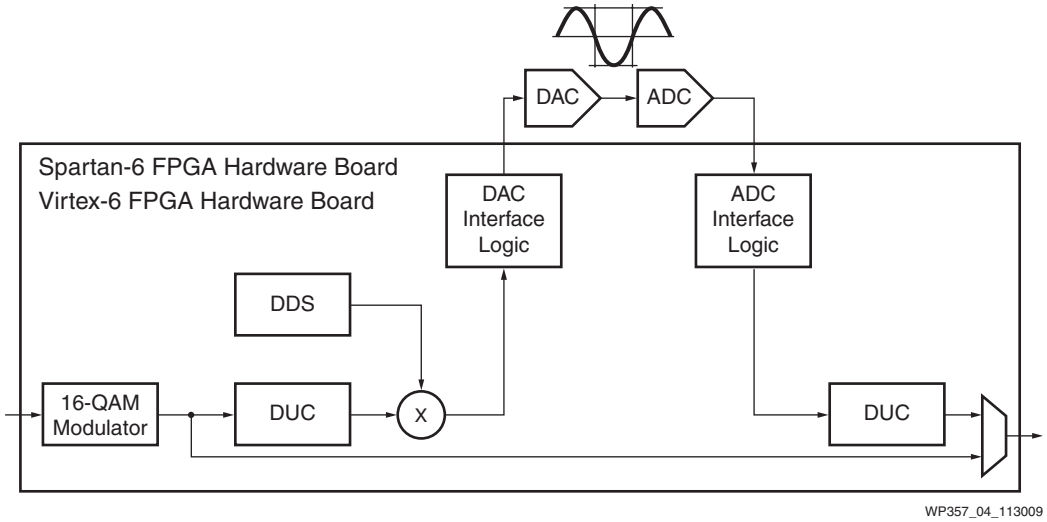

Figure 4: **Xilinx DSP Kit Targeted Reference Design for DAC/ADC Integration**

By offering DAC and ADC FMC mezzanine cards as an option, users can configure a development platform that meets their specific requirements for performance. Users also gain the flexibility of quickly testing multiple options without board redesign. Xilinx has key partnerships in place with Avnet and Curtiss-Write to supply FMC mezzanine cards and reference designs that work with the DSP kits.

Summary

The Xilinx DSP development kits for Spartan-6 and Virtex-6 FPGAs offer an efficient and cost-effective method of creating DSP designs on Xilinx FPGAs. A complete set of hardware, development tools, reference designs, and tutorials introduce new users to the basics of DSP design for FPGAs and then quickly build confidence as reference designs are extended to reflect typical design scenarios. Additional design flows and I/O options are available from a robust ecosystem of partners that supply platform support packages integrated to the DSP development platforms.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/08/09	1.0	Initial Xilinx release.

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