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Accelerating System Designs Requiring High-Bandwidth Connectivity with Targeted Reference Designs

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FPGAs that provide multi-gigabit serial transceivers to implement high-speed serial protocols have become the platform of choice for a large and growing number of applications today. The flexibility to accommodate different protocols, line rates, and emerging standards has made the multi-gigabit serial transceiver the perfect companion to the flexible reprogrammable logic in FPGAs. However, this flexibility comes at a cost. Designing systems that incorporate high-speed serial I/O is difficult enough. Designing systems that work with multiple protocols and different line rates is even more challenging.

To provide a simpler, more accessible solution, Xilinx has created fully-functional, fully-validated, and fully-supported connectivity targeted reference designs introduced in two new kits—the Virtex®-6 FPGA Connectivity Kit (DK-V6-CONN-G) and the Spartan®-6 FPGA Connectivity Kit (DK-S6-CONN-G)—that engineers can use to jump-start their connectivity-based designs.

Connectivity Targeted Reference Designs

To address changing customer requirements and use models, Xilinx surveyed its customers in 2008 to determine what they needed most to complete high-speed serial designs. The results established a number of criteria for the next generation in Xilinx connectivity kits. The most substantial of these was the requirement for a connectivity-based reference design that works with design software, includes all necessary firmware and IP, and can be used as a starting point in a design. The connectivity-based reference design also needs to provide a fully operational system and be tested to a quality standard to enable production-level designs.

To meet these requirements, Xilinx defined the connectivity targeted reference design. It was fairly straightforward to determine what needed to go into the connectivity targeted reference designs. PCI Express® technology is the most commonly required high-speed serial protocol for both Virtex-6 and Spartan-6 FPGAs. XAUI is the second most desired interface for applications using Virtex-6 FPGAs—Gigabit Ethernet is the second most desired for Spartan-6 FPGAs. However, the survey also revealed a consensus that to be truly useful, the connectivity targeted reference designs must also include:

- Source code for easy evaluation and modification of the reference design
- Implementation scripts
- A comprehensive, well-documented design flow
- Support and verification of all reference designs and design flows across the entire tool suite (ISE® software) roadmap for the lifetime of the connectivity kit
- The ability to measure actual transceiver and protocol performance without modifying the design
- Any software required to run the reference design (i.e., an application programming interface (API) for performance analysis)
- Documentation that takes the user from the initial bring-up and evaluation stages through design modification

Another important factor in the connectivity targeted reference design is the need for a direct memory access (DMA) controller. Because all PCI Express devices are memory-mapped, data movement occurs as an exchange between the local onboard memory and the system/host memory. To facilitate this exchange, the connectivity kit must provide an interface to DDR2/DDR3 SDRAM while maintaining support for older (slower) memory devices. To efficiently utilize the available memory space at multi-gigabit serial transceiver speeds, the DMA controller must provide sufficient data transfer sizes and throughput.

To fulfill this requirement, Xilinx worked with Northwest Logic to include a full license for a production Packet DMA engine (with no timeout or reduced functionality) in the Spartan-6 FPGA connectivity kit. This IP, which customers can use in their end systems, significantly simplifies and accelerates design development of all PCI Express applications for the Spartan-6 LXT family. It provides all the necessary PCI Express design elements: the integrated Endpoint block for PCI Express technology, the Northwest Logic Packet DMA engine, and a DDR3 SDRAM controller. The targeted reference design for the Virtex-6 FPGA connectivity kit integrates a production hardware-timeout version of a high-performance (>10 Gb/s) Packet DMA engine from Northwest Logic. This DMA engine enables designers to fully evaluate the performance of system designs implemented on the Virtex-6 FPGA.

Spartan-6 FPGA Connectivity Targeted Reference Design

The Spartan-6 FPGA connectivity targeted reference design is a fully operational bridge between the Gigabit Ethernet IP and the integrated Endpoint block for PCI Express, providing an efficient platform for evaluating the key integrated components in a Spartan-6 FPGA:

- GTP transceivers
- Integrated Endpoint block for PCI Express
- Memory controller block supporting DDR/DDR2/DDR3 SDRAMs and LPDDR (Figure 1).

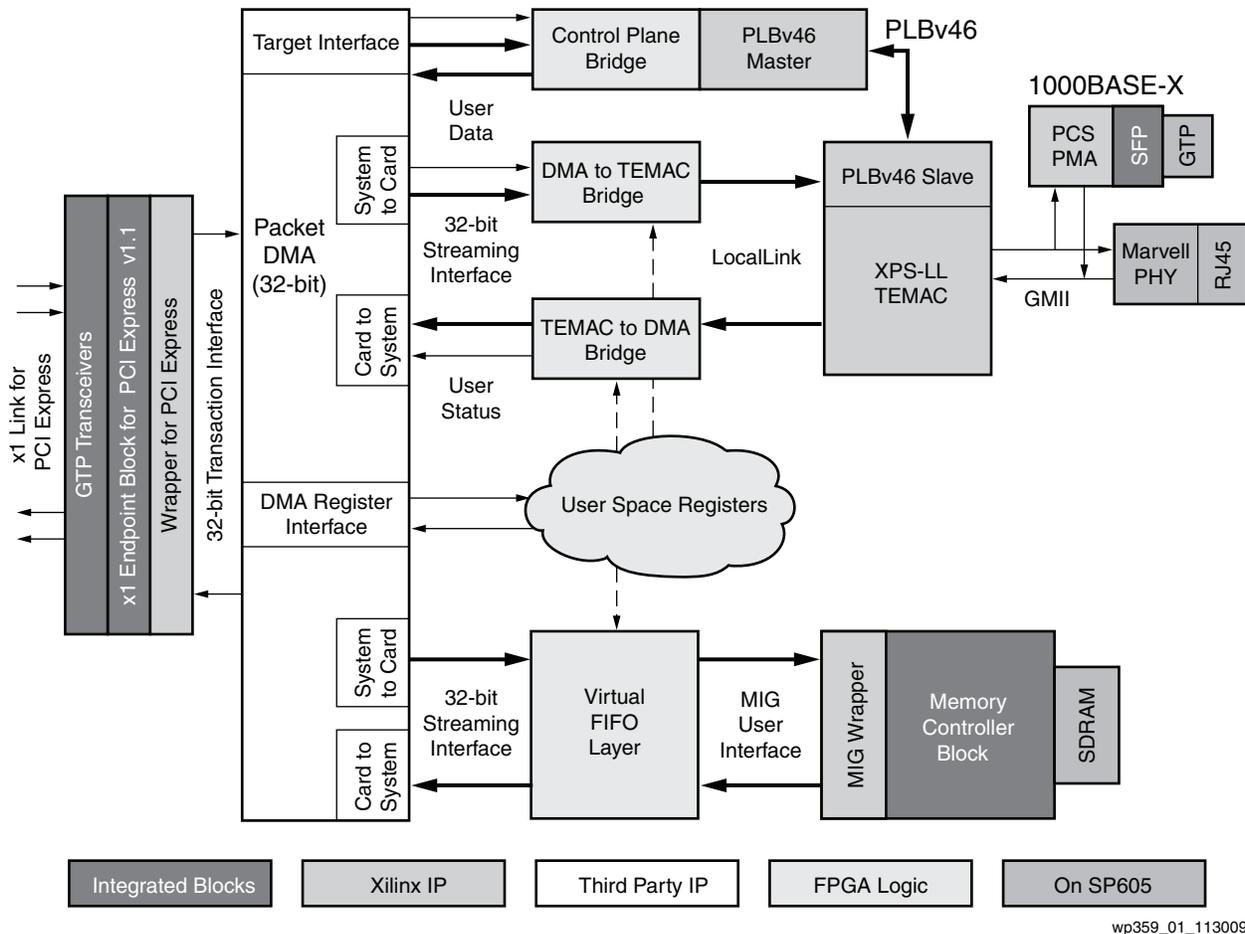


Figure 1: High-Level Diagram of the Spartan-6 FPGA Connectivity Targeted Reference Design

The connectivity targeted reference design also integrates a number of additional IP cores, including the Bus Mastering Packet DMA engine from Northwest Logic (optimized for the Spartan-6 FPGA) and the Xilinx Platform Studio LocalLink Tri-Mode Ethernet MAC (XPS-LL-TEMAC). The DMA engine works in conjunction with the integrated Endpoint block for PCI Express to offload processor data transfer overhead and enables high-speed data movement between the system memory and the FPGA.

This design utilizes one integrated Endpoint block for PCI Express technology that is compliant with the PCI Express Base Specification Revision 1.1. The Endpoint block is used to interface to the host system while the Gigabit Ethernet connection is used to implement a network interface card. The system supports either the Gigabit Media

Independent Interface (GMII) mode using an external Ethernet PHY (typically used to connect to copper networks) or the 1000BASE-X mode using Xilinx GTP transceivers (typically used to connect to optical fibre Ethernet networks). The system design shows how to connect to an external network and run networking applications like Telnet, FTP, etc. The Spartan-6 FPGA connectivity targeted reference design uses the PCI Express standard to exchange data between the local DDR3 memory and system memory. This data exchange is significantly accelerated by a Packet DMA Design maintaining efficient utilization of the available bandwidth.

Each Spartan-6 FPGA connectivity kit comes preconfigured with the targeted reference design loaded and verified on a Xilinx SP605 development board (populated with the Spartan-6 LX45T FPGA). The kit also includes the complete ISE Design Suite: Embedded Edition, device driver files, design source files, and board design files. All the necessary software and files are loaded on a USB memory stick along with printed versions of the Hardware Setup Guide and the Getting Started Guide. This enables customers to bring their systems up quickly, begin evaluation, and start extending the design to build their application.

Virtex-6 FPGA Connectivity Targeted Reference Design

The Virtex-6 FPGA connectivity targeted reference design showcases the capabilities of Virtex-6 FPGAs and various IP cores developed for the Virtex-6 family. Figure 2 provides a block-level overview of the connectivity targeted reference design architecture.

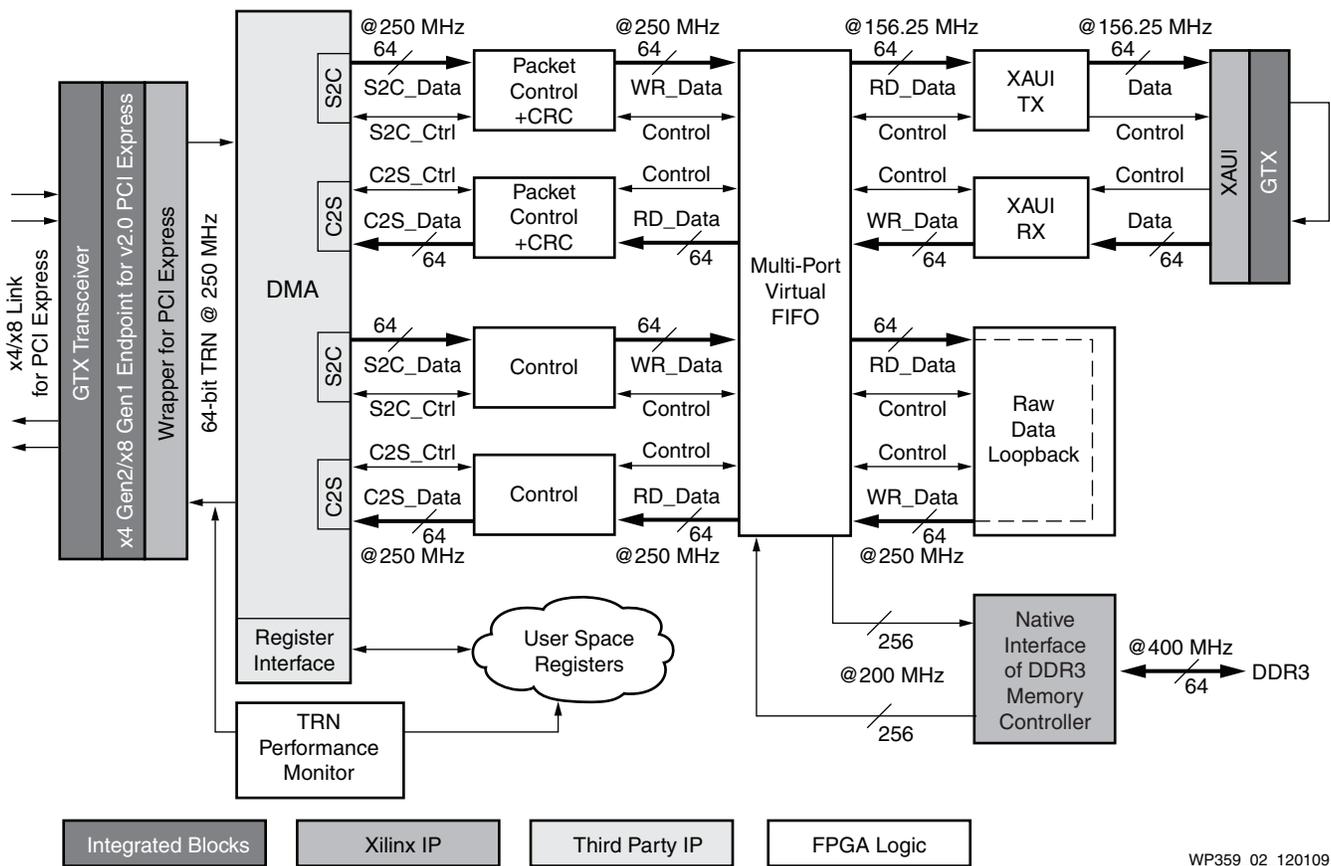


Figure 2: High-Level Diagram of the Virtex-6 FPGA Connectivity Targeted Reference Design

The Virtex-6 FPGA connectivity targeted reference design employs FPGA logic that interfaces with the dedicated blocks and wrappers to deliver up to 10 Gb/s performance end-to-end. The IP cores implemented in the connectivity targeted reference design include:

- Virtex-6 FPGA integrated block for PCI Express (configured as a x4 Gen2 or x8 Gen1 Endpoint)
- Packet DMA from Northwest Logic
- Multi-port virtual FIFO memory interface controller generated with the Virtex-6 FPGA Memory Interface Generator (MIG) tool
- LogiCORE™ IP XAUI core that supports up to 10 Gb/s throughput

Like its Spartan-6 FPGA counterpart, each Virtex-6 FPGA connectivity kit comes preconfigured with the targeted reference design loaded and verified on a Xilinx ML605 development board (populated with the Virtex-6 LX240T FPGA). To enable high-speed serial bandwidth evaluation and measurement, the kit includes the performance monitor interface to the connectivity targeted reference design. The kit also includes the complete ISE Design Suite: Embedded Edition, device driver files, design source files, and board design files. All the necessary software and files are loaded on a USB memory stick along with printed versions of the Hardware Setup Guide and the Getting Started Guide.

Connectivity Targeted Reference Design Deliverables

The connectivity targeted reference design is a design framework that provides key elements to simplify and accelerate system design development. These include:

- Design source and IP files:
 - Top-level system integration RTL source files
 - Xilinx CORE Generator™ technology for dedicated blocks and LogiCORE IP
 - Third-party IP core deliverables and license management
- Simulation environment:
 - Testbench and bus functional models (BFMs) for faster simulation
 - Regression scripts for random and directed tests
- Implementation environment:
 - FPGA/board constraint files
 - Complete steps and parameters for design synthesis
 - MAP, place and route, and timing closure analysis
 - Automated scripts to generate the FPGA programming files
- Software deliverables:
 - Device driver source files
 - Scripts to build and attach the software driver to the hardware board
 - Performance & status monitor application and GUI
- Documentation:
 - Connectivity targeted reference design user guide

Access to the Connectivity Targeted Reference Design

Designers can gain access to a connectivity targeted reference design in two ways:

- Purchase a connectivity kit: Connectivity kits provide the complete targeted reference design framework. A simple, easy-to-follow hardware setup guide enables the customer to bring up the demonstration of the connectivity targeted reference design. The customer can then evaluate the system performance of this connectivity targeted reference design through a performance monitor application. All of the deliverables described in [Connectivity Targeted Reference Design Deliverables, page 5](#) can be accessed by registering on www.xilinx.com and downloading the elements. With these tools, the customer can modify and configure specific system parameters, tune the connectivity targeted reference design to their application requirements, and measure the system performance. The customer can then include the modifications and apply them to their specific design implementations.
- Download the connectivity targeted reference design from the Xilinx website: Customers that already have access to the base Virtex-6 and Spartan-6 FPGA evaluation kits and boards can also gain access to the connectivity targeted reference design deliverables by downloading the complete design from www.xilinx.com. They do not have to purchase the connectivity kit to get started. The IP included in the web download is a hardware evaluation version that is time-limited. Customers that do not have access to the software, IP, and/or hardware elements included in the connectivity kits have to buy them separately to understand and experience the complete hardware bring-up demonstration and flow. However, the included deliverable still enables the customer to go through the simulation and implementation steps and download the time-limited design/bitstream and evaluate system parameters. This enables the customer to quickly ascertain the system performance but precludes them from testing the system parameters through an overnight test run.

Using and Modifying the Connectivity Targeted Reference Design

The connectivity targeted reference design is a building-block architecture design. Design reuse is highly encouraged so that customers can advance their design development stages quickly, as described here:

- System Architecture: The connectivity targeted reference design delivers clocking and reset topologies for high-performance, multi-clock, domain system designs. Architects can borrow this concept and topology for their FPGA-based system design implementations. The I/O blocks of the connectivity targeted reference design can be easily be replaced, modified, or both, by utilizing a different interface. For example, the Virtex-6 FPGA PCIe-10GDMA-DDR3-XAUI connectivity targeted reference design can be scaled up to include the RXAUI interface. Designers can make this change by replacing the XAUI IP instantiation in the connectivity targeted reference design with the RXAUI interface of LogiCORE IP.
- Simulation and Verification: The simulation flow provided with the connectivity targeted reference design includes all the deliverables needed to integrate the tests in the user's environment. This provides the user a working demonstration of an industry-standard simulator like ModelSim. The user can then add more directed and random tests, as needed, and tune the environment for their own

design verification strategies.

- **Design Implementation:** To automate FPGA design and development flow, implementation scripts are provided that support the Xilinx design flow and provide a quick parse-through of possible settings and parameter optimizations. This accelerates closure on design goals—area, design speed, or both.
- **Software Development:** Along with hardware design development strategies, software source files and scripts are also included in the connectivity targeted reference design. These device driver source files enable a software architect to understand the intricacies of mapping and using the underlying hardware infrastructure in the software application. Driver build and insert steps are automated to establish a hardware-to-software connection. A performance & status monitor application and GUI further simplifies the user's ability to configure the available high-speed serial and memory interfaces and to validate system parameter settings.

Use Models

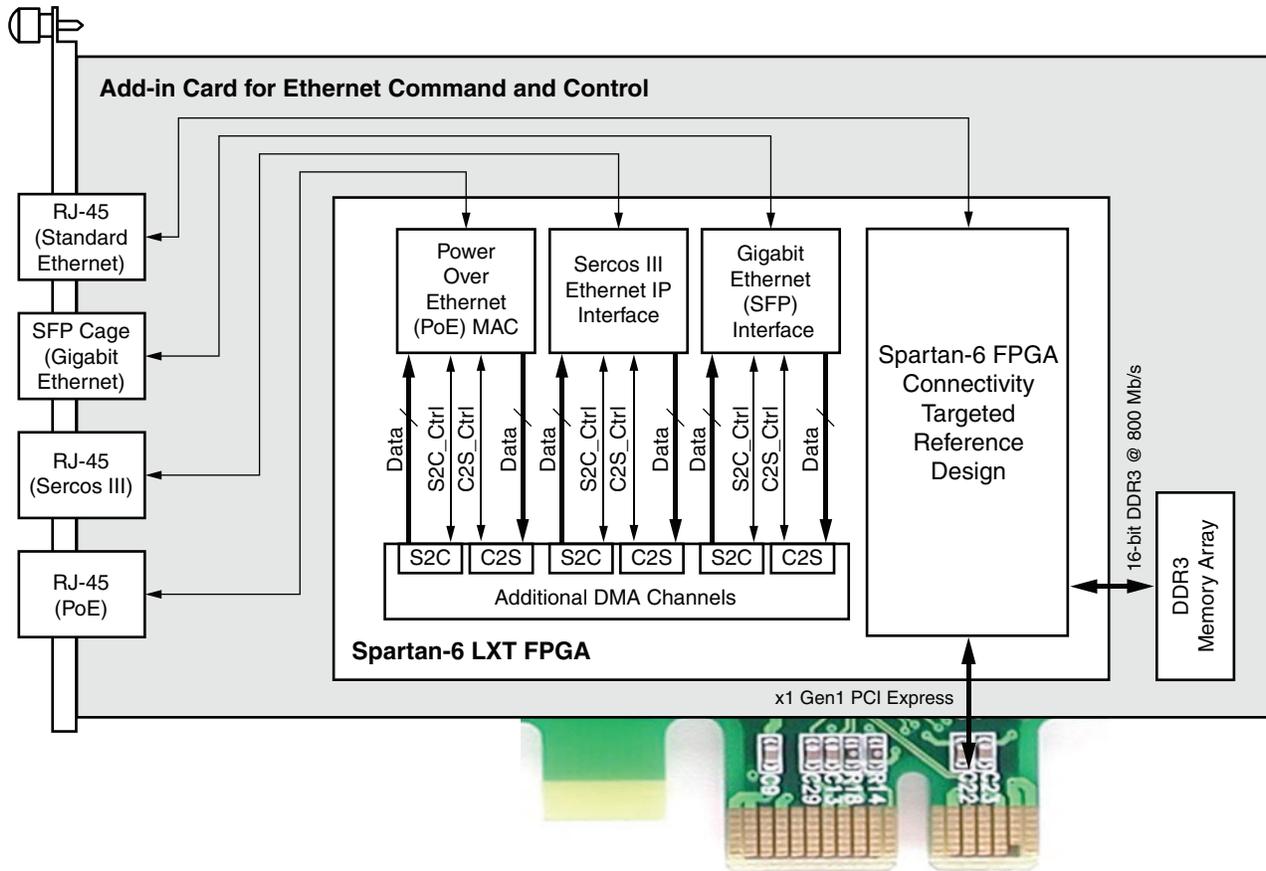
The connectivity targeted reference designs have building-block architectures that can be modified or scaled up and tuned to meet multiple application requirements. For example, Xilinx supports these user flows for the Virtex-6 FPGA connectivity targeted reference design:

- **As Is or Subset:** These are used primarily as a high-bandwidth bridge between PCI Express and XAUI protocol interfaces.
- **Modify by Substitution:** This is used to modify or replace the media/network interface to support higher line rates (e.g., users can replace the XAUI interface of the Virtex-6 FPGA connectivity targeted reference design with another interface such as the 6.25 Gb/s RXAUI or the 6.5 Gb/s Aurora interfaces).
- **Scalable Platform:** This is used to add custom processing blocks such as coprocessing and in-line acceleration.
- **Evaluate/Measure:** This is used for performance evaluation of the PCI Express technology, DDR3, or XAUI interfaces.

The examples in [Spartan-6 FPGA Use Model](#) and [Virtex-6 FPGA Use Model](#) illustrate the application of these use models in the Virtex-6 and Spartan-6 families, respectively.

Spartan-6 FPGA Use Model

The design example shown in [Figure 3](#) is an Ethernet Command and Control card for an industrial Ethernet system. The architecture for this carrier card includes a Spartan-6 FPGA that supports multiple Ethernet protocols: Tri-mode Ethernet MAC (RJ-45), Gigabit Ethernet (SFP), Sercos III, and Power Over Ethernet (PoE). The Command and Control card interfaces to a PC system to control the data and arbitration across these different Ethernet protocols. Because the PCI Express technology link is oversubscribed, to ensure efficient maintenance and packet throughput, the context of current data must be stored until control is established for both the interface throttle and the data switch that services all of the Ethernet interfaces. An external DDR3 memory controller ensures a smooth transition from one Ethernet interface to another.



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Figure 3: **Spartan-6 FPGA Connectivity Targeted Reference Design Use Model**

By adopting the Spartan-6 FPGA connectivity targeted reference design, the user can greatly simplify design development. Access to additional Ethernet interfaces requires only a simple building-block architectural change to the provided DMA design (adding extra channels). This enables the design team to focus their efforts on software development and building differentiation into their solution.

Virtex-6 FPGA Use Model

The design example shown in Figure 4 is a network security carrier card for an Advanced Telecom Compute Architecture (ATCA) chassis. The architecture for this carrier card includes a Virtex-6 FPGA, which provides the line interfaces (SFP, XFP, etc.), and connects to a XAUI backplane. The FPGA design also includes a XAUI interface using PCI Express.

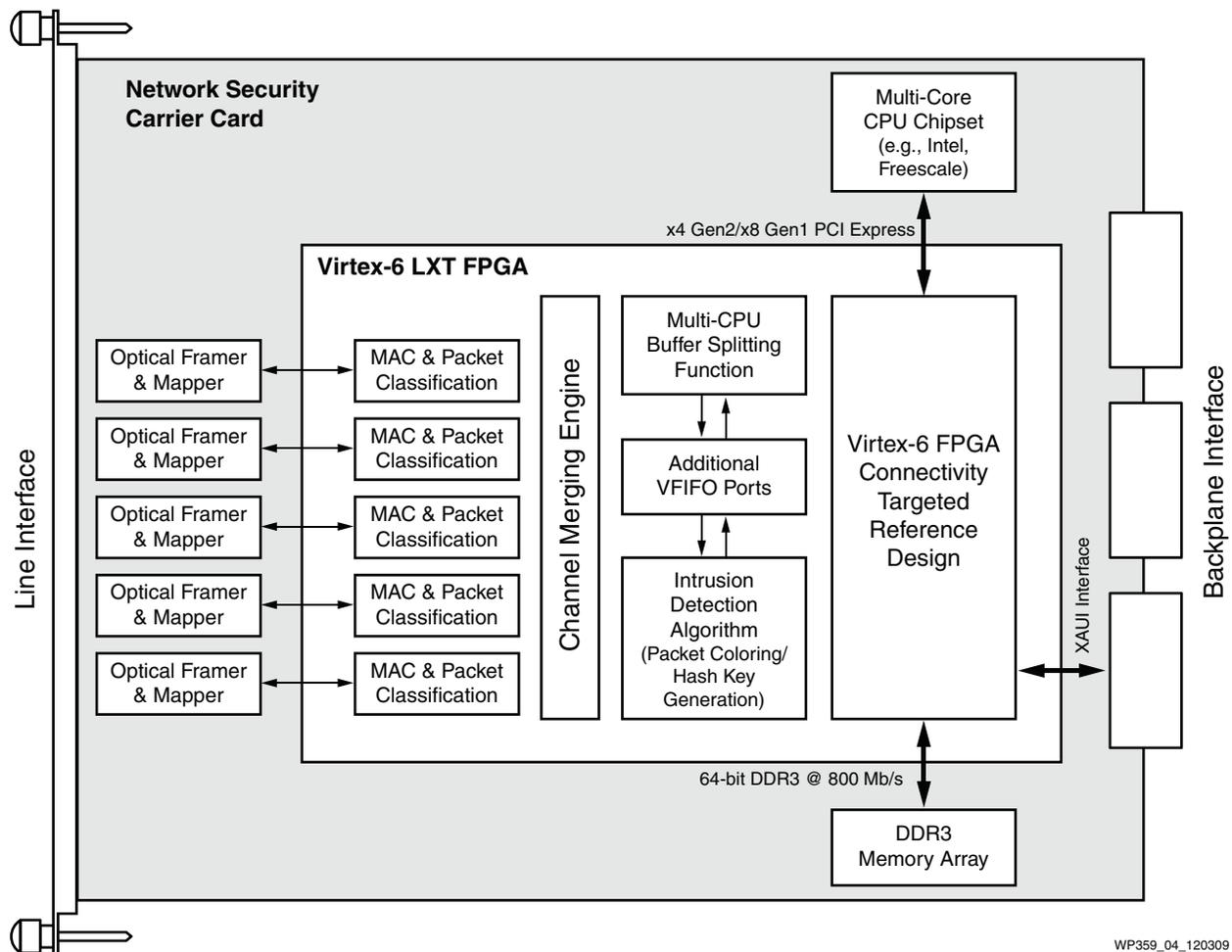


Figure 4: **Virtex-6 FPGA Connectivity Targeted Reference Design Use Model**

Connection to a multi-CPU chipset is enabled by the PCI Express compliant Virtex-6 FPGA. The included DMA engine efficiently transports data to and from the chipset. To ensure error-free operation for highly reliable security systems, the system must store current information until the interface throttle establishes control. A high-bandwidth data pipe to an external DDR3 memory controller ensures this reliability is maintained.

Thus, the Virtex-6 FPGA connectivity targeted reference design can significantly accelerate the design development phase, allowing the design team to focus on key areas for differentiation—network security blocks, such as intrusion-detection algorithms or packet-classification engines.

Summary

Xilinx connectivity design platforms address the mounting market challenges facing designers needing high-speed serial I/O by delivering optimized reference designs. These reference designs are precisely targeted to accelerate application development and serve as a reliable foundation to jump-start customer designs.

To learn more about these kits, visit

<http://www.xilinx.com/technology/connectivity.htm>

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
12/08/09	1.0	Initial Xilinx release.

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