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Unlock New Levels of Productivity for Your Spartan-6 FPGA Design Using ISE Design Suite 14.7

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Xilinx® ISE® Design Suite v14.7 and free ISE WebPACK™ v14.7 tools are the production- optimized tool suites for Spartan®-6 FPGAs that deliver innovation in three critical areas of FPGA design: power reduction, productivity, and performance.

This white paper presents an overview of key achievements and advances in each of these three categories, describing their intent and their impact.

Highlights

Power Optimization

Building on a well-known but often under-utilized power-optimizing design methodology called *clock gating*, ISE Design Suite v14.7 includes automated, intelligent clock gating technology for FPGA design. With this capability, the tool automatically neutralizes unnecessary logic activity, reducing dynamic power usage up to 30%.

Productivity

ISE v14.7 tools offers excellent design productivity with design preservation using PlanAhead, the ability to partition and lock down the placement and routing of timing-critical portions of a design, thus enabling the designer to achieve and maintain timing repeatability. ISE v14.7 tools also include Advanced Microcontroller Bus Architecture (AMBA® protocol) IP, interconnect, and tool support. Xilinx and ARM® jointly developed the version 4 open standard interface specification, which has been widely adopted by Xilinx and its ecosystem partners for development and delivery of plug-and-play IP, providing valuable benefit to design productivity.

Performance

ISE v14.7 tools support production Spartan-6 devices and IP with fully optimized place-and-route and synthesis algorithms, improving Quality of Results (QoR) and greatly decreasing synthesis and implementation runtimes. SmartXplorer in the ISE v14.7 tool release accelerates timing closure by enabling exploration of design strategies in the synthesis space.

Power Optimization

The vast majority of legacy and IP designs are fraught with power inefficiencies. Although the value of power reduction techniques, such as clock gating used to reduced dynamic power consumption, are well understood, rarely does an engineer have the time to manually employ them. ISE v14.7 tools offer a straightforward solution whereby a user can automatically implement power optimizations downstream (after synthesis) that were overlooked or omitted at the RTL level.

A unique set of algorithms enable ISE v14.7 tools to automatically identify and neutralize unnecessary logic activity, a primary contributor to dynamic power inefficiencies. These algorithms utilize the abundant clock enables (CEs) found in the Spartan-6 FPGAs. Each CE is ideally suited for power optimization because it connects to the basic cluster of the FPGA logic (the slice) and controls a small number of registers (only eight). See Figure 1.
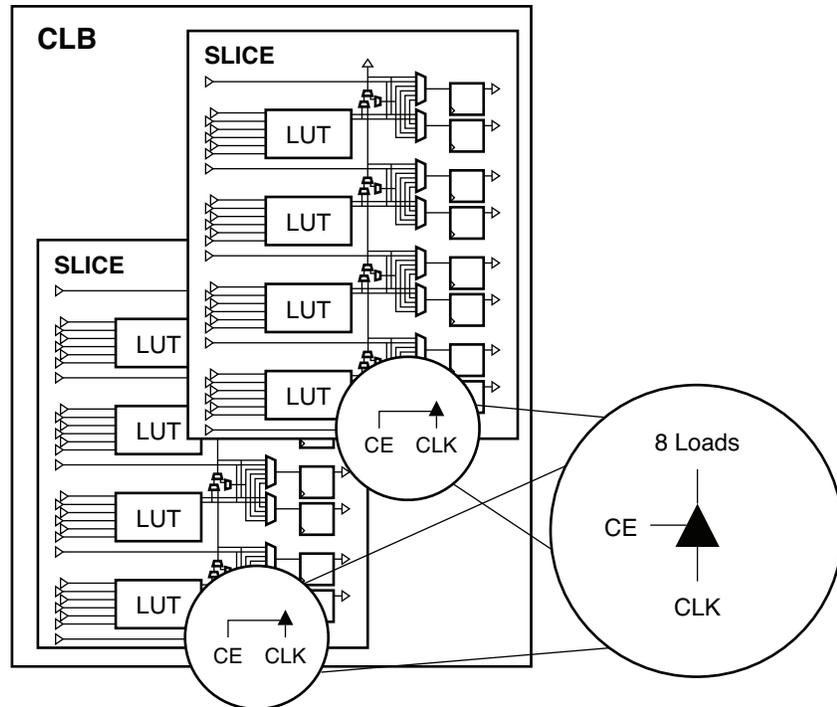
Figure 1: **CE Neutralizes Clock at Source**

Based on a thorough analysis of the sequential elements in the design, the software detects any unnecessary transitions that do not change the final logic and then creates gating signals to cancel these unnecessary transitions, connecting them to the CE, as shown in Figure 2.
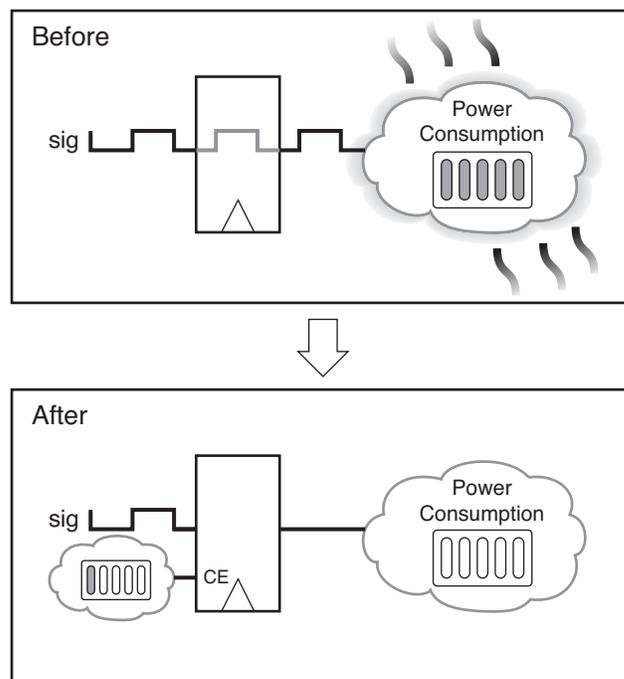
Figure 2: **Activity Factor Reduction via Intelligent Clock Gating**

The use of intelligent, fine-grained clock gating to suppress unnecessary switching in FPGAs can reduce dynamic power by as much as 30%.

ISE v14.7 tools offer intelligent, automated clock gating optimizations integrated with place-and-route algorithms. These optimizations do not alter the preexisting logic or the processing of the design, nor do they alter clock placement. The additional logic created is separate from previous logic and only adds a small percent (an average, 2%) of LUTs to the original design. Thus, in the vast majority of cases, these optimizations have no effect on timing.

In a typical scenario, an engineer would use Xilinx Power Estimator (XPE) or Xilinx Power Analyzer (XPA) to estimate the dynamic power consumption for a design. When the power budget is exceeded, the engineer can, at the flip of a switch, automatically apply intelligent clock gating optimizations to the design. The designer can then use XPA to determine the extent of the anticipated power savings.

See WP370, *Intelligent Clock Gating* for more details.

Productivity

Design Preservation

An FPGA design comprising complex modules can make timing closure difficult to maintain, even though the design of the modules themselves might remain unchanged. As a result, designers can spend vast amounts of time repeatedly trying to regain timing after minor changes to other portions of the design.

The design preservation flow in ISE v14.7 tools solves this problem by allowing the user to establish one or more partitions that can be locked to a particular placement and routing, after timing closure for the partition is achieved. This greatly reduces the number of implementation iterations required during the timing closure phase. Moreover, by using the exact same implementation, design preservation precludes the necessity of performing full verification on unchanged modules.

Establishing an appropriately defined hierarchy in the RTL design phase greatly impacts the success with which design preservation can be employed in a design. The engineer must create partitions that follow the logical hierarchy of an HDL design. Some common rules for creating good hierarchy for partitions include:

- Keep logic that needs to be optimized, implemented, and verified in the same level of hierarchy
- Keep logic that needs to be packed together in the same level of hierarchy
- Register inputs and outputs of modules
- Do not have constants as inputs to partitions
- Do not have unused inputs or outputs in the partition

Even if the design preservation flow was not taken into consideration during the RTL design phase, designs often use independent cores that can still benefit from this flow.

For information on the use of the design preservation flow to achieve repeatable results, see WP362, *Repeatable Results with Design Preservation*. For information on maintaining predictable results throughout the design effort, see WP361, *Maintaining Repeatable Results*.

AXI4: The Path to Plug-and-Play IP

Of all the design productivity benefits delivered in ISE v14.7 tools, the one that might offer the broadest reaching value is the AMBA Advanced eXtensible Interface (AXI). The product of a collaborative effort involving ARM and Xilinx, this IP interface is part of a Xilinx strategic initiative to enable the creation of plug-and-play IP. The interface provides a framework that satisfies the requirements in all three targeted domains (the Embedded, DSP, and Logic/Connectivity domains). Plug-and-play IP removes the design overhead required to address IP with different interface standards, while enabling the rapid growth of a more robust IP ecosystem offering a continuously broadening catalog of IP.

The AXI4 interface standard is built on a high-performance, point-to-point channel architecture that minimizes channel traffic congestion, maximizes data throughput through support of multiple outstanding memory-mapped transactions, and offers a streaming interface that allows efficient data transfer for high-speed serial I/O. Its ability to use register slices to pipeline connections and its support for long burst-based transactions makes it possible to achieve higher F_{MAX} and throughput with AXI4.

A Broadly Adopted Interface Standard for IP

Xilinx and ARM jointly developed the AMBA 4.0 AXI interface. AXI is a royalty-free industry-standard interface that is designed to be very flexible and to enable IP reuse. It is publicly defined in the AMBA specification, which can be accessed at http://www.arm.com/products/system-ip/amba/amba-open-specifications.php.

- The AXI4 specification, one component of AMBA 4.0, is also an open standard. AXI4 enhances the prior generation AXI with support for longer burst lengths.

- AXI4-Lite adds a lightweight, non-bursting, standard interface for peripheral IP or for control registers within an IP.

- AXI4-Stream adds the capability of a lightweight, high-performance streaming interface. Based on the underlying data transfer protocol used for the Write Data Channels of AXI, this interface transfers data with no concept of address through a simple flow-control protocol.

AXI4 supports burst transactions up to a length of 256 data transfers, quality of service and user signaling, and an extensive definition of transaction attributes and device types. A typical system architecture using these components is shown in Figure 3.
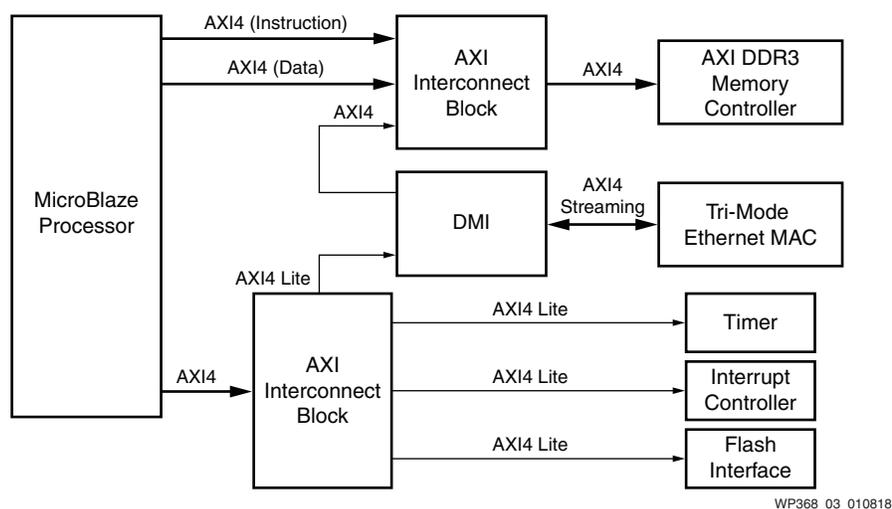

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Figure 3: **A Typical System Architecture Using All Three of the AXI4 Interface Types**

The additional benefits afforded by adopting AXI as the open standard IP interface are many and substantial:

- AXI provides the features that enable multi-processor operation, power control, and security features. Additional features can be added through the use of user-defined sideband signals.

- AXI is thoroughly specified by ARM and already widely understood and accepted by many.

- AXI is an industry-standard interface that supports a viable ecosystem of bus functional models, books, verification IP, and other supporting items. This open industry-standard interface will help to ensure interoperability.

- AXI very effectively separates the interface from the interconnect, returning large benefits in design reuse, design flexibility, and TTM.

- AXI can unify IP. Although not all IP needs to communicate with other IP and not all Xilinx IP will move to an AXI interface, for those cores that do, a standard interface will be used with a very flexible interconnect to provide interoperability.

- AXI is a single well-documented interface with a rich third-party contribution, making it significantly easier to use than the plethora of existing IP interfaces.

- AXI is scalable because it supports a very broad range of functionality and parameters such as data interface width. It provides a signaling design that easily allows pipelining, width conversion, and asynchronous interfaces. It also supports a wide range of topologies—point-to-point, switched, bus, or hierarchical.

In summary, AXI4 has more advanced protocol features that enable the designer to quickly and easily "tune" a system for timing, area, and/or performance. As an open industry-standard specification, it will improve reuse, interoperability, and overall ease of use.

Embedded Configuration Wizard

Productivity benefits substantially from the MicroBlaze™ processor configuration wizard (Figure 4) that dramatically simplifies the optimization of an embedded design for performance, area, or throughput. The wizard benefits both the novice and the expert user enabling either to quickly create and/or explore an appropriate setup for a MicroBlaze processor configuration.

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Figure 4:   **MicroBlaze Processor Configuration Wizard**

Performance

SmartXplorer helps users reach timing closure more quickly by enabling them to run multiple design strategies in parallel. SmartXplorer supports Xilinx Synthesis Technology (XST) as well as the Synopsys Synplify tool. Thus, before running multiple implementation strategies, users can execute several strategies in synthesis to select the best synthesized netlist for the implementation runs, as illustrated in Figure 5.
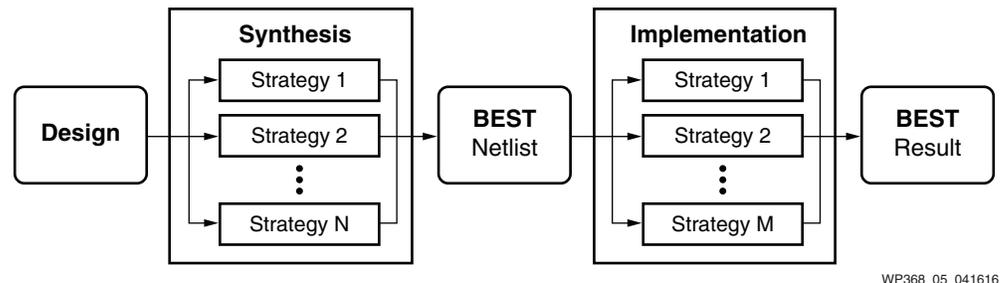

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Figure 5:   **Begin Design Exploration at the Synthesis Phase with SmartXplorer**

The production-level speed specifications for Spartan-6 FPGAs produce an average of 5% improvement in logic performance (QoR) for Spartan-6 FPGAs.

More Advances in ISE Design Suite

Debug with ChipScope Analyzer

The ChipScope™ analyzer supports continuous (otherwise known as "repetitive") trigger mode. In this mode, the trigger is automatically rearmed after a prior trigger event, capture, upload, and display sequence. This feature also includes an optional automatic data export to prevent losing captured information after each trigger/capture/upload/display sequence. This feature allows the user to visually monitor repetitive events without having to manually arm the trigger each time, providing an easy way to capture multiple sparse events that can occur over a long period of time—for example, over a weekend.

The repetitive trigger run mode can also be used to automatically capture and export data so that external applications (such as the MATLAB® software) can import the data for further processing.

Simulation with ISE Simulator (ISim)

ISim is available for the embedded design flow through Xilinx Platform Studio (XPS) and Project Navigator. ISim includes several productivity-enhancing features, including the facility to automatically detect design memories and list them for viewing and editing in a memory editor.

Among its unique attributes, the memory editor arms the user with the facility to explore what-if scenarios, employing a graphical method to force a value or pattern on a signal without the need to recompile the design. The user can automatically scale the time unit and precision for time values shown in the memory editor's waveform viewer by adjusting the zoom factor, or the user can lock in a user-specified choice.

The waveform viewer also provides the means to add signals, dividers, virtual buses, and markers to a waveform configuration, which can then be saved using Tool command language (Tcl) commands. The memory editor also allows the user to navigate directly from the waveform viewer to the HDL source.

Windows 10 Support

Xilinx ISE and free ISE WebPACK tool support for Spartan-6 FPGAs is available for Windows 10 on xilinx.com. Downloading the new Windows 10 version is recommended for all designers to use with their next Spartan-6 FPGA design.

Summary

The Xilinx ISE and free ISE WebPACK tool suites offer excellent quality of results for Spartan-6 FPGAs, and include significant innovations with far-reaching potential. Intelligent clock gating can reduce dynamic power by up to 30%. Design preservation vastly improves the user's ability to achieve and maintain timing closure and design repeatability. With AXI4, Xilinx enables the creation of a vast, ecosystem-supported plug-and-play IP library for Xilinx FPGAs that provides easy access to new and existing IP of both the memory-mapped and data-streaming varieties.

The Xilinx ISE tools, now available on Windows 10, deliver unparalleled value in the three most important criteria for Spartan-6 FPGA designs: better power efficiency, increased productivity, and higher performance.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
01/08/2018	1.2	Updated with Windows 10 information.
04/18/2016	1.1	Updated with current design suite information. Updated Figure 4.
05/03/2010	1.0	Initial Xilinx release.

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