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Xilinx Redefines Power, Performance, and Design Productivity with Three Innovative 28 nm FPGA Families: Virtex-7, Kintex-7, and Artix-7 Devices

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Industry dynamics are driving seemingly insatiable demand for higher bandwidth and higher system-level performance while facing more stringent mandatory requirements to reduce power consumption. At the same time, competitive pressures are forcing customers to increase productivity without sacrificing innovation and differentiation.

To meet these demands, Xilinx® 7 series FPGAs leverage the unprecedented power, performance, and capacity enabled by TSMC's 28 nm high-k metal gate (HKMG), high performance, low power (HPL) process technology and the unparalleled scalability afforded by the FPGA industry's first scalable, optimized architecture to provide a comprehensive platform base for next-generation systems.

Due in large part to the exceptional power/performance characteristics of TSMC's 28 nm HKMG process, coupled with innovative engineering at both the silicon and software levels, Xilinx has pushed the leading edge to unparalleled levels in system power and performance, capacity, and price with the introduction of the Xilinx 7 series: Virtex®-7, Kintex™-7, and Artix™-7 families. Coupled with the proven EasyPath™ cost-reduction technology, these innovative families deliver unprecedented value for next-generation system designers.

The steady migration of FPGA families to new process nodes every two years or so has produced enormous improvements in performance, capacity, and power. In 2008, Xilinx introduced Virtex-6 FPGAs, which offered 11.18 Gb/s serial transceivers, supporting over 1 Tb/s aggregate bandwidth, and 2,016 DSP slices, running up to 600 MHz. The largest Virtex-6 device offers 760,000 logic cells, making it *the* reference for FPGA customers developing ASIC prototyping and emulation applications. Virtex-6 FPGAs were also the first Xilinx product family designed to support voltage scaling, resulting in a 55% total power reduction compared to the previous-generation 65 nm product offerings.

Addressing the Programmable Imperative

When viewed from the customer's perspective, the programmable imperative is the necessity to do more with less, to remove risk wherever possible, and to differentiate in order to survive. In essence, it is the quest to simultaneously satisfy the conflicting demands created by ever-evolving product requirements (i.e., cost, power, performance, and density) and mounting business challenges (i.e., shrinking market windows, fickle market demands, capped engineering budgets, escalating ASIC and ASSP non-recurring engineering costs, spiraling complexity, and increased risk).

To Xilinx, the programmable imperative represents a two-fold commitment. The first is to continue developing programmable silicon innovations at every process node that deliver industry-leading value for every key figure of merit against which FPGAs are measured: price, power, performance, density, features, and programmability. The second commitment is to provide customers with simpler, smarter, and more strategically viable design platforms for the creation of world-class FPGA-based solutions in a wide variety of industries—what Xilinx calls targeted design platforms. See [WP306](#), *Introducing the Xilinx Targeted Design Platform: Fulfilling the Programmable Imperative* for additional information.

The Xilinx 7 series FPGAs strikes at the core of the programmable imperative dilemma by cutting power consumption by 50% in all three families compared to the previous generation. This breakthrough in power consumption provides the headroom for Xilinx to dramatically increase system-level performance in the 7 series families and set new benchmarks in logic density, I/O bandwidth, and signal processing. The 7 series FPGAs lower power consumption allows system designers the flexibility to either lower their system power by 50% or take advantage of additional usable performance and capacity at the previous power budget. See [Figure 1](#).

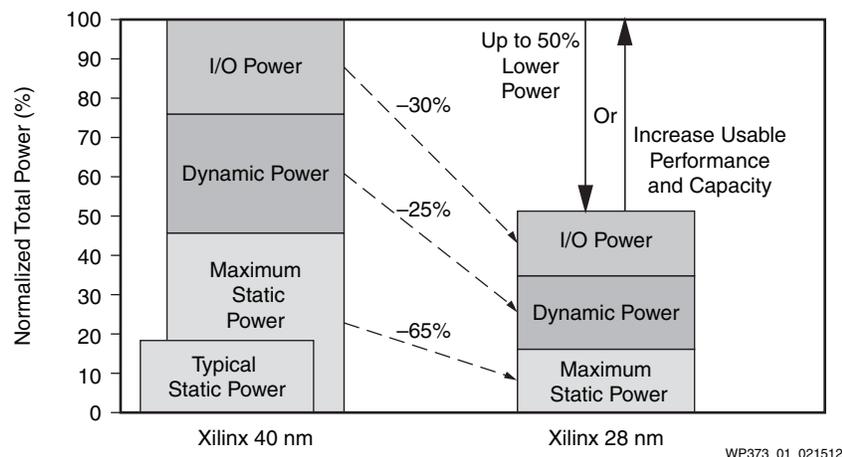


Figure 1: Devices Optimized for System Performance, Capacity, Cost, or Power

See [WP389](#), *Lowering Power at 28 nm with Xilinx 7 Series FPGAs* for more information.

The Xilinx 7 series families address the complete range of system requirements, ranging from low cost, small form-factor, cost-sensitive, high-volume applications to ultra high-end connectivity bandwidth, logic capacity, and signal processing capability for most demanding high-performance applications.

The Virtex-7 family more than doubles the maximum density to 2 million logic cells, offers transceiver line rates up to 28.05 Gb/s, pushes the I/O bandwidth to 2.8 Tb/s, and with up to 3,600 DSP48E1 slices running at 741 MHz, raises the DSP performance to 5,335 GMAC/s (or 2,668 GMAC/s in non-symmetric mode).

The Kintex-7 family, a new class of FPGAs, targets price-performance driven applications, such as those traditionally served by ASICs and ASSPs. The Artix-7 family targets cost-sensitive, high-volume, portable applications.

All three 7 series FPGA families share a scalable, optimized architecture, allowing customers to create a design targeted to one specific 7 series family and then seamlessly port that design to another 7 series family without requiring a redesign. This portability allows customers who have developed highly cost-sensitive systems to scale them toward higher performance and/or higher capacity; likewise, customers who have developed high-performance systems can easily create lower cost versions by migrating their Virtex-7 FPGA designs to Kintex-7 or Artix-7 FPGAs.

The Scalable, Optimized FPGA Platform Architecture

Each new generation of FPGAs, with greater performance and available capacity, has made more complex and more demanding customer designs possible. However, to reduce risk and shorten design time, customer reliance on IP from legacy libraries and third-party IP providers has increased. This forces designers to redesign virtually all existing IP when it becomes necessary to port that IP to a different FPGA family.

The 7 series FPGAs feature a scalable, optimized architecture wherein all devices in all three families are designed with the same architectural building blocks using the fourth-generation ASMBL™ architecture, including: logic fabric (CLB and routing), block RAM, DSP slices, the SelectIO™ interface, PCI Express® control, Agile Mixed Signal (AMS), security, and clocking technology. A closer look at these architectural elements provides a clearer view of the benefit of the shared architectural features:

- Configurable logic blocks (CLBs) – CLBs are the fundamental building blocks of FPGA architecture. In this generation, they are virtually identical to the CLBs used in Virtex-6 FPGAs and similar in many ways to Spartan-6 FPGAs. They use the same look-up table (LUT) structure (6-LUT), control logic, enables, and outputs. The LUTs in CLBs can function in three modes: distributed LUTRAM, serial shift registers, and logical functions.
- Block RAM – Block RAM for 7 series devices support 18K/36K with optional integrated FIFO logic based on the Virtex-6 FPGA design. The 7 series devices also support single-port and true-dual port functionality with the same data, control, and clock inputs as in Virtex-6 and Spartan-6 devices.
- Clocking structure – The clocking structure has up to 24 clock management tiles (CMTs), each consisting of one mixed-mode clock manager and one phase-locked loop (PLL) based on the Virtex-6 FPGA design.

- SelectIO™ Interface – The SelectIO interface with ChipSync™ technology supports higher speeds to accommodate new I/O standards while the interface between the FPGA logic and these I/Os, the per-bit de-skew, and control remains fundamentally unchanged. The 7 series devices also provide support for state-of-the-art 1.6G LVDS and 1,866 Mb/s DDR3 memory interface speeds. Process-tuned for lower power, the Artix-7 family is capable of 1.25G LVDS and 1,066 DDR3 memory interface speeds.
- DSP – The DSP48E1 slices in 7 series devices provide 25 x 18 systolic elements to enable pre-adder, multiply-accumulate engines that are controlled by the same control signals used in the last generation. They also contain the same low-latency pipeline stages and support pattern detection, the same as the DSP48E1 slices found in Virtex-6 devices.
- Serial Transceivers – Transceiver count in the 7 series FPGAs ranges from 8–16 transceiver circuits in the Artix-7 family, 8–32 transceiver circuits in the Kintex-7 family, and up to 96 transceiver circuits in the Virtex-7 family. Each serial transceiver is a combined transmitter and receiver. The various 7 series serial transceivers use either a combination of ring oscillators and LC tank or, in the case of the GTZ, a single LC tank architecture to allow the ideal blend of flexibility and performance while enabling IP portability across the family members. GTP, GTX, and GTH serial transceivers support higher rates but retain similar PCS/PMA interfaces, control, and clocking inputs as Virtex-6 and Spartan-6 devices.
- Agile Mixed Signal – All 7 series devices have independent dual 12-bit, 1 MSPS, 17 channel Agile Mixed Signal capability and contain temperature and supply sensors that greatly enhance reliability, security, and safety capabilities.
- Security – In all 7 series devices, an encryption block leveraging the 256-bit AES coding mechanism allows for loading secured bitstreams where the storage of the encryption key is similar to Virtex-6 devices (permanently inside the device (eFUSE) or on battery powered memory cells).
- PCI Express– All 7 series devices include at least one integrated block for PCI Express technology that can be configured as an Endpoint or Root Port, compliant to the PCI Express Base Specification Revision 2.1 or 3.0. Integrated blocks for PCI Express are fundamentally unchanged from Virtex-6 FPGAs, leveraging the same control, data, and clocking inputs as the legacy devices while including support for PCIe Gen1, Gen2, and Gen3. Xilinx provides a light-weight, configurable, easy-to-use LogiCORE™ IP wrapper that ties the various building blocks (the integrated block for PCI Express, the serial transceivers, block RAM, and clocking resources) into an Endpoint or Root Port solution.
- Partial Reconfiguration - All 7 series FPGAs support partial reconfiguration, which is an extremely powerful and flexible feature that allows the user to change portions of the FPGA while other portions remain static. Users can time-slice these portions to fit more IP into smaller devices, saving cost and power. Where applicable in certain designs, partial reconfiguration can greatly improve the versatility of the FPGA.
- Cost Reduction Capability – The identical Xilinx EasyPath technology architecture provides the fastest and only no-risk cost-reduction path in the FPGA industry. The EasyPath-7 FPGAs support Kintex-7 FPGAs and Virtex-7 FPGAs, providing 100% of the capabilities found in the equivalent 7 series FPGA.

In the past, changes to the data, control, and clocking inputs to these elements could cause IP to break as they were ported from one FPGA family to the next. Engineers were forced to review data sheets, instantiation templates, and user guides to determine which modifications were required to make the IP work. After the change was determined, the designer needed to re-synthesize, re-test, and re-verify the IP.

By unifying the elements within the 7 series FPGA families, IP can leverage the same data, control, and clock inputs in elements that behave in the same predictable way. This portability creates profound value for companies with vast repositories of IP and third-party IP developers by making their IP easier to use and reuse, enabling faster development of highly scalable applications. Even the Zynq-7000 Extensible Processing Platform (EPP), containing ARM® dual-core Cortex™-A9 MPCore processors, has the same optimized 7 series logic architecture, block RAM, DSP48E1 slices, Agile Mixed Signal, and PCI Express, enabling easier migration from 7 series designs.

Derived primarily from the fundamental building blocks of the Virtex-6 architecture, this scalable architecture will enable designers to migrate the majority of their Virtex-6 FPGA designs to any of the Xilinx 7 series FPGAs with minimal effort.

The three 7 series FPGA families target the broadest range of power, performance, cost, and capacity requirements ever offered, accessing new markets and applications (see [Table 1](#)).

Table 1: Product Highlights

Devices	Description	Markets
Virtex-7	Highest performance and capacity FPGAs	Wired, wireless, and test and measurement (T&M) applications, such as 400G bridging/switch fabric, advanced RADAR systems, ASIC emulation, and high-performance computing systems.
	50% lower power than previous generation Virtex devices	
	Up to 2M logic cells	
	Up to 2.8 Tb/s bidirectional total serial bandwidth and 96 total serial transceivers	
	Up to 16 serial transceivers at 28.05 Gb/s plus up to 72 serial transceivers at 13.1 Gb/s	
	Up to 96 serial transceivers at 13.1 Gb/s	
	Up to 56 serial transceivers at 12.5 Gb/s	
	Up to 1,200 SelectIO interface pins, enabling the industry's most parallel banks of 72-bit DDR3 memory interfaces, supporting up to 1,866 Mb/s	
	Highest DSP-to-Logic Cells ratios – up to 3,600 DSP48E1 slices for 5,335 GMAC/s (or 2,668 GMAC/s in non-symmetric mode)	
	Highest block RAM-to-logic cell ratios (up to 68 Mb with 1,139K logic cells)	
	High Range (3.3V) and High Performance (1.8V) I/O	

Table 1: Product Highlights (Cont'd)

Devices	Description	Markets
Kintex-7	Industry's best price-performance FPGAs	Wireless, industrial, medical, broadcast, and military applications, such as high-volume 10G optical wired communication equipment, LTE wireless networks, next-generation high definition 3D flat panel displays, set top boxes, medical and avionics imaging, motor control, and broadcast video-on-demand systems.
	50% lower power than previous generation Virtex devices	
	Virtex-6 FPGA performance at one half the price	
	Up to 32 serial transceivers at 12.5 Gb/s	
	High DSP-to-Logic ratios - with up to 1,920 DSP48E1 slices for 2,845 GMAC/s (or 1,423 GMAC/s in non-symmetric mode)	
	High block RAM-to-logic cell ratios (up to 34.4 Mb with 478K logic cells)	
	High Range (3.3V) and High Performance (1.8V) I/O	
Artix-7	Lowest power and lowest cost, small form factor FPGAs	Consumer, automotive, and highest volume applications, such as battery-powered portable ultra-sound equipment, commercial digital camera lens control, military avionics, portable eReaders, military software defined radios, multifunction printers, automotive infotainment, video surveillance, and communications equipment.
	65% lower static and 50% lower power than previous generation Spartan devices	
	35% lower cost compared to Spartan-6 devices	
	Up to sixteen 6.6 Gb/s serial transceivers	
	High DSP-to-Logic ratios - with up to 740 DSP48E1 slices for 929 GMAC/s (or 465 GMAC/s in non-symmetric mode)	
	High block RAM-to-logic cell ratios (up to 13 Mb with 215K logic cells)	
	High Range (3.3V) I/O	

7 Series Family Details

Virtex-7 Devices

The Virtex-7 family offers industry-leading capacity and twice the system performance of Virtex-6 devices. Unquestionably well-suited for high-end designs, the largest device in this family is the first FPGA to provide 2 million logic cells—2X larger than any alternative FPGA, with system performance numbers that are equally impressive.

System performance is the combination of I/O bandwidth to bring data on and off the device, low-latency processing performance, on-chip storage for dynamically updated coefficients, and I/O that supports fast off-chip memory for data storage. The ultra-high-end Virtex-7 family addresses all of these aspects to deliver the highest system performance for the most demanding applications.

In addition to providing the highest system performance on the market, the Virtex-7 family supports critical frequencies for multi-level logic paths, enabling support for the most demanding applications in specific end markets:

- 491 MHz for next-generation wireless applications
- 334 MHz for wired applications
- 148.5 MHz for broadcast applications
- >500 MHz for aerospace and defense systems

The composite of industry-leading specifications that characterizes the Virtex-7 family will enable customers to easily move their multi-chip designs to single-chip implementations, thereby acquiring even greater benefits of cost, power, and performance. See [DS180](#), *7 Series FPGAs Overview* for details.

Kintex-7 Devices

The Kintex-7 family sets a new price-performance point for FPGAs, designed to dislodge ASSPs and ASICs in cost-sensitive, low-power, high-performance applications. This family creates the potential for substantial penetration and growth in market segments and applications that were previously inaccessible to FPGAs.

Kintex-7 devices are half the price and offer the equivalent performance to a Virtex-6 LXT device.

To achieve this price-performance, Xilinx leveraged a number of architectural innovations. First, Xilinx used its column-based ASMBL architecture (introduced in Virtex-4 FPGAs) to tune Kintex-7 devices to create the ideal feature mix at the lowest price point.

Second, Xilinx exploited the fact that at 28 nm, die sizes have gotten smaller and the device packaging now makes up a larger component of the overall cost. By exploring innovative packaging options, such as lidless flip-chip, Xilinx is able to meet performance requirements while dramatically reducing device cost.

Finally, the Kintex-7 family includes a unique combination of transceiver technology and packaging to achieve the required bandwidth, i.e., higher-performance transceiver technology is paired with higher-performance packaging, while moderate transceiver performance is paired with less expensive packaging. Thus, Kintex-7 devices offer the highest level of signal integrity at the lowest price point. This combination of "market-tuned" resources coupled with cost-optimized packaging results in the highest performance per dollar available in any FPGA family. See [DS180](#), *7 Series FPGAs Overview* for details.

Artix-7 Devices

Artix-7 FPGAs benefit from Virtex series based improvements in architecture and routability, providing superior performance (30% over Spartan-6 devices) while delivering a 50% improvement in power and a 35% improvement in cost over the previous-generation Spartan-6 FPGAs—critical values that address the needs of cost-sensitive, lower-power, high-volume markets.

The Artix-7 family also offers serial I/O line rates up to 6.6 Gb/s, with 3.3V capable I/O to allow interfacing with legacy components. Devices are offered in various types of low cost wire-bond packages—from chip-scale packaging with 0.8 mm ball spacing for the smallest form factor to BGA packaging with 1.0 mm ball spacing for low-cost PCB manufacturing. In short, for their performance level, the Artix-7 family offers the

industry's lowest cost and smallest form factor FPGAs. See [DS180](#), *7 Series FPGAs Overview* for details.

Silicon Foundation for Next-Generation Targeted Design Platforms

Viewed from the perspective of the system designer, the Programmable Imperative is an unrelenting challenge to continuously accomplish more with less: more performance with less power, more function and differentiation in less time—all at a lower cost and in smaller form factor packages. Xilinx views the Programmable Imperative as an opportunity to empower its customers to meet these challenges and regards it as the foundation for a two-fold commitment:

- To continue developing programmable silicon innovations at every process node that deliver industry-leading value for every key figure of merit against which FPGAs are measured: price, power, performance, density, features, and programmability
- To provide customers with simpler, smarter design platforms for the creation of world-class FPGA-based solutions in a wide variety of industries—what Xilinx calls Targeted Design Platforms

Xilinx Targeted Design Platforms comprise the silicon (FPGAs), development tools, IP, boards, and targeted reference designs that enable customers to bring new, effectively differentiated products to market faster, with less risk and cost.

Simplified Design

The scalable, optimized architecture shared by the 7 series FPGA families inherently produces more portable RTL and IP. Since the lowest-level building blocks of the architecture are shared across the 7 series families, engineers can port hand-coded RTL with block instantiations of memories, DSP blocks, or logic elements to any of the 7 series devices without modifications, eliminating time-consuming re-optimizations.

The Xilinx ISE® Design Suite also contributes substantially to the quest for a simpler, smarter, more efficient design process with three unique features:

- Design Preservation – The ability to lock down selected levels of hierarchy in the design from one run to the next to maintain timing closure and repeatability of results.
- Partial Reconfiguration – The ability to modify a portion of an operating FPGA design, enabling designers to dramatically reduce system cost and power consumption by fitting sophisticated applications into the smallest possible device.
- AMBA® Advanced Extensible Interface (AXI-4) – The interface standard (the result of a collaborative effort with ARM) enables the creation of Plug-and-Play IP. Built on a high-performance, point-to-point channel architecture, the interface minimizes channel traffic congestion, maximizes data throughput through support of multiple outstanding memory-mapped transactions, and offers a streaming interface that allows unlimited burst size for high-speed I/O.

The ISE software also has the option to leverage multi-core processors for the 7 series families to improve run times.

Plug-and-Play IP

With device sizes in the largest 7 series FPGAs topping 2 million logic cells, customers face the daunting task of filling these FPGAs with very large and very complex designs in as short a time as possible, making the use of legacy designs and third-party IP virtually mandatory. To meet customer demand for a wide variety of IP cores for many markets and applications, Xilinx introduced the Plug-and-Play IP initiative in the Xilinx design tools to create an open and scalable infrastructure that employs a standard interface architecture and tool flow for the development and deployment of IP.

The Plug-and-Play IP Initiative is Xilinx's response to growing customer demand for system-level design using multiple IP cores from multiple sources. Plug-and-Play IP removes the design overhead required to address IP with different interconnect standards.

Combined with the scalable, optimized architecture that enables easy migration of complete designs across all three 7 series families, Plug-and-Play IP will dramatically shorten design times for even the largest designs.

Conclusion

Xilinx has created extraordinary value in its 7 series FPGAs, leveraging the power advantage afforded by the TSMC 28 nm HKMG, HPL process to push the leading-edge envelope in performance, price, and capacity. Moreover, the 7 series FPGAs are the first to employ a scalable, optimized architecture to provide unparalleled design portability, scalability, and productivity.

In addition to enabling the migration of designs across the three families, the 7 series architecture also simplifies migration from Virtex-6 and Spartan-6 devices to the 7 series families because all 7 series FPGA architectural elements are based on elements of the Virtex-6 family. With careful consideration, customers can develop IP in Virtex-6 and Spartan-6 and then migrate this IP to Virtex-7, Kintex-7, and Artix-7 families.

Learn more about the Xilinx 7 series FPGAs and the applications they enable at Xilinx.com/7 and follow the guidelines included in this white paper to start building IP and applications using Virtex-6 and Spartan-6 devices with the confidence that this investment can be leveraged in the 7 series families and beyond.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/21/10	1.0	Initial Xilinx release.
03/28/11	1.1	Updated the introduction. Also updated all sections to reflect new 7 series product family information.
10/11/11	1.2	Updated Addressing the Programmable Imperative , The Scalable, Optimized FPGA Platform Architecture , Table 1 , and Simplified Design .
02/15/12	1.3	Updated The Scalable, Optimized FPGA Platform Architecture and Artix-7 Devices sections.
05/01/12	1.3.1	Minor typographical updates.
10/15/12	1.4	Updated The Scalable, Optimized FPGA Platform Architecture .

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