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Using Xilinx FPGAs to Solve Endoscope System Architecture Challenges

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The advent and growth of minimally invasive surgery (MIS) has made endoscopes an indispensable part of improved surgical procedures. Advances in semiconductor manufacturing and imaging technology continue to fuel innovation and pave a path for endoscopes to be used in many new applications each year.

This white paper describes how Xilinx® FPGAs can enable endoscope system manufacturers to meet complex design constraints to produce competitive products and the use of Xilinx FPGAs to build low power, small form-factor endoscope camera heads; low cost, high-performance camera control units (CCUs); and low cost, versatile image management devices.

Introduction to Endoscope Systems

Technology advancements have enabled the use of endoscopes in many different applications. Health care providers have aggressively adopted endoscopic techniques and continue to challenge suppliers to push the boundaries of technology for many reasons.

Endoscopy provides unprecedented diagnostic capabilities for certain ailments that no other method can match today, such as detecting polyps in the colon and ulcers or fungi in the GI tract. Diagnosis with endoscopes is radiation-free and can be done with minimal pain to the patient. With these inherent benefits, physicians have aggressively adopted endoscopic techniques and are continually demanding innovation to improve imaging capabilities even further. Such demands force suppliers to deploy new techniques such as Narrow Band Imaging, Autofluorescence Imaging, and Multi-Band Imaging. These methods provide much more accurate visualization of blood vessels, lesions, and mucosal surfaces than could be achieved in earlier endoscope systems, enabling physicians to more accurately diagnose patient ailments.

Endoscopy greatly improves the quality of patient care by enabling minimally invasive surgical techniques. While traditional surgeries required large incisions to enable surgeons to view the subject tissue and to use large, hand-held instruments, endoscopes and laparoscopes (a type of endoscope with a rigid tube) enable minimally invasive surgical techniques with only one or two incisions less than a centimeter in length. This greatly reduces risk of infection and provides faster patient recovery time, allowing patients to leave the hospital in days compared to weeks for many procedures. Shorter hospital stays are a big benefit to the cost structure of health care providers and insurance companies. However, laparoscopic procedures tend to be more expensive and take longer to perform than open cavity procedures. So the health care providers are continually pushing for innovative ways to perform operations more efficiently and at a lower cost point.

Physicians want equipment to be small, flexible and light weight so they can easily position their equipment for sustained periods of time to maximize patient comfort without causing operator fatigue. Within the case of both diagnostic and surgical endoscopy, burden is placed on the physician to maneuver equipment through small openings to obtain a usable visual image of the subject. In diagnostic procedures with flexible endoscopes, the physician often has to hold the endoscope for a period of time. In surgical procedures, although equipment is mounted on a mechanical assembly, several laparoscopes and operating tools are used simultaneously in a confined location, leading to complexity in setting up for a procedure.

Within this small system, the electronics must also be low heat generating, since there is minimal clearance for heat dissipation techniques, and the tolerance for heat at the exterior of handheld products is low. This puts the demand on suppliers to keep the mechanical footprint of the electronics to a minimum with the added challenge of satisfying the low power design constraints.

Endoscope System Architecture

A typical endoscope system has five key components (Figure 1).

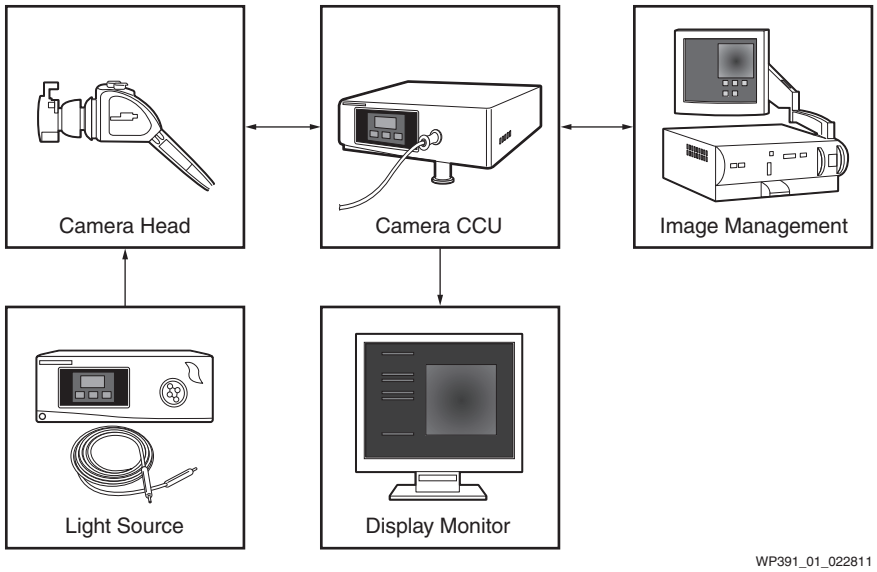

Figure 1: **Endoscope System Components**

Camera Head

The camera head is the physical device that contains the CCD or CMOS image sensor, pre-processing electronics and connections for the light source, and various mechanical apparatus such as water tubes, air, vacuum, and biopsy tools.

In flexible endoscopes, the image sensor is located at the distal end of the tube; in rigid endoscopes the sensor is located at the proximal end of the tube, often in the camera head itself. The camera head is connected to the camera control unit through a cable that supplies power to the camera head and enables data transfer between the two units.

One of the main design constraints of the camera head is to keep the mechanical form factor and the electronics footprint to a minimum for improved ease of use. Reducing the electrical components through integration of functionality and using smaller component packages provides system designers the ability to shrink the overall mechanical envelope. To further reduce the form factor, system designers can also reduce the amount of processing functions performed in the camera head. This places the burden of performing the majority of the image processing on the CCU. A typical system-level functional block diagram of an endoscope camera head is shown in Figure 2.

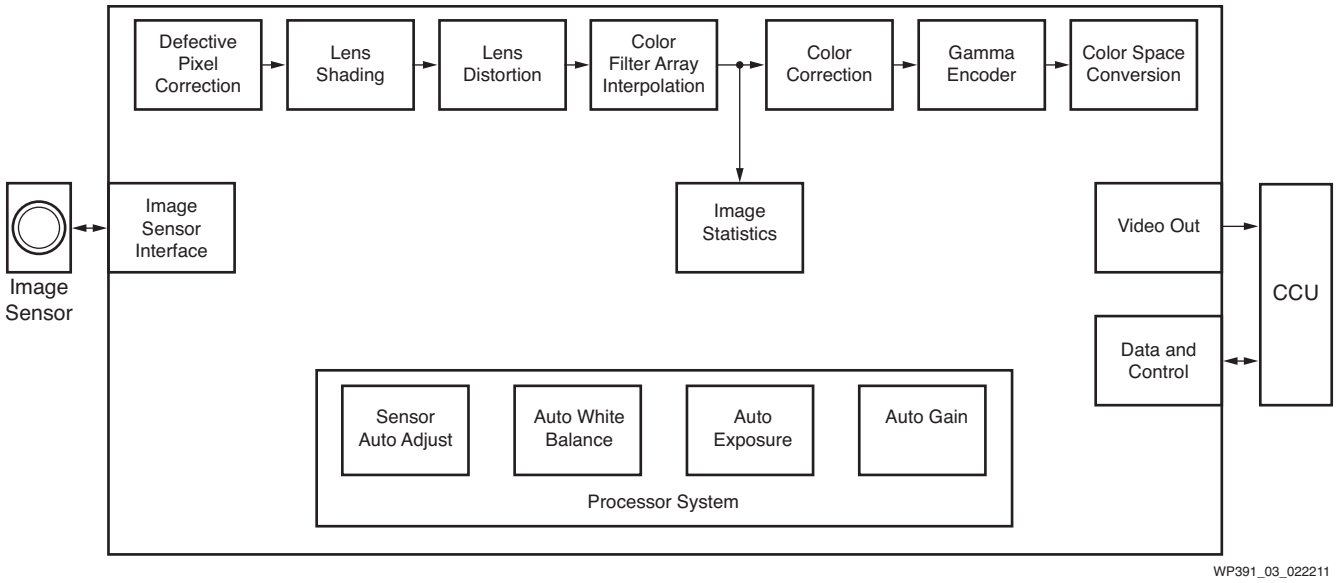

Figure 2: **Endoscope Camera Head Diagram**

The initial image is generated on the CMOS/CCD image sensor and is then passed to the downstream image processing chain before being transmitted to the CCU. The standard Bayer pattern for image sensors is passed through the lens shading and distortion blocks to help minimize noise and create uniformity in the image. The Color Filter Array (CFA) interpolates between pixels and converts the Bayer image to RGB color space. The RGB image can then be used to automatically control the Auto Exposure, Gain, White Balance, and other parameters such as Focus.

- Auto Exposure - Controls the amount of brightness within the image by allowing the sensor to absorb more/less light. There are several functions starting with the mechanical shutter through the digital gain that affect exposure.
- Gain - The amount of amplification that is performed on the sensor output. This is one mechanism used to adjust exposure.
- White Balance - Controls the color fidelity of the image and usually employs the color correction block to align the image to the appropriate color temperature of the scene.
- Focus - When using an Auto-Focus lens, this provides the sharpest image automatically. Focus is generally independent of the color or exposure controls.

Adjustment of the exposure, gain, and white balance is most effective when completed as far upstream as possible where there is a minimal amount of noise. These adjustments are completed by a two-step process; first, a dedicated hardware block determines the image statistics; second, the image statistics are passed to the software for decision making on how to set the various parameters in the system for optimum quality. The Exposure, Gain, and White Balance functionality are inter-dependent to some extent and, therefore, can be quite complicated to implement. For example, if the Exposure needs to change the iris size, there is a downstream effect of altering the White Balance. All of the automatic functions are performed simultaneously with the image processing steps and are done on a frame by frame basis.

Camera Head Design Challenges

The image sensors and analog circuitry used in endoscopes have a low tolerance for power supply noise. While power is delivered to the camera head through a long cable from the CCU, the power within the camera head is regulated and filtered to maintain a stable, spike-free supply to the camera system. This power regulation must be designed carefully because voltage spikes occur naturally as current switches across the impedance of long cables. In a typical system, voltage spikes are mitigated by voltage regulation, using bulk capacitance of the Printed Circuit Board (PCB) and by adding additional bulk and bypass capacitors to the PCB. The added capacitance also helps reduce noise generated from local switching activity on the board such as from logic devices. However, in a small form-factor system like an endoscope camera head, there simply is not enough bulk capacitance on the PCB or enough space to add capacitors around the components.

The best solution to minimize power supply noise is to reduce the power consumed by logic devices in the camera head. This limits power spikes and the switching current across the power cable, thereby reducing local noise of the system. The benefits from reducing power are twofold; first, the cost and mechanical footprint are lowered; second, heat is minimized. Since power supplies for medical systems have uniquely stringent requirements for safety and quality that must be adhered to, increasing the system power increases the cost and complexity of the power supply design. The camera head has low heat dissipation capabilities, so lowering the power translates directly to lower heat within the camera head.

System designers have several options when choosing the central image processor in an endoscope camera head. One solution is to implement multiple ASSPs and/or DSP processors to support the functions; however, these types of implementations are not the most efficient use of PCB real estate. A single device solution is a better choice for two reasons. It has a much smaller PCB footprint compared to a multiple device solution, and it can offer improved manufacturing reliability since there is only one component to be assembled. The system designer must decide whether to implement an ASIC or an FPGA. The ASIC implementation has substantial NRE and design costs, which might not provide the return on investment needed to justify the costs for this implementation. FPGA technology provides the best cost and performance in a single device, low-power solution for developers of endoscope systems.

Camera Control Unit

The CCU receives image data from the camera head in RGB or YUV format through a DVI or SDI interface, and then performs any combination of processing steps to enhance the image quality. Dedicated image processing devices are typically used to deliver optimal image quality at high resolution with minimal lag.

A functional block diagram of a typical CCU is shown in Figure 3.

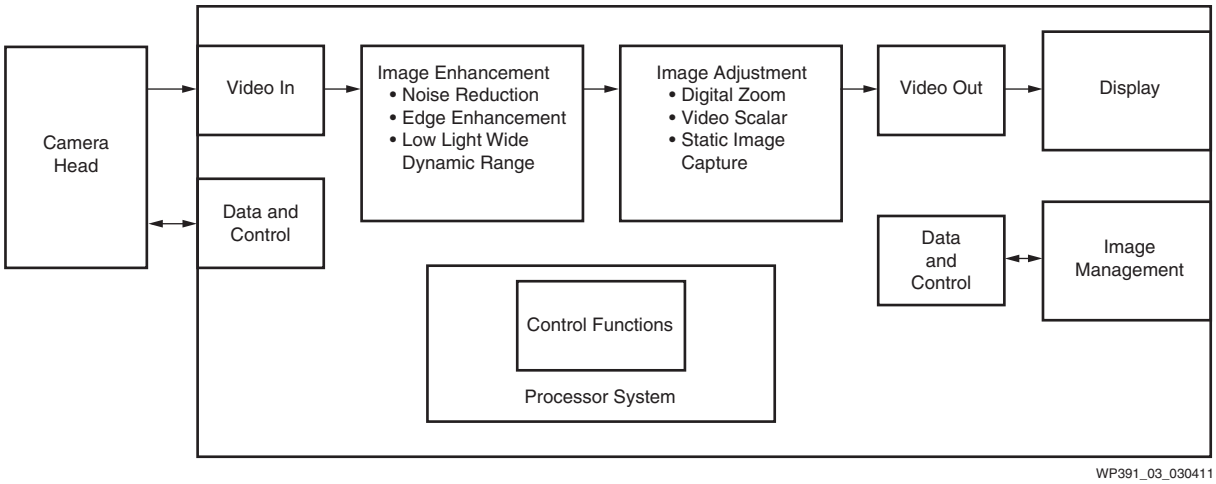

Figure 3: **CCU Functional Diagram**

The first stage of image enhancements typically includes:

- Noise reduction
- Edge enhancement
- Wide dynamic range correction

The image enhancement stage is followed by user-controlled image adjustments, which typically include:

- Digital zoom
- Video scaler
- Static image capture

A processor is often employed to manage data flow and to control the algorithms and functions of the CCU. It also can oversee communications to the camera head, the image management unit, and the display.

Noise Reduction

The best noise reduction algorithm to implement in a given endoscopy system is highly dependent on the specific application and the sensor quality. In general, endoscopy generates video of slow-moving objects, so high-speed motion noise is not a concern. However, it is still critical for video to be blur-free as motion blur can adversely affect the sharpness of subject tissue, making it difficult to perform an accurate diagnosis. High frame rate image sensors can help solve the problem of motion blur, but they do not solve the problem completely. Noise reduction algorithms are used in the CCU to add further improvement. In applications where small, low frame rate image sensors are employed, the noise reduction algorithm plays a key role in improving the image quality. Temporal, or motion-based noise reduction techniques, are often best suited for endoscopy applications where motion is a concern. In temporal filtering techniques, a noise model is created for individual pixels over time. Then a low pass filter is applied to eliminate rapid changes in pixels. These rapid changes are predominantly caused by motion, so by filtering them, only the slower-moving pixel changes related to the subject are allowed to pass, leaving a clean, blur-free image.

In applications where motion is less of a concern, such as in colonoscopy, or where a small, low resolution sensor is used, such as in cystoscopy, a spatial noise reduction technique can be employed. In spatial noise reduction, noise is detected and corrected

on a frame by frame basis. This technique can exasperate blur, so a hybrid spatial/temporal filter might be needed.

Edge Enhancement

Edge enhancement is an important image processing technique for endoscopes because it provides physicians a better view of the boundary of abnormalities in tissue. As an example, small blood vessels might be difficult to discern from surrounding tissue based on color alone. Edge enhancement might be required to generate a sharper view of the vessels so they can be further analyzed by the physician. Edge enhancement is also commonly used for improved viewing of tissue textures and the surface of mucous membranes.

A variety of edge enhancement technologies can be leveraged for endoscopy. Sobel operators and bilateral filters are two popular implementations. Many endoscopy system suppliers have developed proprietary enhancement techniques for specific applications. Most systems give the user control over the amount of filtering to provide, in the form of "low," "medium," and "high" settings.

Wide Dynamic Range Correction

A wide dynamic range (WDR) defines the ability of an imaging system to provide clear images when there is a wide range of luminance within each image. Since endoscopes often acquire imagery in a setting with a bright foreground and a dark background, WDR is an important characteristic of the system. High quality, low noise CCD or CMOS image sensors have the biggest impact on dynamic range and should be used whenever possible. However, many endoscopy applications use lenses that are constrained by other parameters such as physical size and resolution, so the sensors do not offer maximum dynamic range. In such cases, WDR processing algorithms become a critical component of the system. The closer the WDR processing block is to the sensor, the larger impact it has on the resultant image. Ideally, WDR is located in the camera head; however, to satisfy power and device density constraints in the camera head, the designer needs to consider locating the WDR processing in the CCU.

Digital Zoom

While some endoscopes include an optical zoom lens, many do not due to size restrictions. The ability to zoom is a valuable feature in endoscope systems that enables physicians to get a much closer view of the subject. Digital zoom increases the image size at the expense of resolution. If the native resolution of the video stream is high, the quality of the resulting zoom image can be acceptable. For lower resolution systems, interpolation filtering might be needed to improve the resolution.

Video Scaler

A video scaler is used to map a video stream to the appropriate aspect ratio and resolution for a receiving device. As shown in Figure 3, the CCU can output the video stream to both a local display and to the image management unit. The local display might be a much lower resolution and smaller aspect ratio than the native video format, so the video scaler adjusts the video accordingly for the display device and passes the video stream directly to the image management unit.

Static Image Capture

Static image capture is used by physicians to quickly capture and share an image of the subject tissue. The sensor control circuit built into some image sensors contains a static image capture circuit. In other systems, this function is typically performed downstream, after the image enhancement functions have been performed. The static image capture can be performed either in hardware or software, and the image is typically held in local memory until saved to disk by the physician.

Camera Control Unit Design Challenges

In endoscopic surgeries, physicians are often looking at imagery for hours at a time, so eye fatigue can become an issue. It is important to have high-speed image processing, which reduces video lag and achieves maximum frame rate, to deliver smooth video that minimizes eye fatigue and reduces the chance of injury to the patient due to lag between actual and perceived location of instruments. Some endoscopy systems, especially those used in critical applications such as surgery, can avoid using compression altogether due to the inherent lag that results from the calculation-intensive compression algorithms.

Endoscope suppliers often differentiate their products by the unique image enhancement functions that they implement in the CCU, and they are continually pushing the limits of processing capabilities to deliver new image enhancement techniques without sacrificing processing speed. Like most electronic systems, the CCU is also constrained by a power budget, time to market requirements, and by cost. When selecting the type of device to use for image processing in the CCU, it can be a difficult task to meet the performance requirements without sacrificing the other constraints.

Dedicated ASSPs and DSP processors tend to have a familiar design flow and short ramp up time, but do not typically offer the processing performance required and are limited in I/O options and count. An ASIC solution offers the performance needed—but limited volume and long redesign schedules make them an unattractive solution. The best balance between performance, cost, power, and shortened development cycles is achieved through the use of FPGAs as the main image processor. Furthermore, a very high-level of integration can be achieved with Xilinx FPGAs by integrating multiple interfaces into a single device to provide interface bridging, which reduces component count and lowers both cost and power of the system.

Image Management

In endoscopy systems, the image management unit is usually responsible for image file management, user interface, network connectivity, and other system management functions. It can also perform some post-processing image enhancement such as rotation, on-screen display (OSD), and picture-in-picture display. In compact systems, the image management functions can be incorporated as one unit with the CCU; in large systems, they can be a separate unit. The image management unit is typically a PC-style architecture, built around a processor system. It will likely include an operating system such as Windows or LINUX with a custom GUI for endoscopy. It can have multiple video inputs to simultaneously display images from different angles or different zoom levels. It can offer control with a mouse and keyboard and have its own monitor.

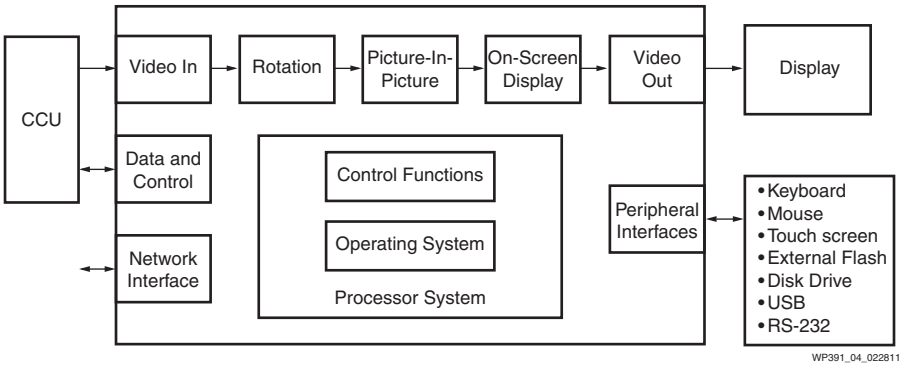

Figure 4: **Image Management Unit**

High-end systems, especially those incorporating high definition video, often offload the video interface and video processing to a Xilinx FPGA. In such a case, image rotation, picture-in-picture, on-screen display, and video receive and transmit are all handled in FPGA hardware, rather than in software on the processor. This architecture ensures that the video stream is processed only by high-performance logic, resulting in low-lag video that does not impact other processes running simultaneously in the processor. System designers can also leverage the FPGA's available high pin count and versatile I/O interface standards to implement data, network, storage, and user interfaces. This can help reduce overall component count for the system.

Light Source

The light source is used for illumination of the subject during endoscopic examinations and procedures. The light unit connects to the camera head via fiber-optic cables. The light is then transferred to the distal tip of the endoscope through another set of fiber optic cables. The light unit typically consists of either a xenon or Metal Halide bulb, and is predominantly built of power electronics. It also typically has a simple user interface with controls for brightness, power, and system status.

Some light sources might connect to the image management unit via Ethernet or other communication protocol so it can be controlled remotely by an operator using the image management interface. This interface must be real-time and must remain active even when the rest of the system is inactive, so it can wake up the light source on command. While multiple ASSPs can be used to implement each of the various functions, an FPGA offers a single device solution to perform all of the user interface and communication requirements. A small, low power FPGA, such as the Artix™-7 FPGA by Xilinx is well suited for managing the logic requirements in the light source with its optimized combination of low power consumption, high performance, and high degree of interconnect versatility.

Display

The final component of an endoscopy system is the display monitor. Displays are a key component that can influence diagnostic accuracy in endoscopy systems. Medical displays have a few unique requirements over commercial displays, so they are typically purpose-built. Some of the key requirements include: excellent gray scale and black level performance, factory and on-site calibration, communication with a PC for diagnostics and calibration, ability to tile multiple monitors together to display a single image, image enhancement for long cable lengths, anti-glare, low reflection,

and support for multiple, simultaneous inputs. The display monitor is an important component that, like other medical devices, must conform to stringent medical safety and quality criteria. It can connect to the CCU or the image management unit. It is also common to have multiple display monitors for a single system, where one or multiple display monitors are connected to the CCU for viewing by physicians and assistants, and another is connected to the image management unit for viewing or control by others.

The architecture of the display electronics is similar to a consumer monitor, and a typical block diagram is shown in Figure 5.

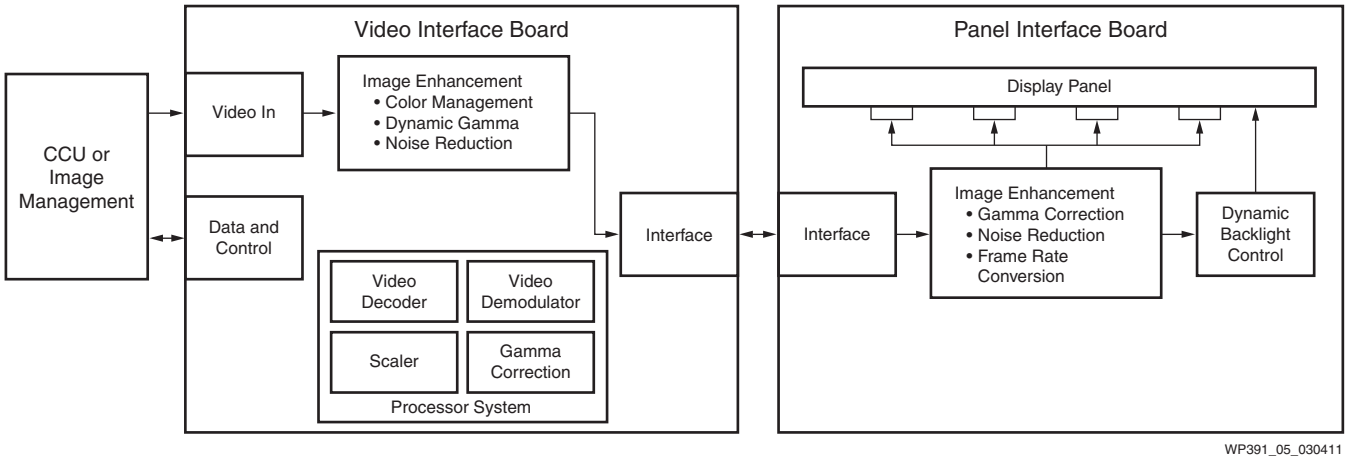

Figure 5: **Medical Display Block Diagram**

Several different technology solutions can fulfill the logic requirements of display monitors. ASICs, microprocessors, DSP processors, ASSPs, and FPGAs are all capable of performing many of the functions. However, only FPGAs are able to provide a cost effective, fast time-to-market, scalable solution that can be used across a product line. They also are capable of supporting the wide array of interface standards found within displays and are capable of performing the required image enhancement, gamma correction, and noise reduction processing functions, making them an excellent fit.

Power Consumption

Reducing power consumption is a major design constraint for endoscopy systems. In medical systems, this requirement stems from uniquely stringent requirements for safety and quality that must be adhered to. To remain within safety and quality constraints, the cost and complexity of the power supply design can increase greatly as the demand for added power increases. System designers continually strive to adopt new technology and design techniques that keep power consumption at a minimum without sacrificing performance.

Heat is another major factor driving the reduction of power consumption. When semiconductors containing an enormous amount of system gates are clocked at high frequency, they generate heat that has to be rapidly removed from the system to keep the temperature of components within the desired operating range. To expel this heat, heat sinks, fans, packaging, and the PCB must be carefully designed. The heat management system adds to the overall weight, size, and cost of the system, and the use of increasing fan speeds adds to the power consumption.

Interfaces

Endoscope systems use many different types of logic devices to handle the various interconnect and processing tasks. Each of these devices has different interface requirements, creating the need for a versatile interconnect solution. However, the interconnect solution must also be high performance due to high demand for increasing bandwidth throughout the system. The high bandwidth requirement is due to high resolution image sensors, large displays, and the need to pass serial data between system components through cabling. The combination of requirements for versatility and high bandwidth places an enormous burden on the I/O count and throughput between devices and the system components. Most of the microprocessors, ASSPs, and DSP processors available do not offer enough I/Os for parallel interfaces and do not directly support many of the interfaces found in endoscope systems such as PCIe®, USB, and serial transceiver data transfers used for SDI and chip-to-chip communication. Figure 6 shows common interfaces used in endoscope systems.

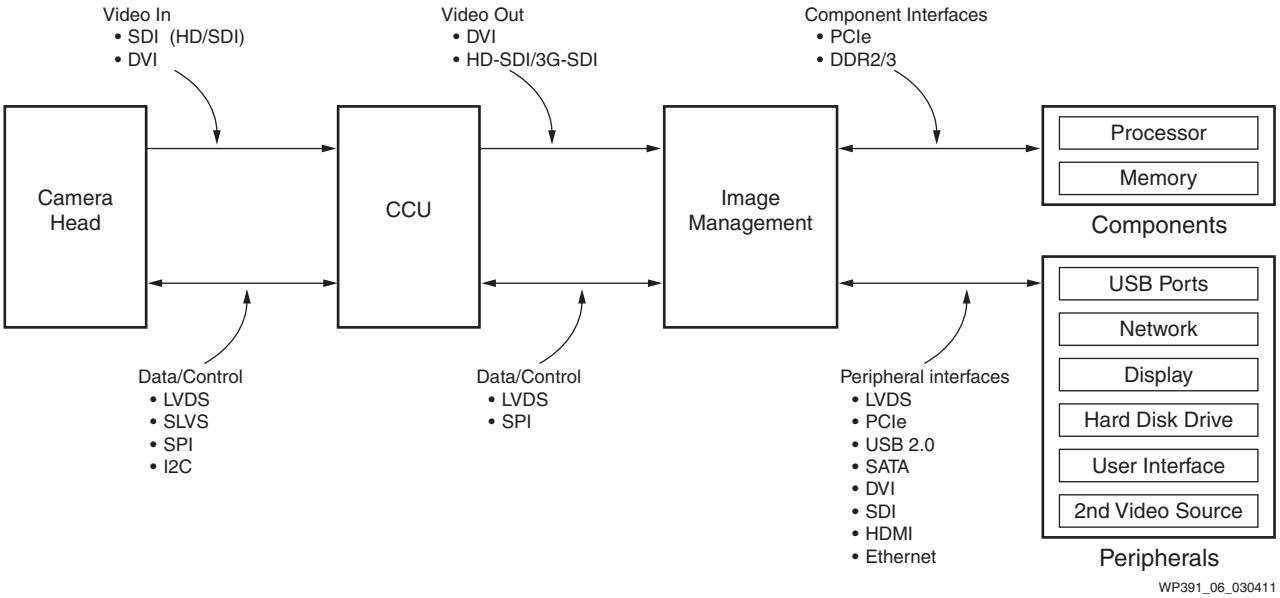

Figure 6: **Common Interfaces in Endoscope Systems**

System architects are left with few choices to address this interface complexity. They can select discrete components for each interface, build a custom ASIC, or use FPGAs. ASICs tend to be too expensive for endoscopes. FPGAs offer the highest I/O count and support most interface standards for a reasonable price. Therefore, they are commonly used to handle interface challenges throughout an endoscope system. Depending on the size of the FPGA being used, system architects might decide it is more cost effective to use dedicated interface devices for the most complex functions such as USB.

Xilinx FPGAs in Endoscopes

An FPGA is a multipurpose silicon device that enables designers to integrate multiple system functions in a single device. It is a collection of configurable memory, DSP, and I/Os that are tightly integrated with a large array of logic cells, built on leading-edge process technology. This single device system integration greatly reduces the need for challenging and expensive physical PCB-level connectivity.

A Xilinx FPGA is more than just a silicon device though. It represents a design ecosystem that is packaged with design tools and a comprehensive IP library to help users create their designs quickly. Since the silicon is designed by Xilinx, there are no NRE mask or production costs for the system designer, who only has to create the design, download the design file to the device, and then the device is configured for that specific design.

Power

High power requirements increase the cost, form factor, and noise of an endoscope system, while impacting reliability and performance. Xilinx has produced high performance, power optimized FPGAs, which are ideally suited for endoscope camera heads, CCUs, and displays.

Xilinx achieves an excellent economy of scale by providing a product line that spans many customers' applications. This economy of scale is unmatched by other types of logic products, so it enables Xilinx to lead the adoption of advanced semiconductor process technologies. By utilizing the latest process, Xilinx offers an excellent balance of power, performance, cost, and features. Xilinx brings customers the ability to migrate their silicon to the next generation process technology easily by continuing to push technology node advancements with every product family.

Xilinx works closely with semiconductor fabrication partners to develop a variety of transistor sizes that can be used opportunistically across the product line and within each device. This approach ensures that system designers experience extremely high performance with substantially reduced power compared to other FPGAs at the same process node. In addition, high-speed DSP blocks are able to maintain Xilinx's performance leadership by leveraging dedicated high-performance processing slices. Xilinx FPGAs also provide the localized memory and logic resources to achieve the performance requirements for endoscope applications. That, coupled with embedded processing, standardized I/O, and a proven ecosystem of soft IP, brings customers a path to reducing risk, cost, and schedule when developing their products.

To easily achieve the lowest possible power consumption in the 7 series FPGAs, several advanced design optimization techniques have been simplified. A low power device option enables the use of a low power supply voltage, which reduces standby power by 26%, giving a 50% improvement over previous generation FPGAs. Power optimization tools, such as automatic clock gating, reduce dynamic power by an additional 30%, while best-in-class power analysis tools help design engineers pinpoint power inefficiencies in their design so they can implement significant power saving design techniques.

More information and resources supporting Xilinx's low power advantage can be found at the Power Solutions Resource Center:

http://www.xilinx.com/products/design_resources/power_central

Cost Savings with Scalable Design

Xilinx 7 series FPGAs use nearly identical logic architectures across the Artix-7, Kintex™-7, and Virtex®-7 product families. This enables IP portability across devices, so that system designers can scale their designs up or down to efficiently address their entire product line with a single base design. In endoscope systems, this can be particularly valuable because there is often proprietary image processing IP or functionality that is used for different systems with different feature sets and image resolutions. Xilinx's common device architecture provides system designers with a large cost and time savings over the re-coding time that is typically required to port RTL from one FPGA architecture to another.

Intellectual Property

Xilinx Intellectual Property (IP) cores are key building blocks for Xilinx designs. An extensive catalog of general purpose cores is available to address the general needs of FPGA designers as well as robust domain- and market-specific cores to address requirements found in DSP, embedded, and connectivity designs. Many of the key DSP functions and connectivity interfaces found in endoscope systems are available as direct or partner IP cores throughout Xilinx's extensive partner ecosystem. Using Xilinx ecosystem IP minimizes development schedules and enables system designers to focus on the differentiating aspects of the design rather than developing standard functions—a distinct advantage with Xilinx.

Refer to Xilinx's IP Center for more information:
http://www.xilinx.com/ipcenter/

Refer to Xilinx's video and image processing IP for more information:
http://www.xilinx.com/ipcenter/video/video_core_listing.htm

Design Platforms

Xilinx has created a variety of Targeted Design Platforms (TDPs) that enable system designers to evaluate Xilinx FPGAs in specific applications and for specific functions. The combination of hardware, reference designs, and development tools integrated into the TDPs provides customers with the ability to start differentiating their product from the very beginning. The market-specific TDP kits provide additional market-specific applications to help system designers evaluate IP, demonstrate product implementations, and develop advanced algorithms. One such market-specific TDP kit is the Spartan®-6 FPGA Industrial Video Kit (IVK), which gives system designers an out- of-the-box video processing system to use during the development of display and camera applications. The IVK leverages Xilinx's image processing pipeline (iPipe) to perform image pre-processing functions, so system designers can focus their efforts on developing their own high-value, proprietary algorithms. The IVK is well suited as a starting point for endoscope system development.

Some of Xilinx's relevant TDPs include:

- Connectivity Design Platform:
  http://www.xilinx.com/technology/connectivity.htm
  - High-speed serial/parallel protocols
  - PCIe x8 Gen2
  - High-performance DMA
- DSP Design Platform:
  http://www.xilinx.com/technology/dsp.htm
  - Optimized IP library
  - High-level DSP design tools
- Embedded Platform:
  http://www.xilinx.com/technology/embedded.htm
  - Out-of-the-box software development
  - AXI4 interconnect support
  - Automatic BSP generation
- Industrial Video Processing Kit:
  http://www.xilinx.com/products/devkits/AES-S6IVK-LX150T-G.htm
  - CMOS image sensor
  - DVI/HDMI in/out
  - Image processing and enhancement pipeline

Selecting the Right Xilinx Device

Xilinx offers an array of devices with varying feature sets, logic densities, package options, and power-performance trade-offs. While this wide selection gives users the opportunity to find a perfectly optimized product for their application, it also can be a challenge to compare and contrast the multitude of parameters that define the optimal part. To help system designers select the best product for their implementation, Table 1 provides initial guidance for the product selection process along with some suggested devices.

Table 1: **Xilinx Device Selection for Endoscope Systems**

	Camera Head		CCU		Image Management		Display	
Criteria	Low power, small form-factor, low density, SDI/DVI support		High DSP performance, medium power, mid density, high pin count, SDI/DVI, DDR2/3		High pin count, mid-density, medium power, PCIe, SDI/DVI, 10/100 Ethernet		Low power, low density, good DSP performance, on-chip RAM.	
Product Family	Spartan-6 Virtex-6	7 Series	Spartan-6 Virtex-6	7 Series	Spartan-6 Virtex-6	7 Series	Spartan-6 Virtex-6	7 Series
Recommended Devices	XC6SLX16 -CPG196 (no SDI), XC6SLX25T (SDI)	XC7A20 (no SDI) XC7K30T (SDI)	XC6VLX365T XC6VLX130T	Two XC7K325T	XC6VLX130T XC6VLX130T	XC7K160T XC7A175T	Three XC6SLX25	Three XC7A20
Advantages	8 x 8 mm package, low power	Lowest power Artix or higher performance Kintex devices	Balanced power and performance	Higher density, improved performance, lower power	Balanced power and performance	Lowest power Artix and high performance Kintex devices	Balanced power and performance	Lowest power Artix device

Summary

FPGAs are an excellent fit for endoscope systems, where small form-factor, low power, and high performance are critical. Xilinx Spartan-6, Virtex-6, and 7 series FPGAs offer the performance of ASICs with the added benefits of low NRE cost, substantially reduced time to market, scalable design, and high I/O count. In addition, Xilinx's custom low-power process, coupled with leading edge power optimization tools, offer significantly lower power consumption than competing solutions. All of these benefits enable endoscope system developers to improve patient care by rapidly deploying systems that deliver the latest technology within budget and power consumption constraints.

For additional information on Xilinx's medical solutions, please visit:
http://www.xilinx.com/esp/ind_sci_med/medical.htm

Available Resources

Xilinx Medical Solutions:
http://www.xilinx.com/esp/ind_sci_med/medical.htm

Xilinx 7 Series FPGAs
http://www.xilinx.com/technology/roadmap/7-series-fpgas.htm

Xilinx Targeted Design Platforms:
http://www.xilinx.com/products/targeted_design_platforms.htm

Xilinx Industrial Video Kit:
http://www.xilinx.com/products/devkits/AES-S6IVK-LX150T-G.htm

Connectivity Design Platform:
http://www.xilinx.com/technology/connectivity.htm

DSP Design Platform:
http://www.xilinx.com/technology/dsp.htm

Embedded Platform:
http://www.xilinx.com/technology/embedded.htm

Xilinx IP Center:
http://www.xilinx.com/ipcenter

Xilinx Video IP:
http://www.xilinx.com/ipcenter/video/video_core_listing.htm

- Camera Head:
  - Gamma Correction:
    http://www.xilinx.com/products/ipcenter/EF-DI-GAMMA.htm
  - Color Correction Matrix:
    http://www.xilinx.com/products/ipcenter/EF-DI-CCM.htm
  - RGB to YCrCb Color-Space Converter:
    http://www.xilinx.com/products/ipcenter/RGB_to_YCrCb.htm
  - YCrCb to RGB Color-Space Converter:
    http://www.xilinx.com/products/ipcenter/YCrCb_to_RGB.htm
  - Color Filter Array Interpolation:
    http://www.xilinx.com/products/ipcenter/EF-DI-CFA.htm
  - Defective Pixel Correction:
    http://www.xilinx.com/products/ipcenter/EF-DI-DEF-PIX-CORR.htm
  - Image Statistics Engine:
    http://www.xilinx.com/products/ipcenter/EF-DI-IMG-STATS.htm

    - Image Characterization:
      http://www.xilinx.com/products/ipcenter/EF-DI-IMG-CHAR.htm
- CCU and Image Management:
    - Video Scaler:
      http://www.xilinx.com/products/ipcenter/EF-DI-VID-SCALER.htm
    - Video Timing Controller:
      http://www.xilinx.com/products/ipcenter/EF-DI-VID-TIMING.htm
    - Motion Adaptive (Temporal) Noise Reduction:
      http://www.xilinx.com/products/ipcenter/EF-DI-IMG-MA-NOISE.htm
    - Noise Reduction:
      http://www.xilinx.com/products/ipcenter/EF-DI-IMG-NOISE.htm
    - On-Screen Display:
      http://www.xilinx.com/products/ipcenter/EF-DI-OSD.htm
    - Video Edge Enhancement:
      http://www.xilinx.com/products/ipcenter/EF-DI-IMG-ENHANCE.htm
    - Video DMA Core:
      http://www.xilinx.com/products/ipcenter/EF-DI-VID-DMA.htm

Power Solutions Resource Center:
http://www.xilinx.com/products/design_resources/power_central

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
03/21/11	1.0	Initial Xilinx release.

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