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Multi-Gigabit Serial Link Simulation with Xilinx 7 Series FPGA GTX Transceiver IBIS-AMI Models

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The 7 series GTX transceiver is the first 28 nm transceiver in the FPGA industry. The transceiver supports line rates from 500 Mb/s to 12.5 Gb/s. To enable fast high-speed serial link simulation and accurate link margin estimation, Xilinx provides an IBIS-AMI model kit for the 7 series GTX transceiver. The features and the quality of this IBIS-AMI model kit are the subject of this white paper.

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Introduction to High-Speed Serial Link Simulation

The high-technology industries have been transitioning from parallel to serial interfaces, and the data rates required of high-speed serial interfaces have been steadily increasing. These higher data rates have produced higher bandwidths, along with associated challenges for system design. Data recovery from a received serial data stream is negatively impacted by channel loss, reflections, crosstalk, etc. Overall, the complicated channel conditions that exist at 10 Gb/s and higher raise the importance of serial link simulation to a newly critical position.

Meanwhile, the cost of simulation, like simulation time, rises as the transceiver circuits incorporate more and more complicated equalization features. Classic time-domain transient simulations based on multi-gigabit transceiver transistor netlists have reached a stage where simulation time is intolerably long, even for the fastest workstations.

Over the past few years, therefore, the IBIS Algorithmic Modeling Interface (IBIS-AMI) has become the industry standard for transceiver simulation, with ~1,000X faster time-domain simulation speeds while maintaining a high-level of accuracy.

IBIS-AMI

Developed by the IBIS Advanced Technology Modeling (IBIS-ATM) working group, the IBIS-AMI is a modeling standard for transceivers to enable fast and accurate simulation of multi-gigabit serial links. Semiconductor vendors provide IBIS-AMI models as compiled binary executables without exposing their proprietary algorithms. The models are portable through different EDA platforms. Multi-million bits of simulation can be done in minutes, thus making it practical to run low Bit-Error-Rate (BER) channel analysis.

An IBIS-AMI simulation starts with analyzing the analog network and generating the impulse response characteristics of the transmitter and receiver analog buffers, the packages, and the link channel between transmitter and receiver, as illustrated in Figure 1.

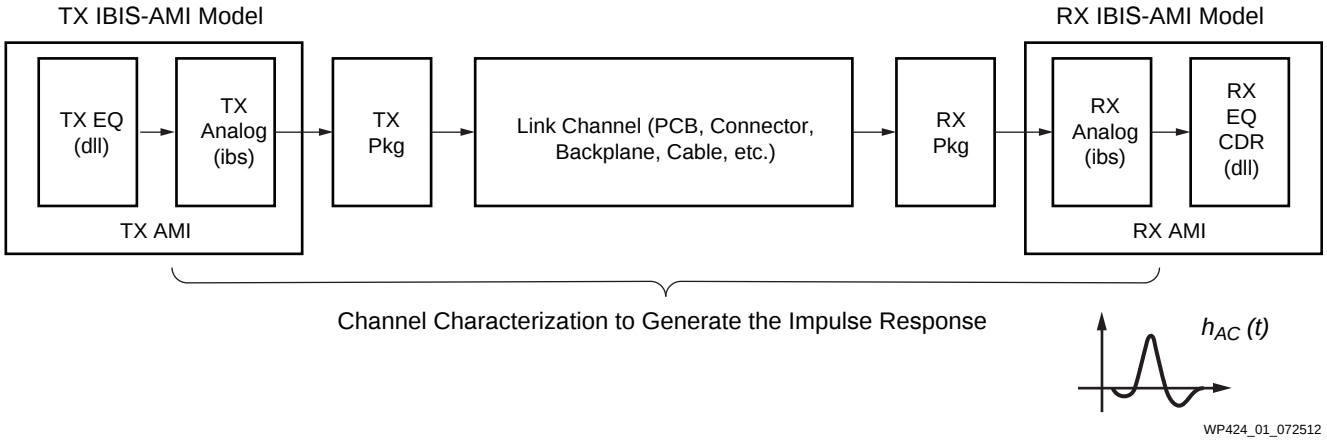

Figure 1: **Building Blocks of an IBIS-AMI Simulation and Channel Characterization**

The EDA tool calls Tx_Init() and Rx_Init() with the characterized channel impulse response to generate a system impulse response. To run a bit-by-bit simulation, the EDA tool takes the stimulus through Tx_GetWave(), system response, and

Rx_GetWave(), then outputs the behavior of the overall system. The Init() and GetWave() calls are all defined in the executables of the AMI models. See Figure 2.

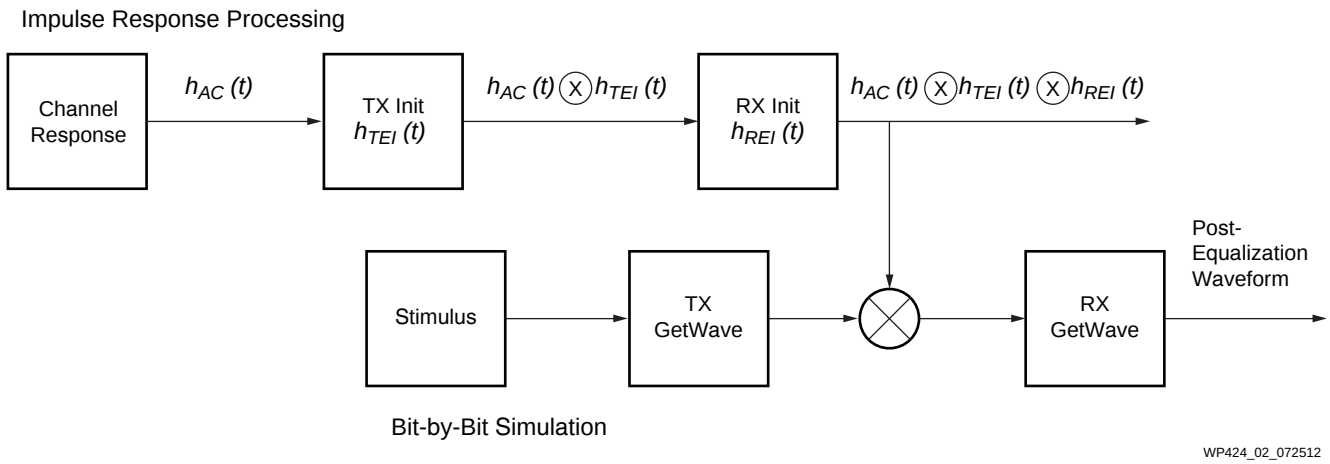

Figure 2: **IBIS-AMI Simulation Flow**

7 Series Transceiver IBIS-AMI Modeling Overview

With 7 series FPGAs, Xilinx offers a portfolio of four transceivers (Figure 3) to meet different application requirements, running from 500 Mb/s to 28.05 Gb/s. As a member of the IBIS Advanced Technology Modeling Group, Xilinx provides an IBIS-AMI model for each transceiver, which enables customers to run serial link simulation and estimate system performance.

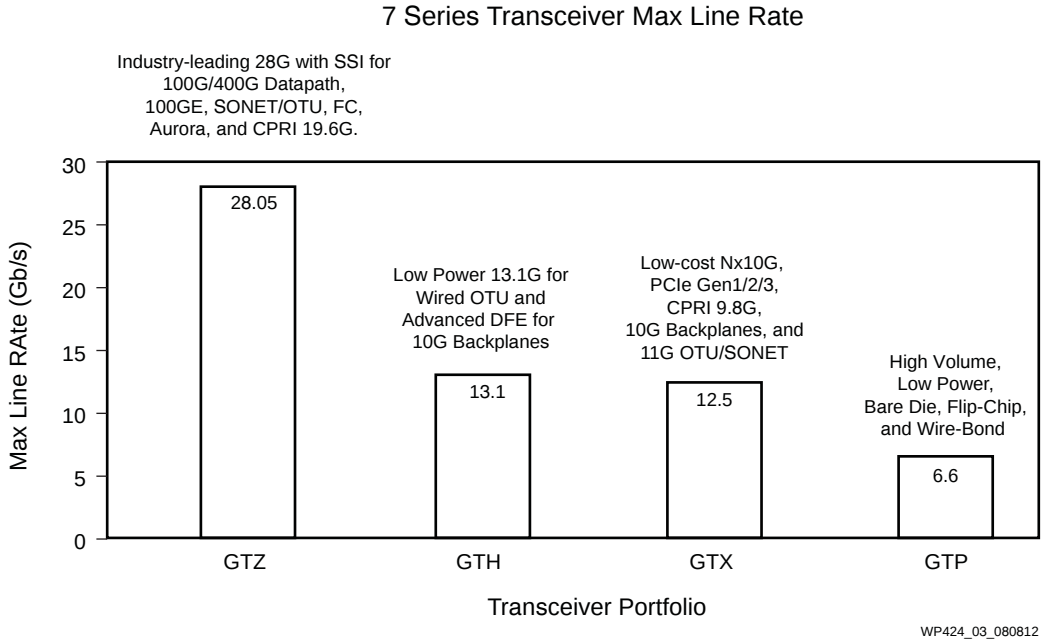

Figure 3: **Xilinx 7 Series FPGA Transceiver Portfolio**

The 7 series GTX transceiver is the first of four 7 series transceivers available to the market. It is designed for best-in-class signal integrity. Figure 4 describes the blocks dedicated to achieving excellent signal integrity in the Kintex™-7/Virtex®-7 GTX transceiver in DFE mode. All the shaded blocks — PLL, TX pre-emphasis, RX Automatic Gain Control (AGC), RX Linear Equalization (EQ), RX Decision Feedback

Equalization (DFE), RX Clock Data Recovery (CDR), and Adaptation block — are modeled in the GTX transceiver IBIS-AMI model kit. The generic packages for both transmitter and receiver are also provided in the model kit.

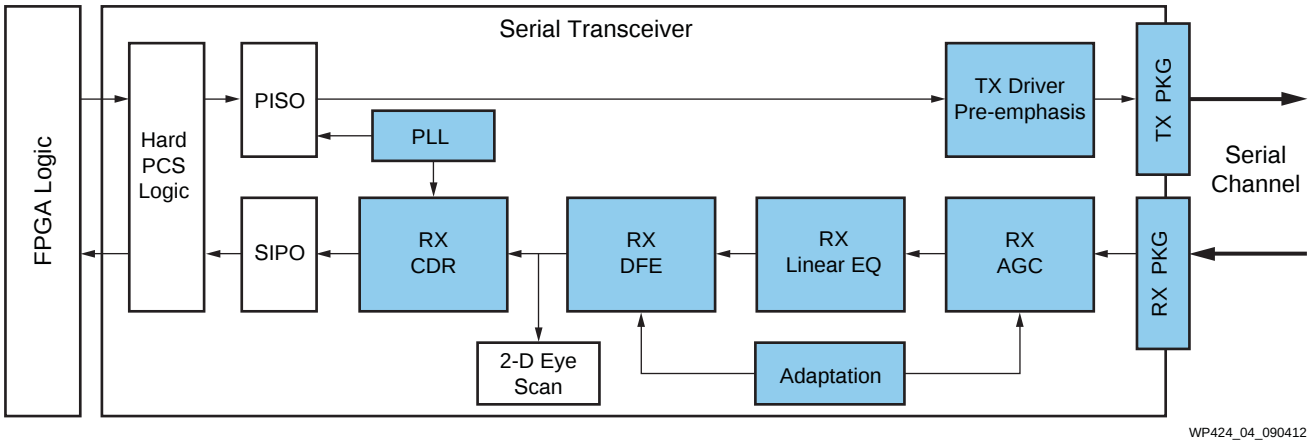

Figure 4: **7 Series GTX Transceiver Blocks for Signal Integrity**

IBIS-AMI Features in 7 Series Transceiver Models

IBIS-AMI Model Transportability

The IBIS-AMI provides a standard mechanism for modeling transceivers. The models developed based on this standard must be able to run on any IBIS-AMI compatible EDA platform. The 7 series GTX transceiver IBIS-AMI model is fully compatible with the IBIS 5.0 standard. As part of the model release process, the transceiver models have been verified with different EDA tools that support IBIS-AMI simulations. Table 1 lists, in alphabetic order, the EDA tools with which the GTX transceiver IBIS-AMI model has been verified.

Table 1: **7 Series GTX Transceiver EDA Tool Compatibility**

EDA Tool	Compatible
Agilent Advanced Design System	Yes
Mentor Graphics HyperLynx	Yes
Sigrity SystemSI	Yes
SiSoft Quantum Channel Designer	Yes

Figure 5 is a sample simulation setup provided in the GTX transceiver IBIS-AMI model kit. Figure 6 through Figure 9 show the statistical simulation results from four different EDA tools running this setup at 8 Gb/s.

The four tools used are Agilent ADS 2011.01, Mentor Graphics HyperLynx 8.2, Sigrity SystemSI 12.0, and SiSoft QCD 2011.11.

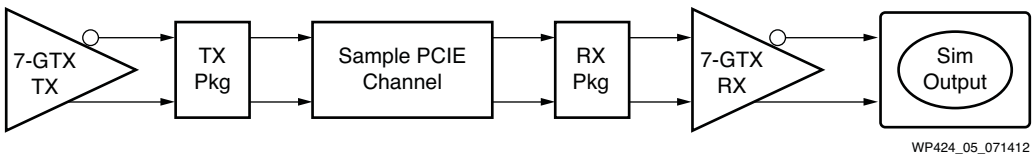

Figure 5: **Sample GTX Transceiver Measurement Setup**

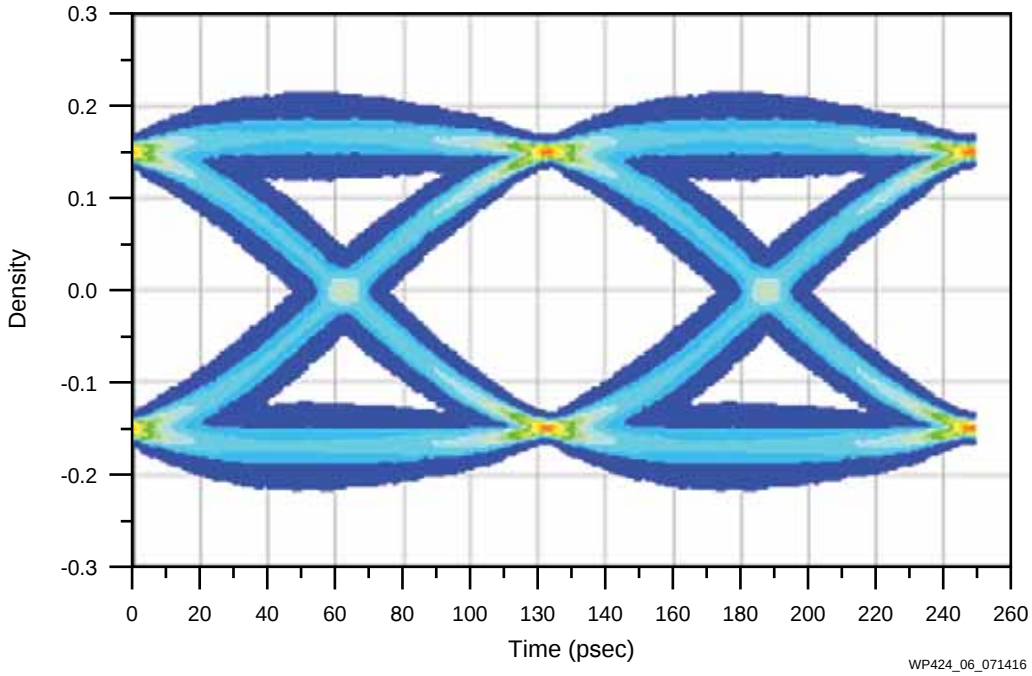

Figure 6: **GTX Transceiver Statistical Simulation Result (Agilent ADS 2011.01)**

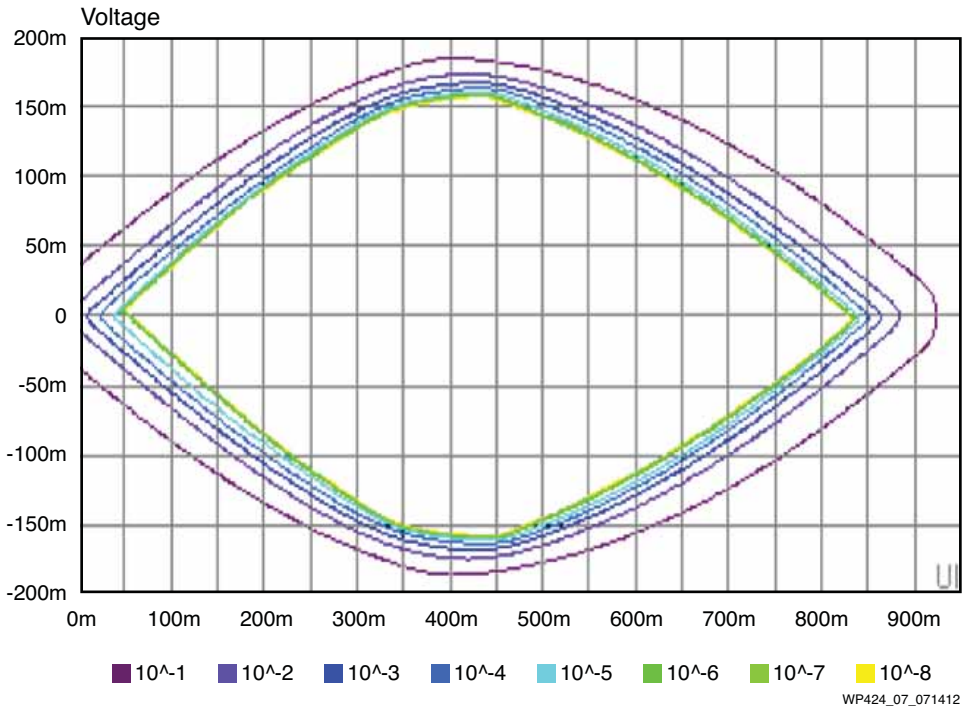

Figure 7: **GTX Transceiver Statistical Simulation Result (Mentor Graphics HyperLynx 8.2)**

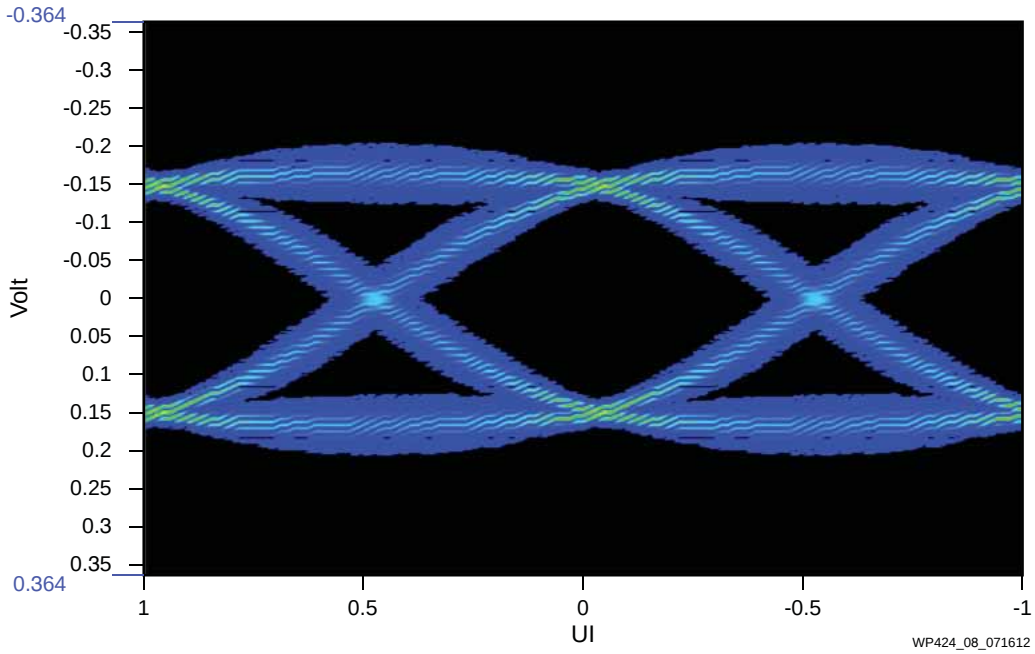

Figure 8: **GTX Transceiver Statistical Simulation Result (Sigrity SystemSI 12.0)**

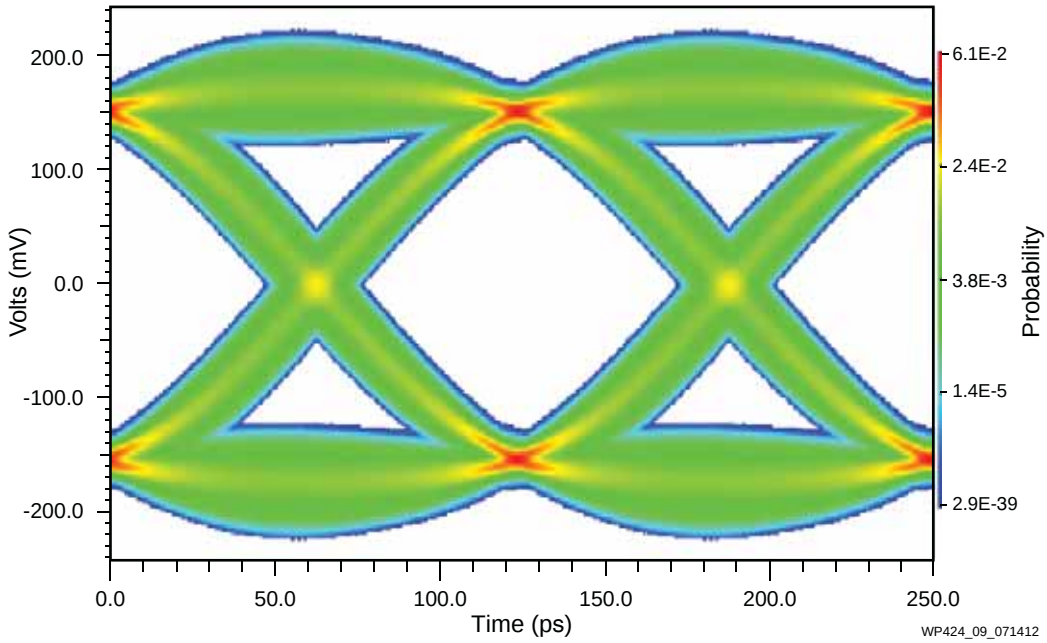

Figure 9: **GTX Transceiver Statistical Simulation Result (SiSoft Quantum Channel Designer 2011.11)**

7 Series GTX Transceiver IBIS-AMI Model Flexibility

Two modes of simulation are supported by the IBIS-AMI standard: statistical analysis and time domain simulation.

Statistical analysis makes the assumption that TX/RX equalization is both linear and time invariant. It uses the impulse response and applies the respective equalization to derive the statistical eye for the serial link. Statistical analysis is faster than a time-domain simulation and well suited to exploring a large design space.

Time-domain simulation uses a waveform instead of impulse response during the simulation. It allows nonlinear and/or time-varying effects in the TX or RX IP to be represented, and it supports detailed modeling of the clock data recovery (CDR). The clock information from the CDR is used to generate the eye diagram post equalization. Time-domain analysis is well suited to detailed analysis of specific stimulus patterns or conditions.

7 series transceiver models support both statistical analysis and time-domain simulation. Figure 10 to Figure 13 are the time-domain simulation results with the setup described in Figure 5, page 4.

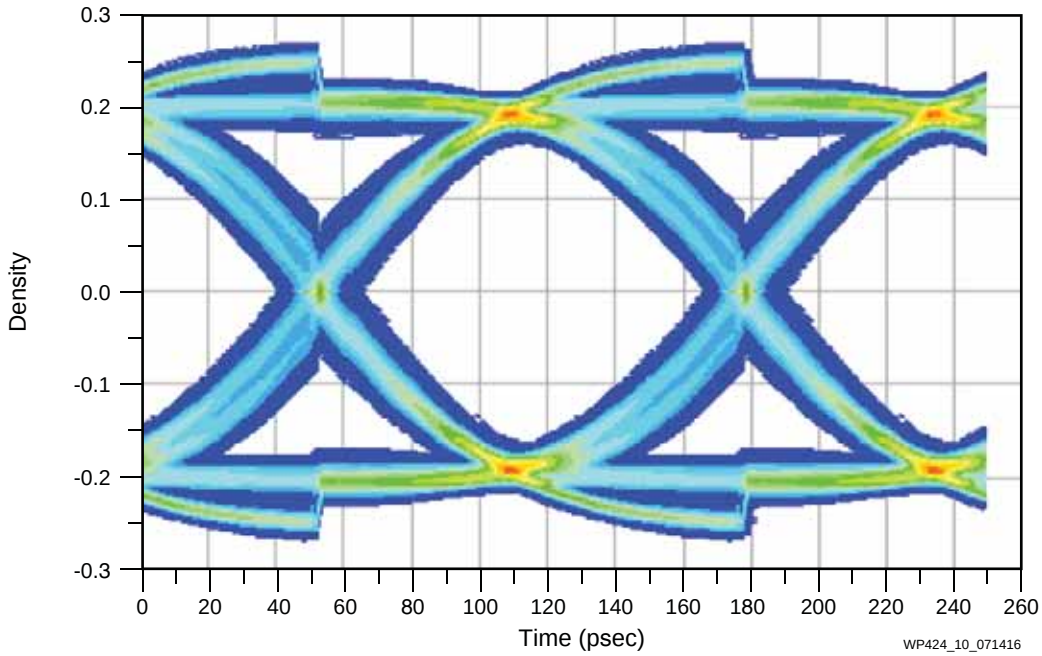

Figure 10: **Sample GTX Transceiver Time-Domain Simulation Result (Agilent ADS 2011.01)**

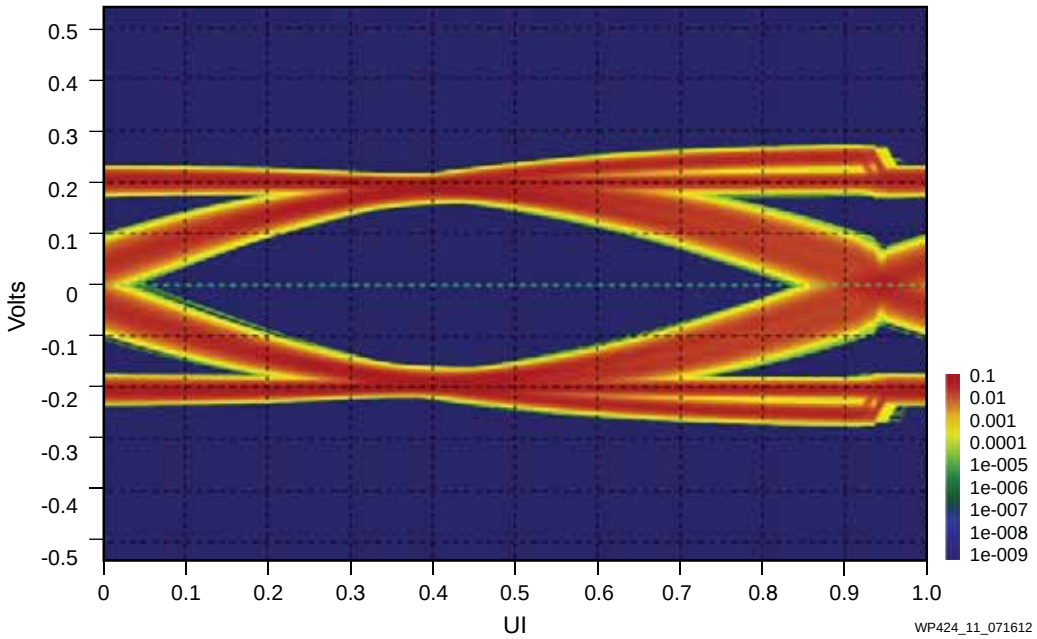

Figure 11: **Sample GTX Transceiver Time-Domain Simulation Result (Mentor Graphics HyperLynx 8.2)**

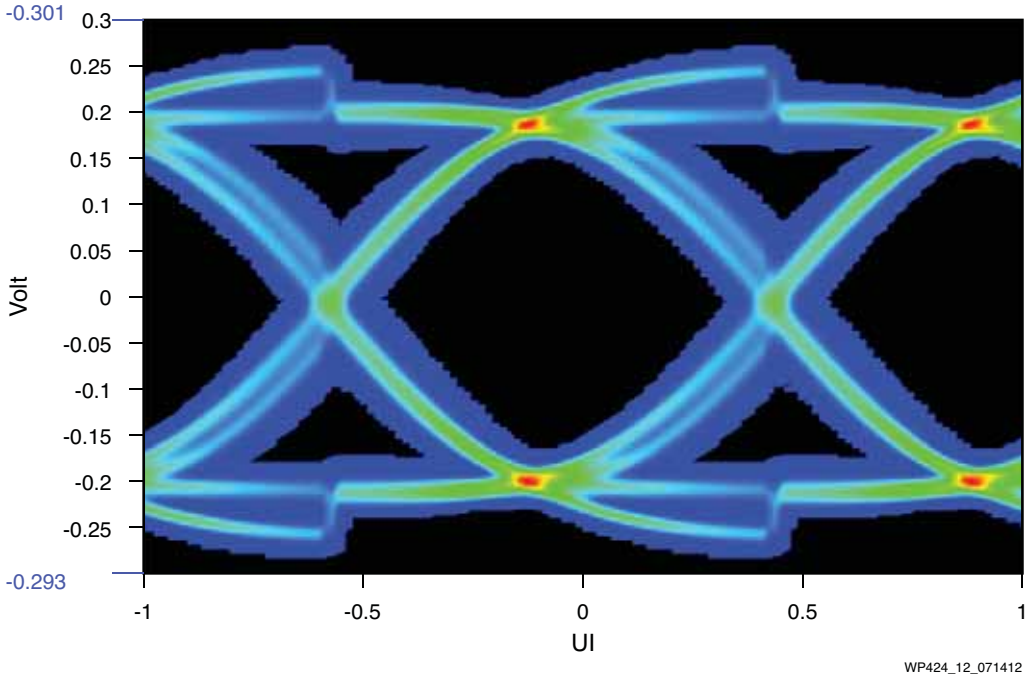

Figure 12: **Sample GTX Transceiver Time-Domain Simulation Result (Sigrity SystemSI 12.0)**

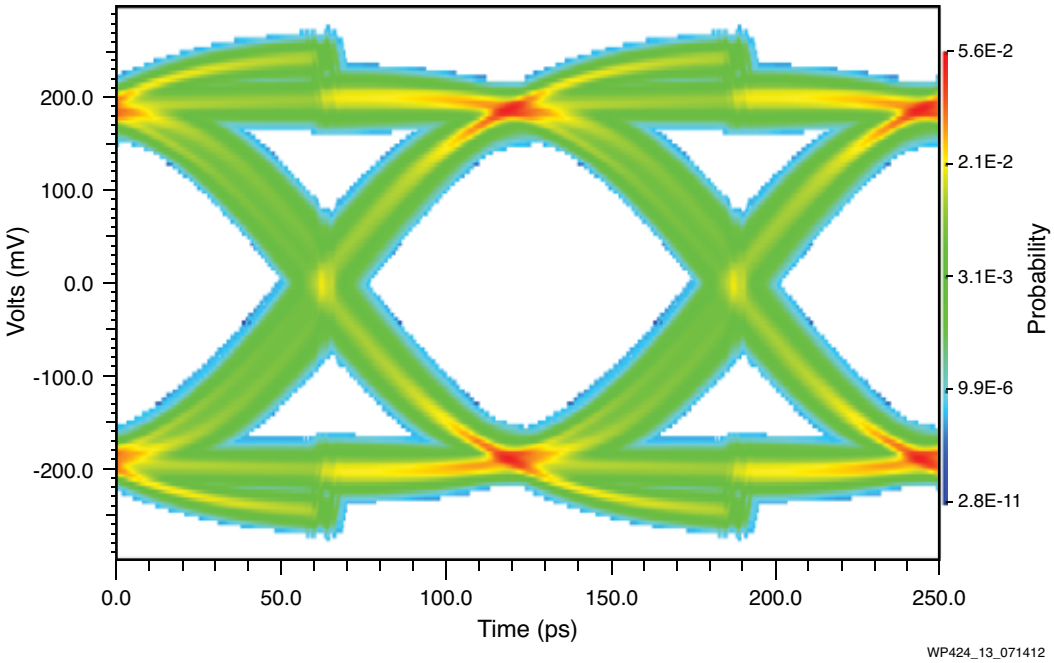

Figure 13: **Sample GTX Transceiver Time-Domain Simulation Result (SiSoft Quantum Channel Designer 2011.11)**

7 Series GTX Transceiver IBIS-AMI Model Usability

The IBIS-AMI models allow users to customize the settings of the transmitter and receivers do meet different channel conditions, as well as process/voltage/temperature variations.

7 series GTX transceiver IBIS-AMI model covers different signal integrity blocks in the transceiver. The same algorithm used to architect the transceiver is also implemented in the IBIS-AMI model. The same control parameters (listed in UG476, *7 Series FPGAs GTX/GTH Transceivers User Guides*) available on the 7 series transceiver silicon are also available in the IBIS-AMI model. The match between the simulation parameters and the silicon parameters ensures the easy transformation of simulation setup to silicon setup, or vice-versa.

Table 2 shows transmitter parameters that are available in the IBIS-AMI model and described in UG476, *7 Series FPGAs GTX/GTH Transceivers User Guides*. In Figure 14, parts (a) and (b) show the waveform differences created by adjusting the TXPOSTCURSOR parameters.

There are parameters only available in the IBIS-AMI models. For example, the process parameter to select the process/voltage/temperature (PVT) corner is only available for simulations. Exploring different PVT corners can ensure the system is stable under different conditions.

Table 2: **Sample Control Parameters in GTX Transceiver Receiver IBIS-AMI Models**

Parameter Name	Tunable Bits	Description
TXDIFFCTRL	[3:0]	Adjust transmitter output amplitude swing. There are 16 settings represented by 16 codes. The swing level for each code could vary with the process corner selection. The minimum output swing (differential peak-to-peak) is ~230 mV (code `0000`); the maximum swing is ~1,280 mV (code `1111`). Default = `4'b1111`
TXPRECURSOR	[4:0]	Adjust transmitter pre-cursor emphasis. Default = `5'b00000`
TXPOSTCURSOR	[4:0]	Adjust transmitter post-cursor emphasis. Default = `5'b00000`

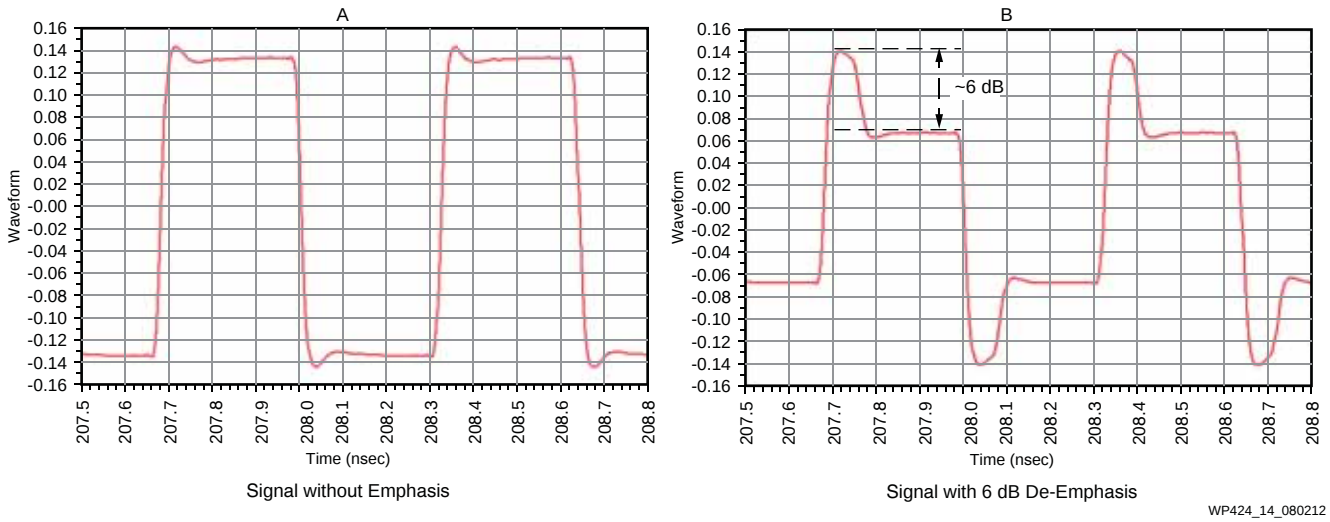

Figure 14: **Sample GTX Transceiver TX Waveforms with Different Post-Tap Settings**

7 Series GTX Transceiver IBIS-AMI Model Accuracy

The main reason to move from traditional SPICE simulation to IBIS-AMI is the simulation time. While the speed of SPICE simulation makes it impractical to run system analysis, accuracy close to that of the SPICE simulation is an important goal of IBIS-AMI model development. Correlation with the SPICE simulation is always a significant milestone—one that the 7 series GTX transceiver IBIS-AMI model has achieved.

The same algorithms used to architect the transceiver blocks are implemented in the IBIS-AMI models. This simplifies the tuning process to correlate the behavior of the IBIS-AMI model with the behavior of the circuits.

In Figure 15, parts (a) and (b) show comparisons of GTX transceiver receiver simulation eye-diagrams, with part (a) from IBIS-AMI simulations and part (b) from HSPICE models. Figure 16 is the time-domain representation of the two simulations, which produce virtually identical waveforms. The simulations were running at 12.5 Gb/s with TT corner. As shown in both Figure 15 and Figure 16, the IBIS-AMI and HSPICE simulations correlate with a high degree of exactness.

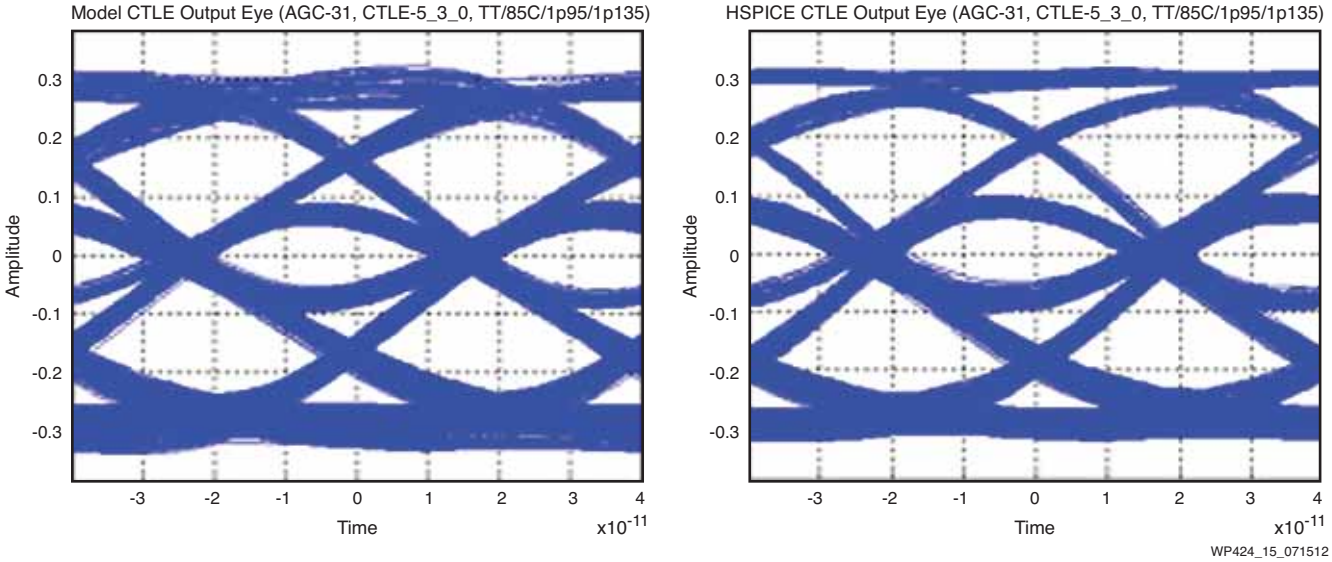

Figure 15: **Model CTLE Output Eye (AGC-31, CTLE-5_3_0, TT/85C/p95/1p135)**

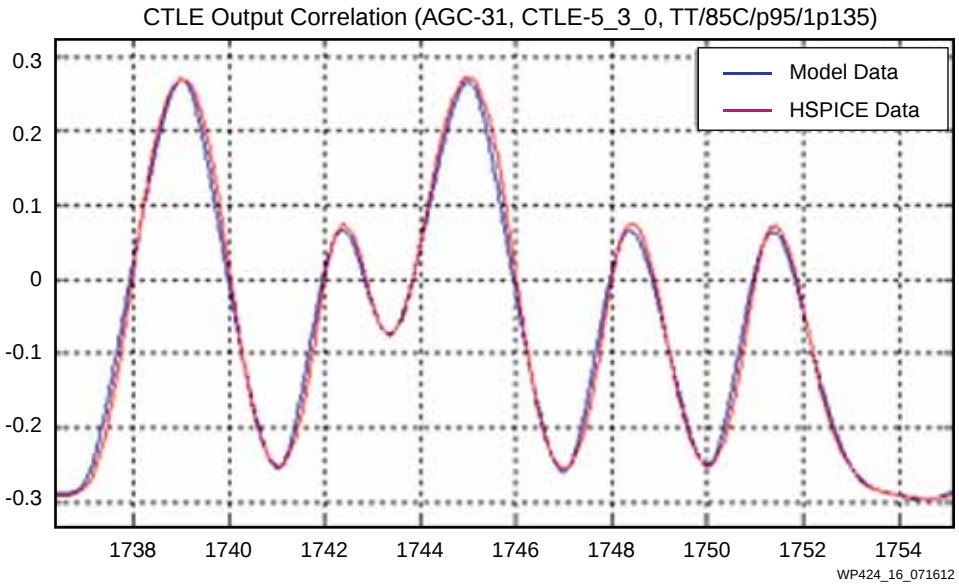

Figure 16: **Time Domain CTLE Output Correlation Waveform (AGC-31, CTLE-5_3_0, TT/85C/p95/1p135)**

The GTX transceiver IBIS-AMI models have been correlated against SPICE simulations in hundreds of cases to cover different data rates, different equalization settings, and different PVT corners. Figure 15 and Figure 16 show only one sample of these correlation case results.The eye width and eye height of the simulation results are used as the main metrics to quantify the correlation. Figure 17 and Figure 18 show histograms of the correlation data on eye height and eye width, respectively. With ~500 valid data points, eye width correlates to well within 7%, and eye height correlates to well within 10%, with one outlier at 11.71%.

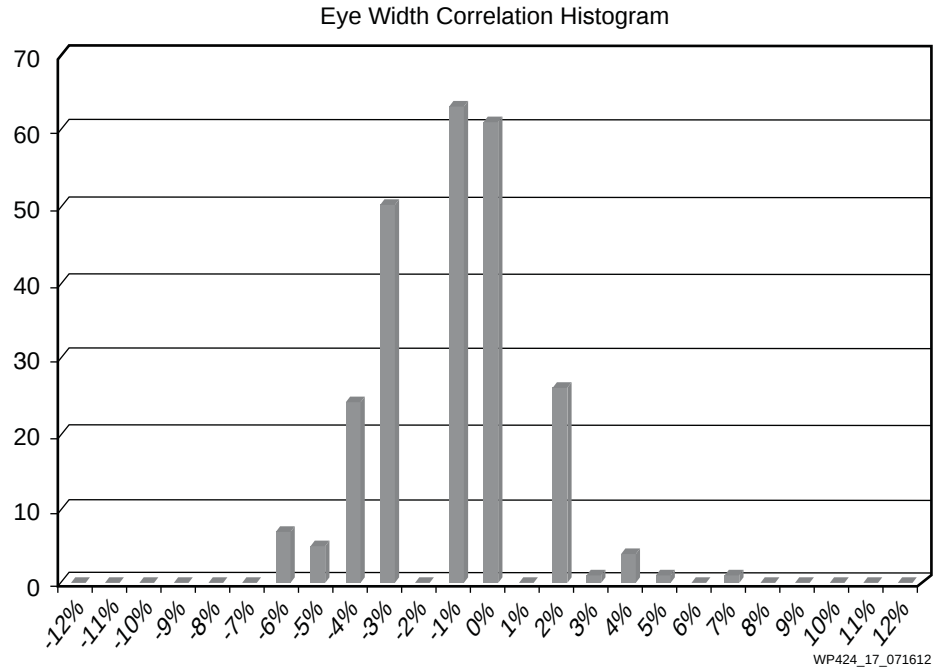

Figure 17: **Eye Width Histogram for GTX Transceiver IBIS-AMI and HSPICE Correlation**

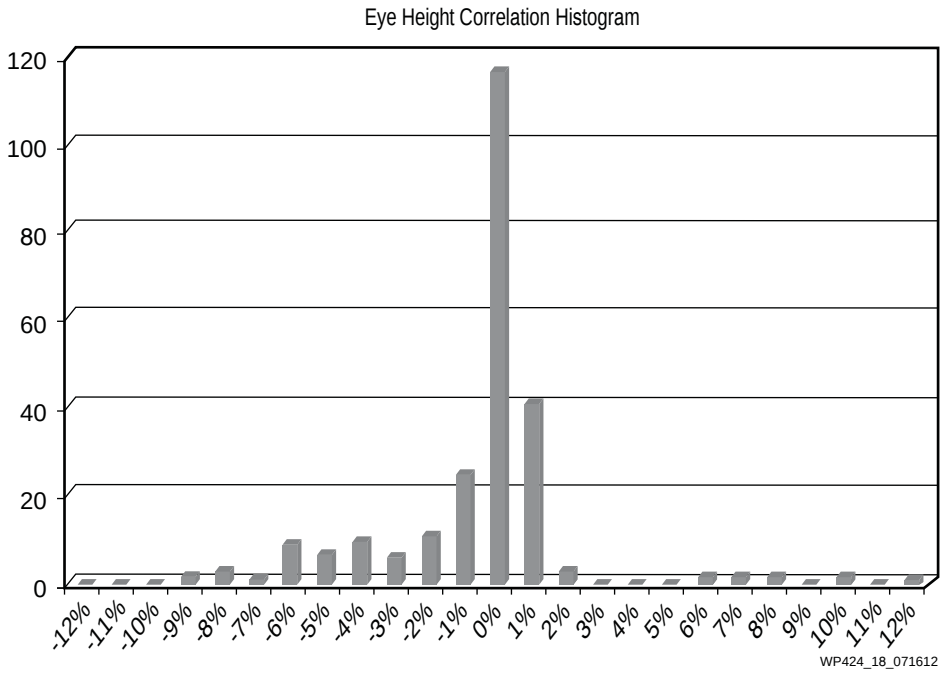

Figure 18: **Eye Height Histogram for GTX Transceiver IBIS-AMI and HSPICE Correlation**

Conclusion

The 7 series FPGAs include a portfolio of four transceivers that covers different application needs with unrivalled signal integrity features. To enable channel analysis of the serial links with the transceivers, Xilinx continues to supporting IBIS-AMI models for high-speed transceivers.

The 7 series GTX IBIS-AMI model is fully compatible with IBIS 5.0. It has been verified with four industry-leading EDA platforms. Both statistical analysis and time-domain simulation are supported. Customers can manually adjust the transceiver settings to meet different channel conditions, or rely on the auto-adaptation features in the receiver to tune the transceivers. The model is well correlated with SPICE models. It provides an portable, fast, and accurate solution for link margin estimation on multi-gig serial links.

The currently released IBIS-AMI model and the correlation reports can be requested through Xilinx FAEs or I/O specialists.

For additional information, visit the Transceiver section on xilinx.com: http://www.xilinx.com/products/technology/transceivers/index.htm.

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
09/28/12	1.0	Initial Xilinx release.

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