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Understanding and Mitigating System-Level ESD and EOS Events in Xilinx 7 Series Devices

By: James Karp, Michael Hart, and Tc Chai

The semiconductor industry's scaling trend known as "Moore's Law" leads to a reduction in integrated circuit component-level electrostatic discharge (ESD) immunity, and consequently to exposure to board-level/system-level ESD and electrical overstress (EOS) events. Xilinx 7 series devices use the most advanced 28 nm technology generation and hence are subject to this trend.

This white paper describes the relationship between FPGA component-level ESD and system-level EOS, and provides industry-standard roadmaps and references. Customer responsibilities are clearly specified, and some recommended customer-side approaches to EOS avoidance and mitigation are described.

Introduction

The scaling trend of the semiconductor industry, “Moore’s Law,” leads to a reduction in integrated circuit component-level ESD immunity. In previous technology generations, a high level of integrated circuit (IC) component ESD immunity was often able to protect against low-level system ESD and EOS events. Only high system-level ESD and EOS events were able to damage a Xilinx device installed on a board. Such events were usually readily recognized and eliminated. For advanced technology nodes, 28 nm and beyond, the component-level ESD immunity is 50% less compared to previous generations.

Each package pin of a Xilinx device has on-chip ESD protection elements. Power and ground pins have the strongest ESD protection, while TX and RX SerDes pins are the most vulnerable. These state-of-the-art high-speed I/Os are designed with the smallest transistors available at the given technology node. Their ESD protection is carefully optimized with respect to I/O performance; as a result, they have *just enough margin* to pass a component-level ESD qualification for all package/silicon variants.

Per the ESD Association, which establishes ANSI-recognized standards for managing ESD in manufacturing and in the electronics industry: “While significant progress has been made over the past decades in the design, handling, and application of electromagnetic-compatible (EMC) and ESD-protected electronic devices, progress has been less than ideal in the minimization of EOS of such devices. The Industry Council has recognized this deficiency and has decided to write a white paper on EOS to help the industry understand the root causes of EOS and minimize it in electronic devices.”[Ref 1]

Along these same lines, this Xilinx white paper aims to educate and help Xilinx customers anticipate increasing system ESD and EOS event sensitivity, and to develop adequate procedures to minimize them.

EOS/ESD Definitions

Electrostatic Discharge (ESD) is a sudden transfer of charge between objects at different potentials. The charge is generated by triboelectrification or electrostatic induction. Device survival of an ESD event is defined at two different levels:

Component-Level ESD Immunity is the ability of an IC to survive ESD events related to IC package contact with any object. Events could be the result of human touch, placement in or removal from a storage tray, pick-up or drop-off by a robotic handler arm, placement in or removal from a tester socket, etc.

System-Level ESD Immunity is the ability of an IC *mounted on a board* to survive ESD events caused by contacts of the board with any object. Such events could come from a cable, human touch, physical placement of the board onto a metallic surface, etc. System ESD events often can be an order of magnitude higher than component-level events. By definition, then, the *minimum* system-level ESD immunity of a device is the same as its component-level ESD immunity.

Electrical Overstress (EOS) is defined as operation of a device outside its absolute maximum ratings (AMR).[Ref 2] EOS can cause damage, malfunction, or accelerated aging leading to early failure of the device.

The scope of this white paper includes ESD and EOS as they relate to Xilinx devices of the current 28 nm generation. The information described herein is also relevant to

advanced integrated circuits other than FPGAs and SoCs; component ESD and system-level EOS should be addressed for *all* parts of a system.

EOS/ESD Ownership

Xilinx is responsible for the shipment of devices (both FPGAs and SoCs) that meet the Xilinx component-level ESD specification.

Customers are responsible for safely handling these devices in compliance with the Xilinx component-level ESD specification.

Once a Xilinx device is mounted on a system board, the customer must establish its own specification for system-level ESD and must implement the measures necessary to meet this specification.

Customer EOS board design and protection must be sufficient to prevent Xilinx devices from exceeding their published absolute maximum ratings.

Component-Level ESD Roadmap

Component-level ESD is traditionally evaluated in accordance with the Human Body Model (HBM) [Ref 3] and the Charged Device Model (CDM) [Ref 4]. The practical threat of an HBM event is significantly alleviated in FPGAs and SoCs because of their close pin spacing and because of the much-reduced incidence of human handling in a typical manufacturing flow. In contrast, CDM has become the primary real-world ESD event, describing electrostatic charging of the FPGA and its rapid discharge during automated handling, manufacturing, and assembly.

One of many examples is a device sliding down a shipping tube (charging) and hitting a metal surface (discharging). The discharge current is limited only by the parasitic impedance and capacitance of the device.

Figure 1 illustrates both HBM and CDM events.

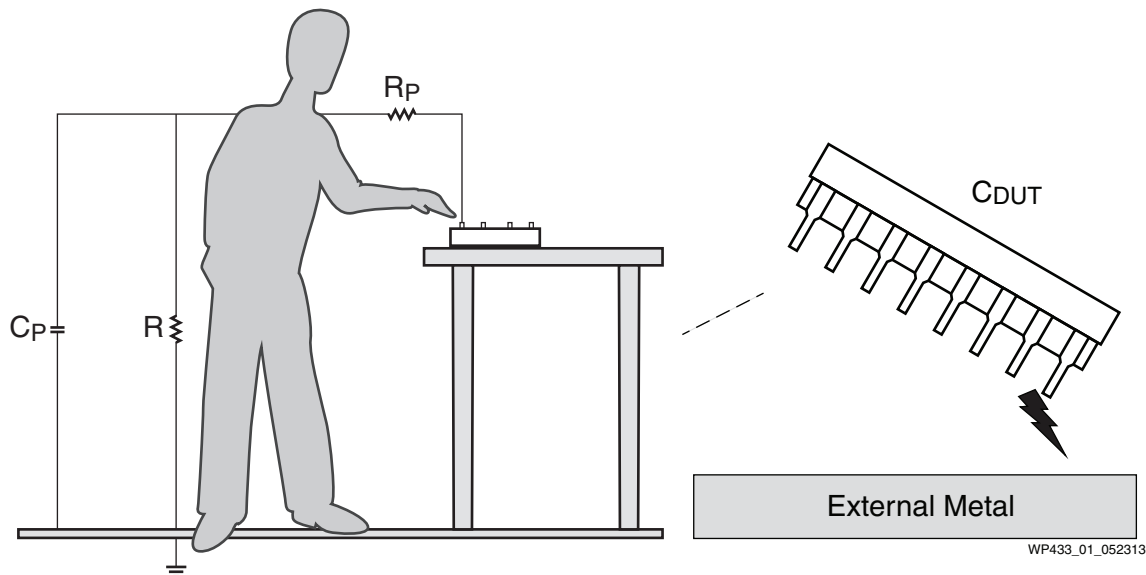


Figure 1: HBM and CDM ESD Events

The roadmap for ESD (associated with the ITRS Roadmap for Semiconductors) projects severe restrictions on achievable HBM and CDM ESD levels. [Ref 5][Ref 6] Constraints from circuit design requirements (such as higher frequencies used by SerDes and RF devices) can eventually reduce practical ESD HBM design levels to the 500V range. Similarly, the CDM level might be reduced to the 100V range.

Note: Machine Model (MM) scaling is not included in this white paper because many in the industry now consider the MM requirement, with the exception of a very few limited applications, to no longer be valid; indeed, there is a strong industry drive to eliminate it from mainstream IC manufacturing ESD specifications.

For users, the trend of lowering component-level ESD immunity means that ESD control in the production flow is absolutely necessary, and that CDM ESD control at the factory must be critically improved.

Figure 2 shows a CDM roadmap that illustrates the evolution of CDM target voltage levels since approximately 1980 as IC process dimensions steadily decreased in accord with Moore’s Law.

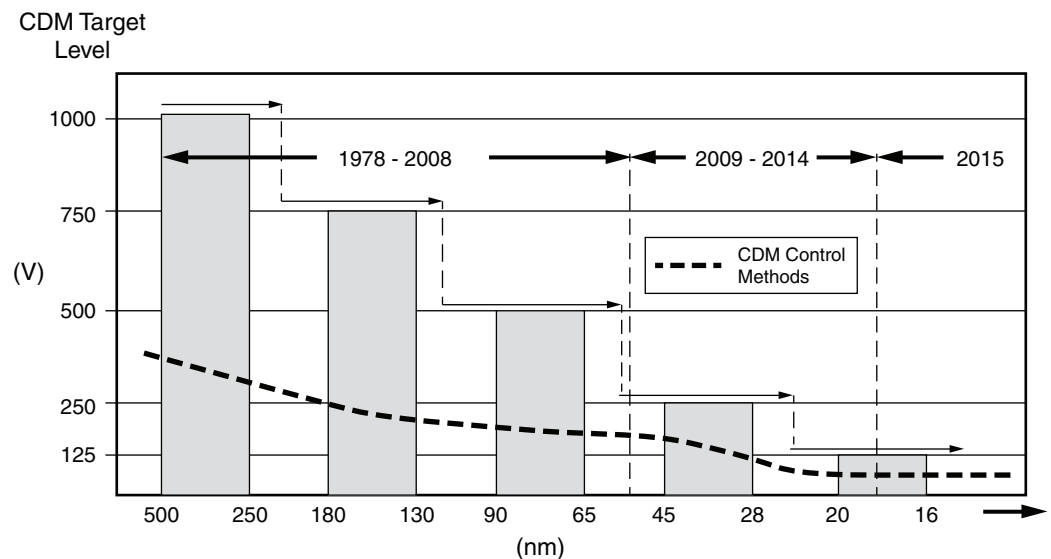


Figure 2: CDM Roadmap

System-Level ESD

After the FPGA or SoC is mounted onto the board, its on-chip ESD elements are still present in the system, but their ESD protection capability is far below that of ESD events the device can be exposed to on the board. HBM and CDM models are still applicable at board level, yet they must be considered as an indication of “two point” discharge (similar to HBM) or “one point” discharge (similar to CDM). A few examples of the most damaging system-level ESD events are described in [Charged Board Event \(CBE\)](#), [Cable Discharge Event \(CDE\)](#), and [Ionizer-Related Discharge Event](#) sections.

Charged Board Event (CBE)

CBE to a printed circuit board (PCB) is equivalent to CDM to the IC. CBE is the discharge of accumulated static charges from a PCB when it makes contact with a metal surface during board assembly or manufacturing. A PCB (as well as the ICs mounted on it) can become statically charged when the PCB is transported during the assembly process — for example, on a conveyor belt. Static discharge then happens when the PCB comes into contact with a metal surface, damaging the IC on the board.

Cable Discharge Event (CDE)

Cables can be triboelectrically charged when removed from a bag or dragged across another material. A low-voltage ESD generated when the charged cable is plugged in can produce a CDE. The electrical signal produced by connecting charged cables to a system connector can cause data corruption and soft failures as well as damage to the external pins of ICs.

Ionizer-Related Discharge Event

Ionizers are primarily used for the reduction of particles and of damaging static potentials in ESD-controlled work areas. One drawback, however, is that ionizers can actually induce charging, due to ion polarity imbalance with voltage-type instruments or to polarity imbalance referred to as space charging.

Some ESD events — for example, CBEs and CDEs, can be misdiagnosed as power-induced electrical overstress, which is described in the [Electrical Overstress](#) section.

Electrical Overstress

An FPGA or SoC on a board can be exposed to electrical overstress (EOS).[\[Ref 2\]](#)

Typical characteristics of EOS events:

- Their duration is longer than an ESD event (i.e., 1 μ s or longer)
- EOS signal levels are typically much lower than ESD events
- EOS signals can be of any type: AC, DC, EMI, transients, and so forth. Unlike ESD, EOS signals are often periodic and/or continuous.

EOS signals deliver significant amounts of energy to devices, and damage is often manifested as massive meltdown. A device in the PCB assembly process can also experience EOS during soldering or board test. A recently-formed EOS Group within ESDA Standards is working on a document that describes EOS.[\[Ref 1\]](#)

EOS due to misapplication can destroy an FPGA or SoC by breaking down its internal elements and melting the on-chip metallization. Most of these issues are due to severe voltage over/under shoots caused by:

- Hot switching of relays (for example, connecting power to a pin through a relay when the power supply is on and programmed to the desired voltage)
- Improper power sequencing
- Improper force/sense connections
- Poor board design for high dI/dt events
- Poorly chosen bias levels for continuity testing (for example, milliamperes of current forced in test)
- Hot-plugged test cables

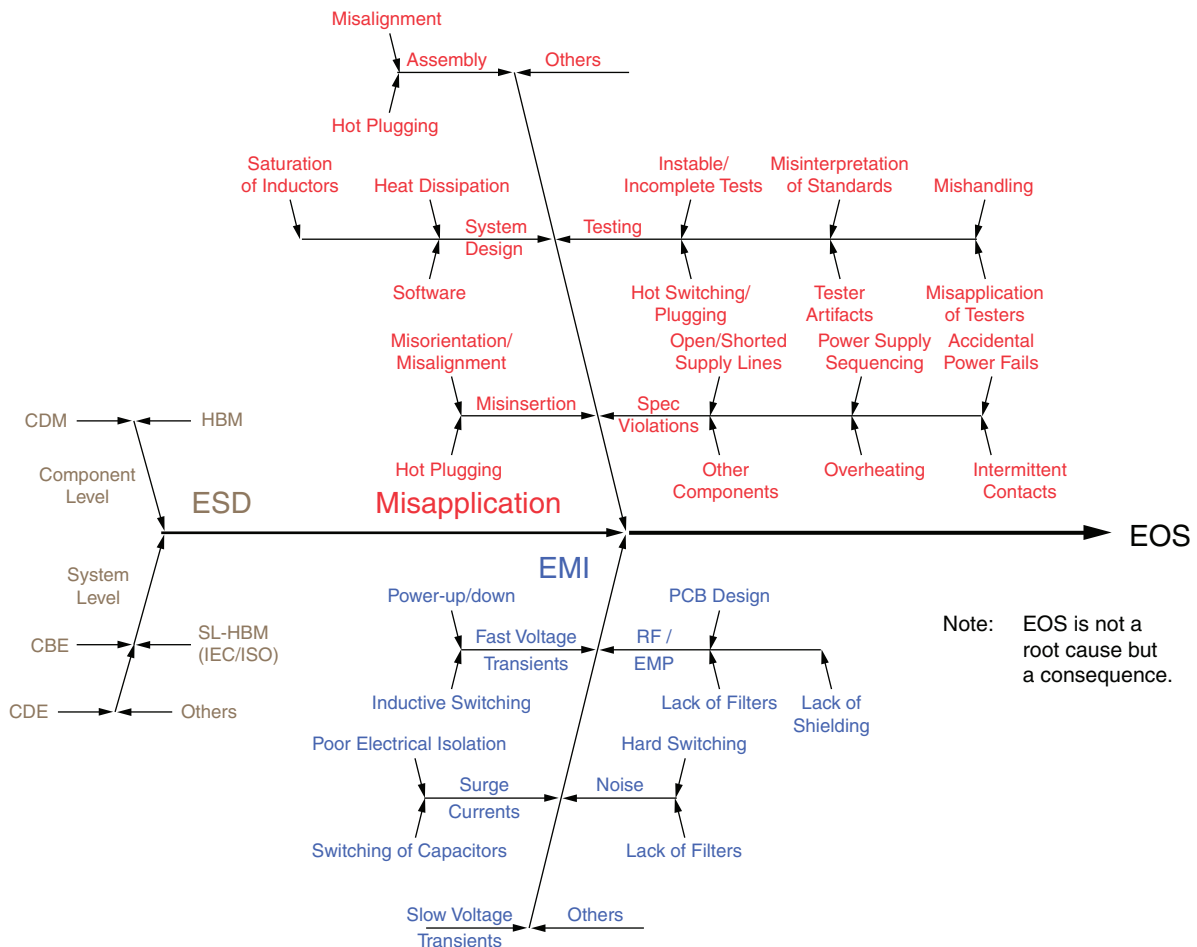
EOS due to electromagnetic interference (EMI) on ground lines is often caused by low-voltage DC motors or other circuits that draw large currents on startup. To minimize the effect of EMI, a robust grounding concept, including filters, is essential. High-level negative EMI can trigger transient latch-up and destroy the devices.

Mitigation: System-Level ESD and EOS

Practically all Xilinx customers have ESD programs implemented at the component level. However, component-level ESD mitigation does not always protect the FPGA or SoC after it has been mounted onto the system board. This white paper aims to facilitate awareness of system-level ESD and EOS events.

Despite the industry trend towards reduction in component-level ESD immunity for advanced technologies of the 28 nm generation and beyond (driven primarily by increasing performance specifications), Xilinx has not only preserved but actually increased the ESD immunity of power pins. Typically, the HBM level of power pins was and is 3 kV, and CDM is about 400-500V or higher. At the same time, I/O pins must be addressed; their ESD protection level is lower, with an HBM specification of 1 kV and a CDM of 200V or less.

See Figure 3 for a component and system ESD/EOS fishbone diagram that shows examples of conditions or events that can cause electrical failures.



Source: Kaschani and Gaertner, 2011 EOS/ESD Symposium and ESDA EOS TR

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Figure 3: Component and System ESD/EOS Fishbone Diagram

Summary

EOS and system-level ESD events are major causes of electrical failures, both in the factory and in the field. The industry trend is towards reduction of ESD/EOS immunity for 28 nm generations and beyond. ESD/EOS damage cannot be undone; thus, the only cure is prevention. The first step in this endeavor is awareness of ESD/EOS events; the second step is mitigation. The Xilinx support team offers advice and consultation to customers on best practices and preventive measures.

Additional Resource

To see a summary of the reliability test data and results for Xilinx devices, see [UG116](#), *Device Reliability Report*. This report is updated four times per year.

References

1. *Threshold*, newsletter of the Electrostatic Discharge Association (ESDA), Vol.29 No.2 (March/April 2013), downloaded from http://esda.org/threshold_archives.cfm
2. Absolute Maximum Ratings (AMR) for 7 Series FPGAs. See Table 1, *Absolute Maximum Ratings* in the data sheet for each of the 7 Series FPGA devices:
Artix®-7: Data sheet [DS181](#), *DC and AC Switching Characteristics*.
Kintex®-7: Data sheet [DS182](#), *DC and AC Switching Characteristics*.
Virtex®-7: Data sheet [DS183](#), *DC and AC Switching Characteristics*.
3. XC Devices: Human Body Model (HBM): **ANSI/ESDA/JEDEC JS-001**
XA Devices: Human Body Model (HBM): **AEC-Q100-002**
4. XC Devices: Charged Device Model (CDM): **JESD22-C101**
XA Devices: Charged Device Model (CDM): **AEC-Q100-011**
5. *Recommended ESD Target Levels for HBM/MM Qualification*: see JEDEC, JEP155. Download (with registration) at <http://www.jedec.org/standards-documents/docs/jep-155>.
6. *CDM ESD Specifications and Requirements*: see Industry Council on ESD Target Levels, <http://www.esdindustrycouncil.org/ic/en/>

Revision History

The following table shows the revision history for this document:

Date	Version	Description of Revisions
06/24/13	1.0	Initial Xilinx release.

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