# 60G Millimeter-Wave Backhaul Link Is Poised to Boost Cellular Capacity

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A complete 60-GHz two-way data communication scheme based on Xilinx's Zynq SoC offers the performance and flexibility to serve the small-cell backhaul market.

The ever-increasing demand for data on the world's cellular networks has operators searching for ways to increase the capacity 5,000-fold by 2030 [1]. Getting there will require a 5x increase in channel performance, a 20x increase in allocated spectrum and a 50x increase in the number of cell sites.

Many of these new cells will be placed indoors, where the majority of traffic originates, and fiber is the top choice to funnel the traffic back into the networks. But there are many outdoor locations where fiber is not available or is too expensive to connect, and for these situations wireless backhaul is the most viable alternative.

Unlicensed spectrum at 5 GHz is available and does not require a line-of-sight path. However, the bandwidth is limited and interference from other users of this spectrum is almost guaranteed due to heavy traffic and wide antenna patterns.

Communication links of 60 GHz are emerging as a leading contender to provide these backhaul links for the many thousands of outdoor cells that will be required to meet the capacity demands. This spectrum is also unlicensed, but unlike frequencies below 6 GHz, it contains up to 9 GHz of available bandwidth. Moreover, the high frequency allows for very narrow and focused antenna patterns that are somewhat immune to interference.

A complete 60-GHz two-way data communication link developed by Xilinx and Hittite Microwave (now part of Analog Devices) demonstrates superior performance and the flexibility to meet the requirements of the small-cell backhaul market (Figure 1). Xilinx developed the digital modem portion of the platform and Analog Devices, the millimeter-wave radio portion.

As depicted in Figure 1, two nodes are required to create this link. Each node contains a transmitter (with a modulator) with its associated analog Tx chain and a receiver (with a demodulator) with its associated analog Rx chain.

The modem card is integrated with analog and discrete devices. It contains oscillators (DPLL module) to ensure the accuracy of frequency synthesis, and all the digital functions are executed in an FPGA or SoC. This single-carrier modem core supports modulations from QPSK to 256QAM in channel bandwidths up to 500 MHz, and achieves date rates as high as 3.5 Gbps. The modem also supports both frequency-division duplex (FDD) and time-division duplex (TDD) transmission

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## MILLIMETER-WAVE MODEM

The Xilinx millimeter-wave modem solution enables infrastructure vendors to develop flexible, cost-optimized and customizable links for their wireless backhaul networks. This solution is targeted at the Xilinx® Zynq®-7000 All Programmable SoC or Kintex®-7 FPGA devices, which are part of Xilinx's "generation-ahead" 28-nanometer product family.

Xilinx's solution is fully adaptive, is low in power and small in footprint, and can be used to deploy indoor and full outdoor point-to-point links as well as point-to-multipoint microwave links. Just as with its silicon, Xilinx's road map for its millimeter-wave modem solution is very aggressive, and presents operators with the unique ability to deploy scalable and field-upgradable systems.

Figure 2 further details the digital modem as implemented on the Zynq SoC platform. Alongside the programmable logic (PL), the platform's scalable processing system (PS) contains dual ARM® Cortex™-A9 cores with integrated memory controllers and multistandard I/Os for peripherals.

This system-on-chip (SoC) platform is highly flexible. Here, it is used to perform various data and control functions and to enable hardware acceleration. An integrated millimeter-wave modem solution complete with PHY, controller, system interfaces and packet processor is shown in Figure 2. However, based on the required architecture, you could insert, update or remove different modules. For instance, you might choose to implement an XPIC combiner so that you could use the modem in cross-polarization mode with another modem. The solution is implemented in the PL, where serdes and I/Os are used for various data path interfaces such as those between the modem and packet processor, the packet processor and memory, inter-modem or DAC/ADC.

Some of the other important features of the Xilinx modem IP include automatic hitless and errorless state switching through adaptive coding and modulation (ACM) to keep the link operational;

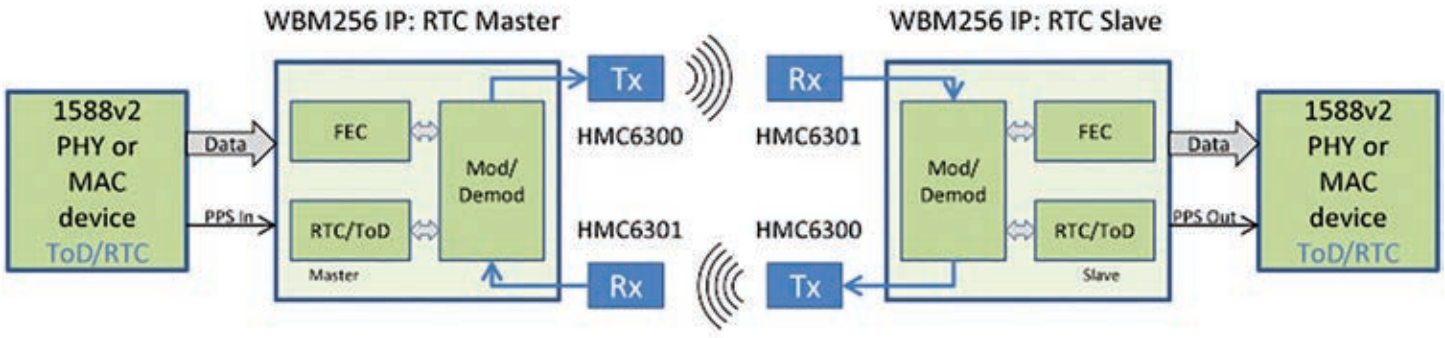


Figure 1 – High-level block diagram of the complete two-way communication link

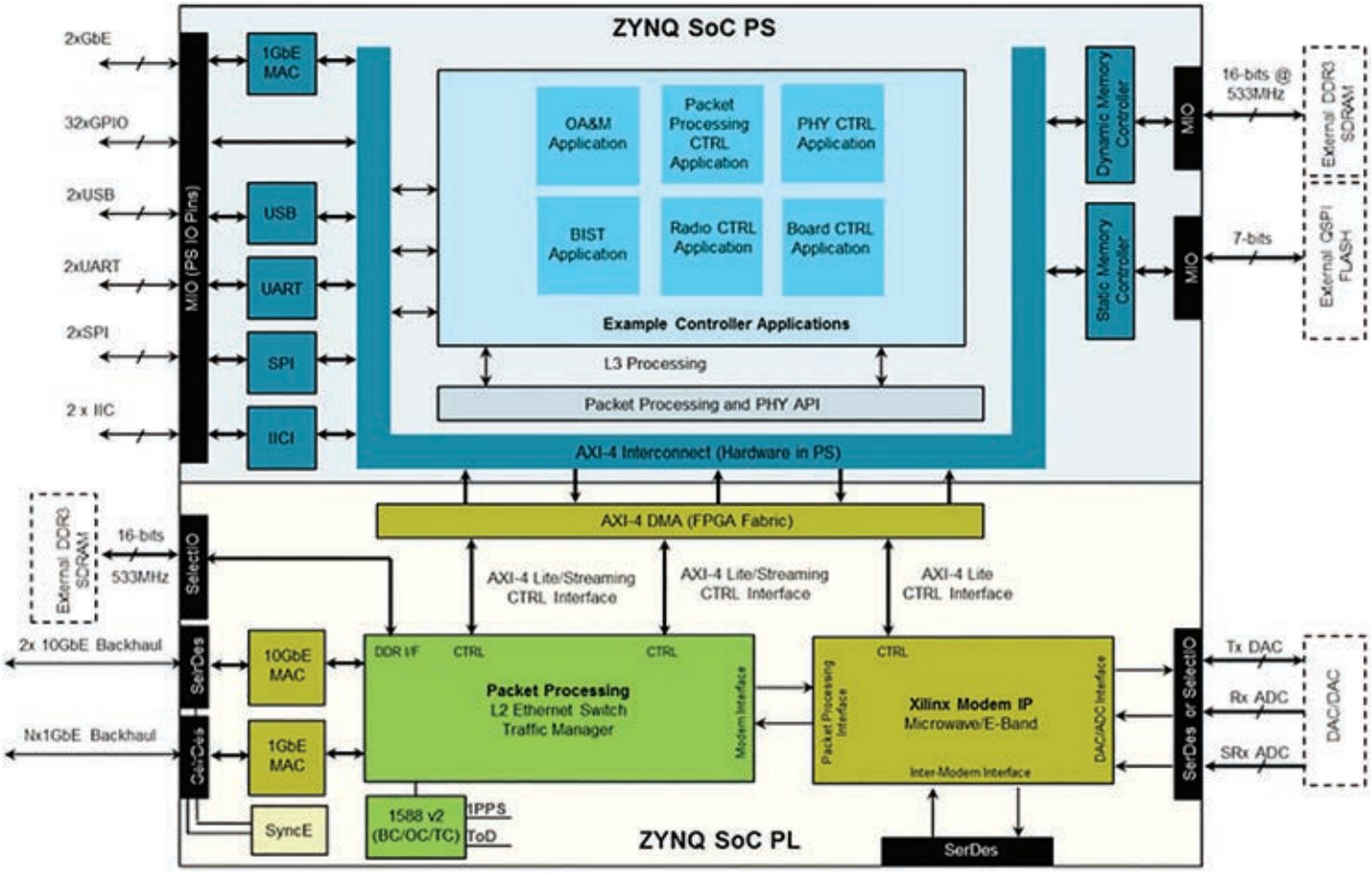


Figure 2 – All Programmable SoC for wireless modem applications

adaptive digital closed-loop predistortion (DPD) to improve RF power amplifier efficiency and linearity; synchronous Ethernet (SyncE) to maintain clock synchronization; and Reed-Solomon or low-density parity check (LDPC) forward error correction (FEC). The FEC choice is based on the design requirements. LPDC FEC is the default choice for wireless backhaul applications, whereas Reed-Solomon FEC is preferred for low-latency applications such as front-haul.

LDPC implementation is highly optimized and exploits FPGA parallelism for the computations done by the encoders and decoders. The result is noticeable SNR gains. You can apply different levels of parallelism by varying the number of iterations of the LDPC core, thereby optimizing the size and power of the decoder. You can also model the solution based on channel bandwidth and throughput constraints.

The Xilinx modem solution also comes with a powerful graphical user interface (GUI) for both display and debug, and is capable of high-level functions such as channel bandwidth or modulation selection as well as low-level ones such as setting of hardware registers. To achieve 3.5-Gbps throughput for the solution shown in Figure 1, the modem IP runs at a 440-MHz clock rate. It uses five gigabit transceivers (GTs) for connectivity interfaces to support ADCs and DACs, and a few more GTs for 10GbE payloads or CPRI interfaces.

## MILLIMETER-WAVE TRANSCEIVER CHIP SET

In late 2014, Analog Devices released its second-generation silicon germanium (SiGe) 60-GHz chip set, significantly enhanced and optimized for the small-cell backhaul application. The HMC6300 transmitter chip is a complete analog baseband-to-millimeter-wave upconverter. An improved frequency synthesizer covers 57 to 66 GHz in 250-MHz steps with low phase noise and can support modulations up to at least 64QAM. Output power has increased to roughly 16-dBm linear power, while an integrated power detector monitors the output power so as not to exceed the regulatory limits.

The transmitter chip offers either analog or digital control of the IF and RF gains. Analog gain control is sometimes needed when using higher-order modulations, since discrete gain changes can be mistaken for amplitude modulation, leading to bit errors. Digital gain control is supported using the built-in SPI interface.

For applications requiring even higher-order modulation in narrow channels, an external PLL/VCO with even

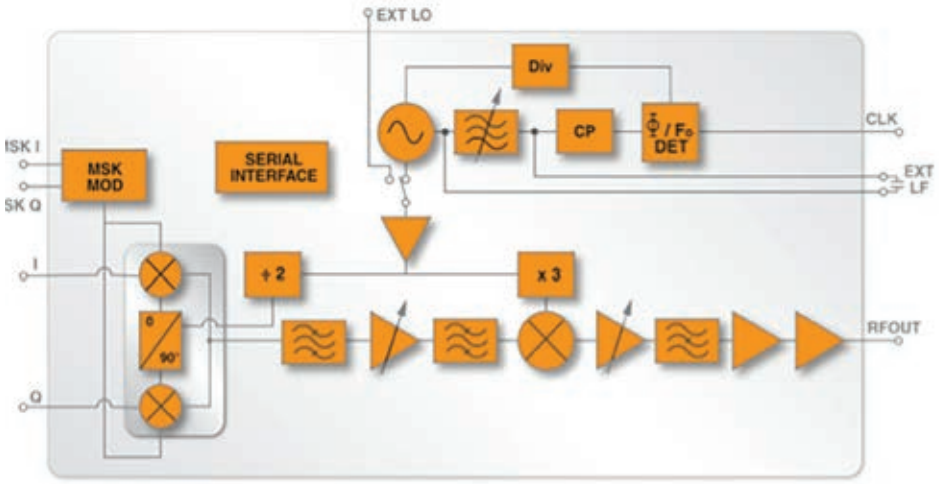


Figure 3 – HMC6300 60-GHz transmitter IC block diagram

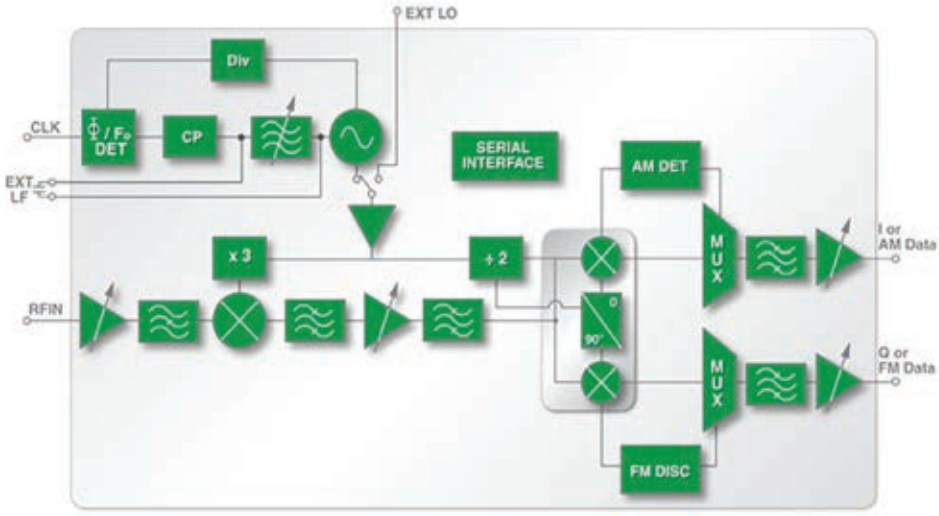


Figure 4 – HMC6301 60-GHz receiver IC block diagram

lower phase noise can be injected into the transmitter, bypassing the internal synthesizer. Figure 3 shows a block diagram of the HMC6300.

The transmitter supports up to 1.8 GHz of bandwidth. An MSK modulator option enables low-cost data transmissions up to 1.8 Gbps without the need for expensive and power-hungry DACs.

Complementing this device is the HMC6301 receiver chip, likewise optimized to meet the demanding requirements of small-cell backhaul. The receiver features a significant increase in the input P1dB to -20 dBm and IIP3 to -9 dBm to handle short-range links where the high gain of the dish antennas lead to high signal levels at the receiver input.

Other features include a low, 6-dB noise figure at the maximum gain settings; adjustable low-pass and high-pass baseband filters; the same new synthesizers as found in the transmitter chip to support 64QAM modulation over the 57- to 66-GHz band; and either analog or digital control of the IF and RF gains.

A block diagram of the HMC6301 receiver chip is shown in Figure 4. Note that the receiver also contains an AM detector to demodulate amplitude modulations such as on/off keying (OOK). Also, an FM discriminator demodulates simple FM or MSK modulations. This is in addition to the IQ demodulator that is used to recover the quadrature baseband outputs for QPSK and more-complex QAM modulations.

Both the HMC6300 transmitter and HMC6301 receiver will be available in a 4 x 6-mm BGA-style wafer-level package. They will be designated the HMC6300BG46 and HMC6301BG46 and are scheduled for sampling in early 2015. These surface-mount parts will enable the low-cost manufacturing of the radio boards.

A block diagram of an example millimeter-wave modem and radio system is shown in Figure 5. In addition to the FPGA, modem software and millimeter-wave chip set, the design also contains a number of other components. They include the AD9234 dual-channel 12-bit, 1-Gsample/second ADC; the AD9144 quad-channel 16-bit, up to 2.8-GSPS Tx-DAC; and the HMC7044 ultralow-jitter clock synthesizer with support for the JESD204B serial data interface that is employed on both the ADC and the DAC ICs.

## DEMONSTRATION PLATFORM

Xilinx and Analog Devices have jointly created a demonstration platform implementation featuring the FPGA- based modem on the Xilinx KC705 development board, an industry-standard FMC board containing ADCs, DACs and clock chip, and two radio module evaluation boards (Figure 6). The demo platform includes a laptop for modem control and visual display, and a variable RF attenuator to replicate the path loss of a typical millimeter-wave link. The Xilinx KC705 development board features the Kintex-7 XC7K325T-2FFG900C FPGA executing the WBM256 modem firmware IP. An industry-standard FMC mezzanine connector on the development board is used to connect to the baseband and millimeter-wave radio boards.

The millimeter-wave modules snap onto the baseband board. The modules have MMPX connectors for the 60-GHz interfaces as well as SMA connectors for optional use of an external local oscillator.

This platform contains all the hardware and software needed to demonstrate point-to-point backhaul connections of up to 1.1 Gbps in 250-MHz

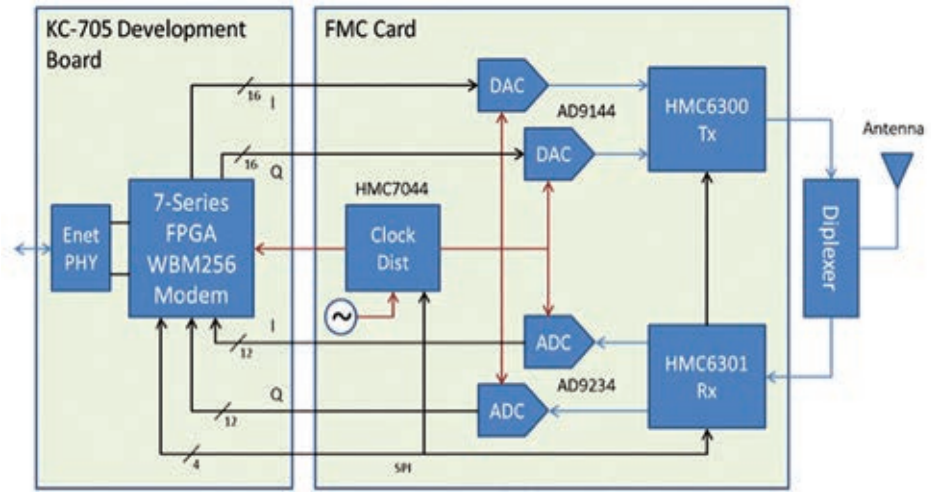


Figure 5 – Example reference design using Xilinx and Analog Devices ICs

channels for each direction of a frequency-division duplex connection.

## MODULAR AND CUSTOMIZABLE

FPGAs are increasingly being used in various wireless backhaul solutions, since the platforms based on them can be highly modular and customizable, thereby reducing the total cost of ownership for the OEMs. Owing to significant power improvements in its 7 series FPGA/SoC families and high-performing wideband IP cores, Xilinx expects its millimeter-wave modem solution to be a front-runner for the small-cell backhaul application. Xilinx FPGAs and SoCs are suitable for high-speed and power-efficient designs, and its high-speed GTs can be used effectively for wideband communications and switching functions. Xilinx's solution can be scaled to support multiple product variations, from lower-end small-cell backhaul products operating at a few hundred megabits per second to 3.5 Gbps on the same hardware platform.

For the radio portion, the transceivers have now been integrated into silicon-based ICs and packaged into surface-mount parts, allowing for low-cost manufacturing. Analog Devices' millimeter-wave chip set meets the wireless backhaul needs of the small-cell deployments and provides market-leading performance in power, size, flexibility and functionality. Analog Devices also provides industry-best data converters and clock-management ICs that are critical components of this complete solution. Together, the two companies intend to drive the industry adoption of this exciting technology.

### Reference

1. "Evolutionary and Disruptive Visions Towards Ultra High Capacity Networks," IWPC, April 2014

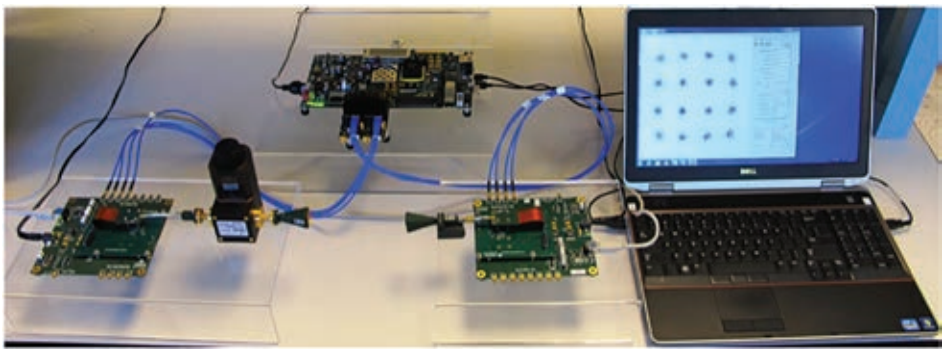

Figure 6 – The demonstration platform in action