Simplify Your 'Hot' Testing with Xilinx's Zynq SoC

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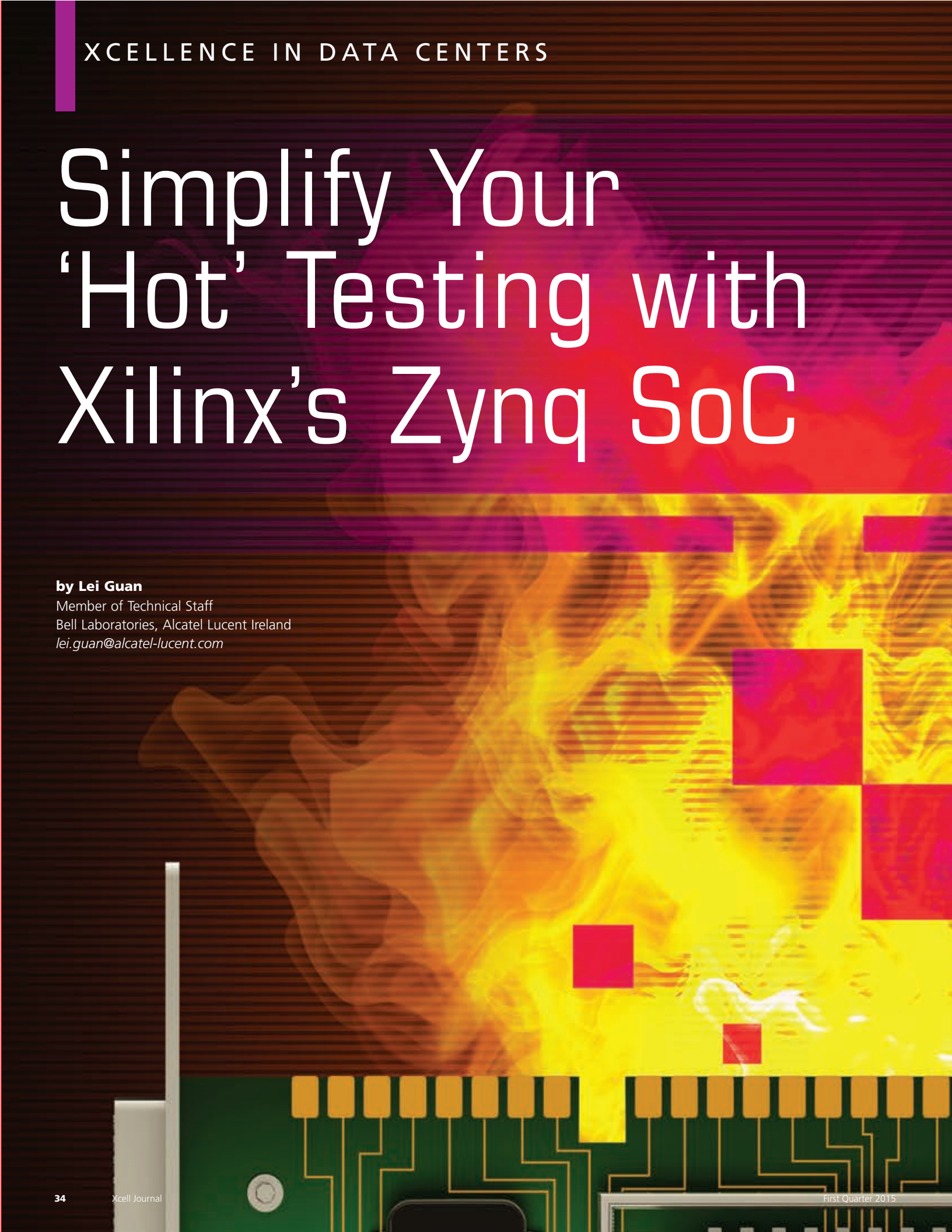
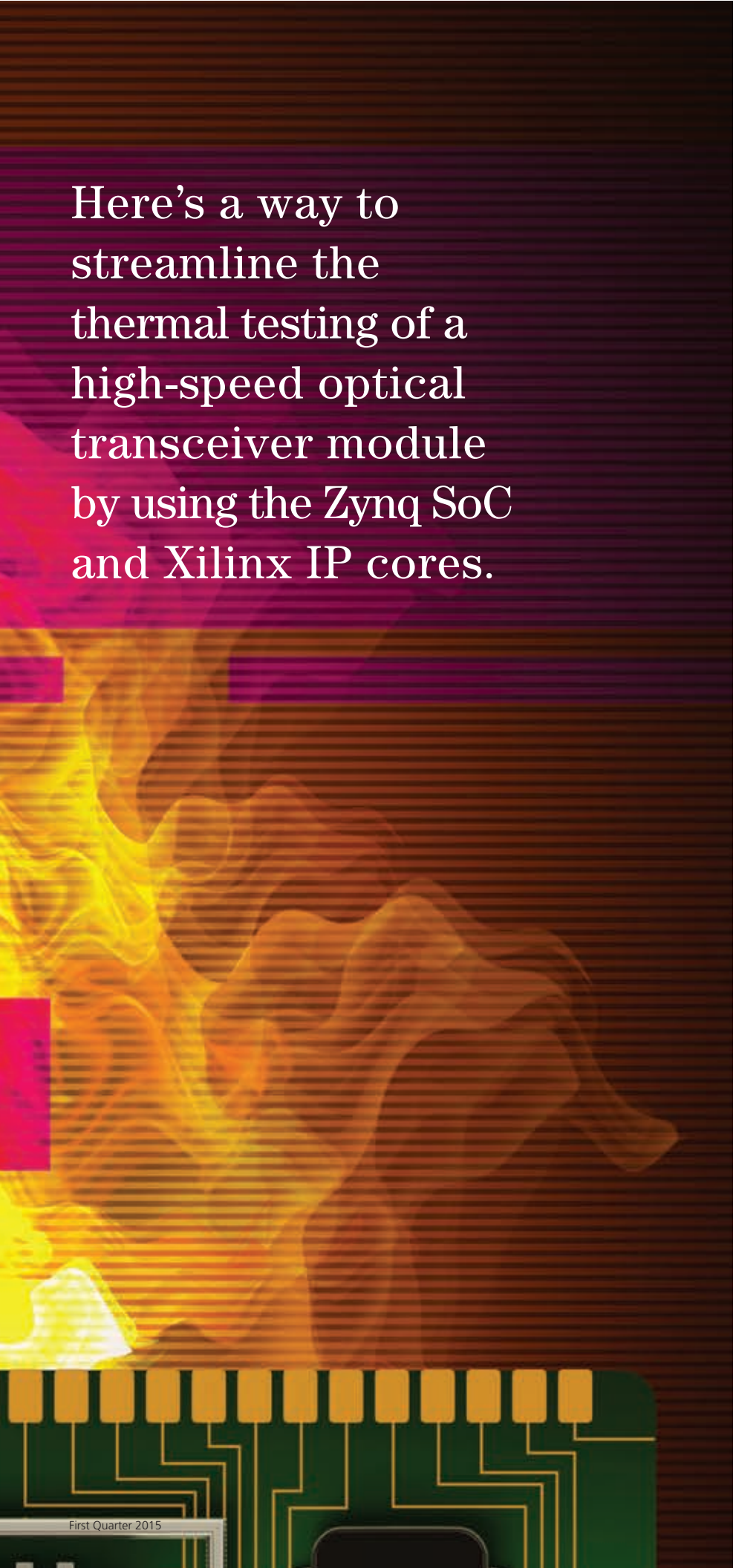


Here's a way to streamline the thermal testing of a high-speed optical transceiver module by using the Zynq SoC and Xilinx IP cores.



As the transmission speed of optical transceiver modules in data centers rises ever higher, the temperature of each chassis in a data center is also rising dramatically. The increase in temperatures becomes compounded when these modules are stacked on top of one another in racks that are flanked by even more racks of speedy but hot modules. This compounded rise in temperature can cause chips to exceed their thermal limits, creating catastrophic chip failures that in turn could adversely affect entire data center systems. Thus, it's imperative that engineers designing optical transceiver modules take thermal properties into account. Designers must zero in on the heat sources and attempt to keep them in check with effective cooling methods at the module and even rack level.

To test the thermal properties of optical modules, engineers traditionally had two choices. They could use a complicated network data generator to create high-speed (10-Gbps) links and then test the thermal properties of the optical modules; or they could utilize a so-called "thermal-equivalent" module with preset tunable voltage and current to mimic the thermal situation and evaluate the thermal properties without using any real high-speed data.

Neither of these approaches is optimal. The first approach is a costly operation due to the need for a professional high-speed network data generator, while the second method is too abstract. A thermal-equivalent module cannot fully reflect the temperature variation driven by the physical switching behavior.

But recently, my team at Bell Laboratories, Alcatel Lucent Ireland, radically simplified this process by using a Xilinx®

I picked the Xilinx ZC706 evaluation board because the GTX transceivers on the main device can easily achieve single-line 10-Gbps data transmission.

Zynq®-7000 All Programmable SoC platform and Xilinx intellectual-property (IP) cores to do the same job. Let's take a closer look at how we accomplished this simplification of testing.

PREDESIGN ANALYSIS

The fundamental requirement of this type of thermal testing is to stimulate the XFP optical transceiver continuously with 10-Gbps data while using an IR camera to track and characterize the temperature variation.

I picked the Xilinx ZC706 evaluation board as the development host, because the GTX transceivers on the main device, the Zynq-7000 SoC XC7Z045 (speed grade -2), can easily achieve single-line 10-Gbps data transmission. The Zynq SoC device contains a processing system (PS) built around an ARM® core and a Kintex®-7 FPGA programmable logic (PL) fabric. Initially, resources at the PL die are enough for handling the 10-Gbps duplex data transmission. Then we can use the PS to generate particular user data patterns if they are required in the future.

Our thermal group provided a Finisar XFP evaluation board as the optical transceiver housing. This FDB-1022 evaluation board is a powerful host for evaluating the state-of-the-art 10-Gbps XFP optical transceivers. SMA connectors are provided for differential data inputs and outputs. The board can be configured to allow a direct connection of a 1/64 clock (that is, 156.25 MHz = 10 GHz/64) via SMA connectors for clocking the module.

SYSTEM DESIGN

I've found over the course of my seven years of doing FPGA development that you can significantly reduce your design cycle by using as many Xilinx cores as possible. In this design, I kept the same strategy and started from the Integrated Bit Error Ratio (IBERT) core, which you can utilize to perform pattern generation and verification to evaluate the GTX transceivers on the Zynq SoC. Then, in order to properly route the design, I created a phase-aligned clock-distribution unit based on the Mixed-Mode Clock Manager (MMCM) core for simultaneously clocking both of the GTX transceivers on the FPGA fabric and the optical transceiver on the XFP evaluation board. Figure 1 shows the system diagram.

For this design project, I used Xilinx's older ISE® Design Suite tools and did the work in three steps.

Step one involved creating an IBERT core with the CORE Generator™ tool.

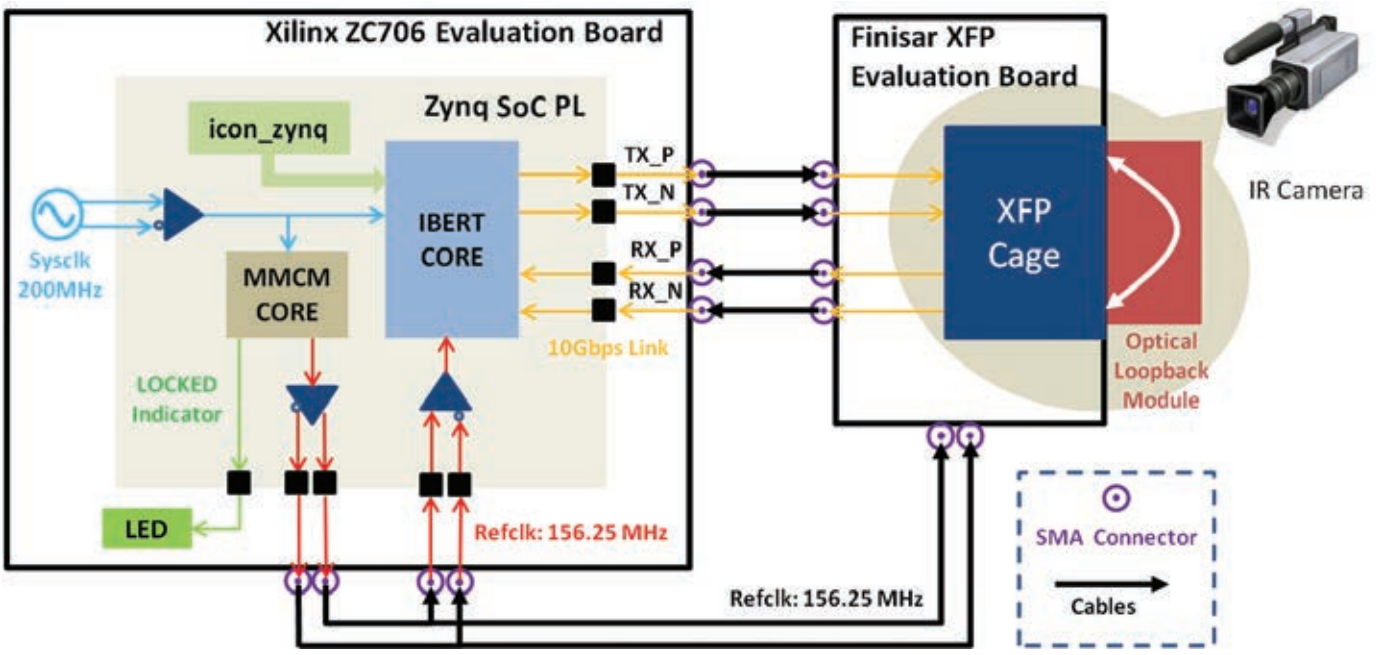


Figure 1 – Block diagram of the proposed system with a connection example

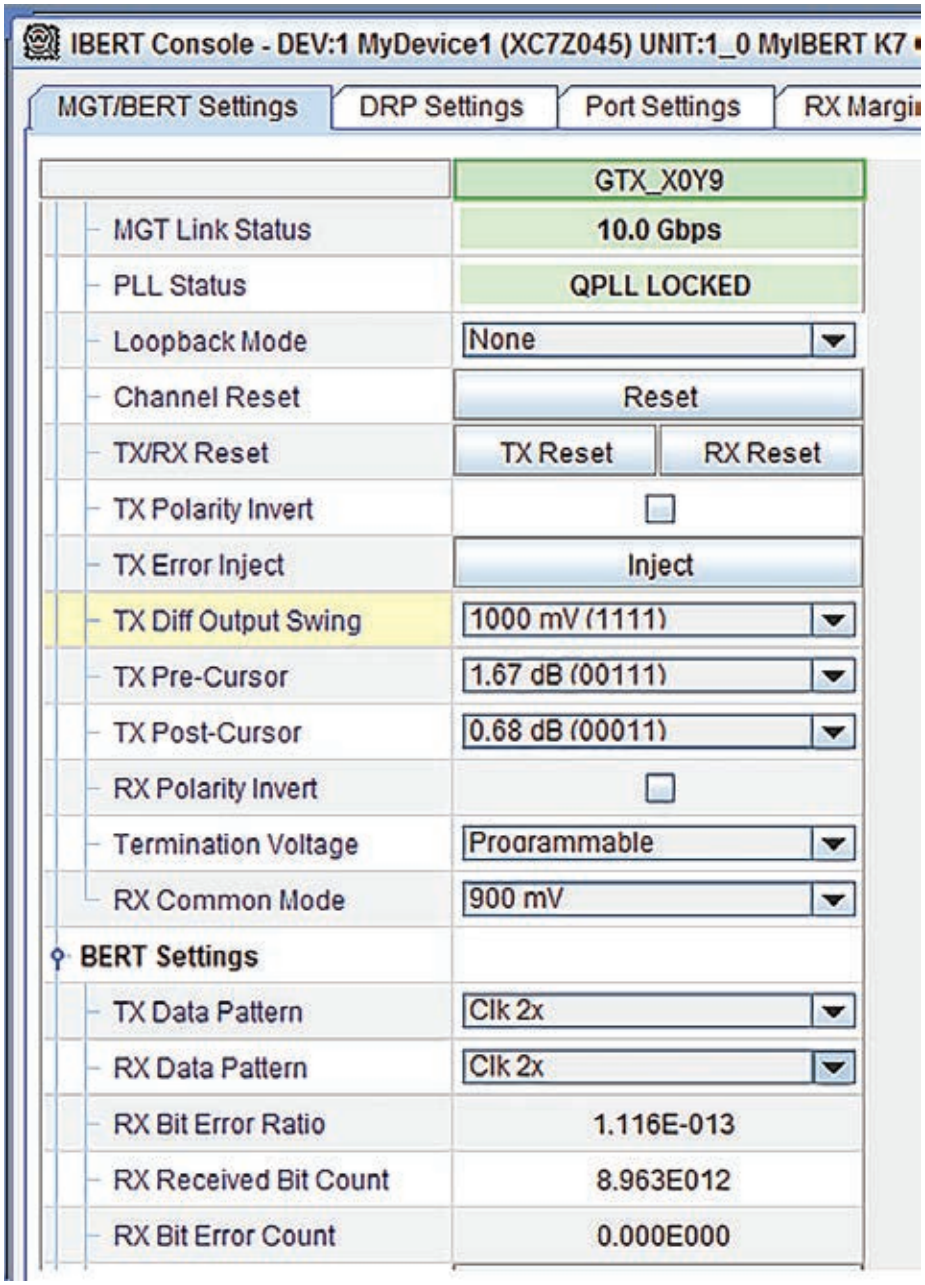


Figure 2 – Snapshot of the ChipScope Pro screen

Here are some of the key settings for this IBERT 7 series GTX (ChipScope™ Pro) IBERT core. In my design, the IBERT system clocking comes from an external clock source on the board—a 200-MHz differential clock with `P pin location = H9` and `N pin location = G9`. The GTX clocking mode is independent for `QUAD 111`, and I set the line rate to `Max Rate = 10Gbps`. I set the reference clock for the GTX to `Refclk = 156.25 MHz` and the `Refclk source = MGTREFCLK1 111`.

In step two, I created an MMCM core with the CORE Generator. It was imperative to get the tool's Clocking Wizard settings correct. To do this, I set the clock features as `frequency synthesis` and `phase alignment`. The input clock has to be the same system clock on the board (200 MHz). And I set the targeting derivative clock to 156.25 MHz with 50 percent duty cycle. I used two extra signals, `RESET` and `LOCKED`, for controlling and indicating the MMCM core.

The third step was to assemble everything with Xilinx's tools. For this project, I used the ISE Design Suite 14.4. At some point later on, I am planning to switch to the Vivado® Design Suite in order to maximize the performance of the chip.

I first created a new project in ISE, then moved the IBERT core folders (`example_ibert_gtx.vhd`, `ibert_gtx_top.ucf`, `ibert_core.ngc` and `icon_zynq.ngc`) to the ISE project. Next, I added `mmcm_core.vhd` from the MMCM core folder (step 2) to the ISE project. I then used `example_ibert_gtx.vhd` as the top module, instantiated the `mmcm_core` and added three new signals (`CLK_OUTPUT_P`, `CLK_OUTPUT_N` and `LED_REFCLK`) to the design and made corresponding pin assignments in the `ibert_gtx_top.ucf`.

SYSTEM TEST

After generating the .bit file, the FPGA design was ready for stimulating the XFP optical transceiver with a 10-Gbps link. I connected the two boards (as shown in Figure 1), then opened a ChipScope Pro analyzer and configured the device with the newly built .bit file. Next, I double-clicked the IBERT console, causing a new graphical user interface to pop up (as shown in Figure 2). With this screen, we can thoroughly evaluate the thermal performance of the optical transceiver by tuning the predefined data patterns, such as Clk 2x (1010….), and pseudo-random binary sequences (PRBS).

By using Xilinx cores, together with the ZC706 evaluation board, it's easy to build a test platform for evaluating high-speed optical transceivers. In this design, we illustrated the evaluation of a single XFP module. However, you can straightforwardly apply the design methodology to quickly build a logic core for testing multiple optical transceiver modules.

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