Faster Design Entry with Vivado IP Integrator and Xilinx IP

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Here's how to optimize Xilinx cores for use with Vivado IPI in a CPRI remote radio head design.

Modern FPGA-based designs use an increasing amount of intellectual property (IP), both in variety and number of instances. The Vivado® Design Suite's IP Integrator (IPI) tool and Xilinx® communications IP are making it easier to quickly connect these IP blocks together.

To illustrate the power of the IPI approach, let us consider the example of a wireless remote radio head (RRH). Situated near the antenna, the RRHs form part of a cellular communications network. They are normally connected with optical fiber upstream to a baseband transceiver station and optionally downstream to further RRHs, thus implementing a multihop topology (Figure 1).

The Common Public Radio Interface (CPRI) protocol is widely used in linking these RRHs together. Let's create an example design with one uplink CPRI port and three downlink CPRI ports, and connect them. We can accomplish the majority of this job with IPI. The result will form a major component in the overall design. We will use a Kintex®-7 device, which is an excellent fit in this application due to its low power, low cost and high performance. The GTX transceivers in -2 speed-grade All Programmable Kintex FPGAs and Zynq®-7000 SoCs make it possible to use the 9.8-Gbps CPRI line rate.

Figure 2 shows what we will create within IPI. We can create the block design and instance the required IP from the IP catalog. The CPRI cores are available in the standard Xilinx IP catalog and have been optimized for the sharing of resources where possible and for ease of use in IPI. The switches are custom IP.

IP CORE RESOURCE SHARING

One of the challenges customers encounter when using multiple instances of IP is how to share resources efficiently. A number of communications IP cores support the "shared logic" feature. In the case of the CPRI core, we can configure the IP with sharable logic resources inside the core or we can omit these shared resources. If they are included in the core, they will provide the necessary outputs to let us connect them to the cores that have excluded the logic.

Users with specialized requirements may wish to exclude this logic on all their cores and implement their own.

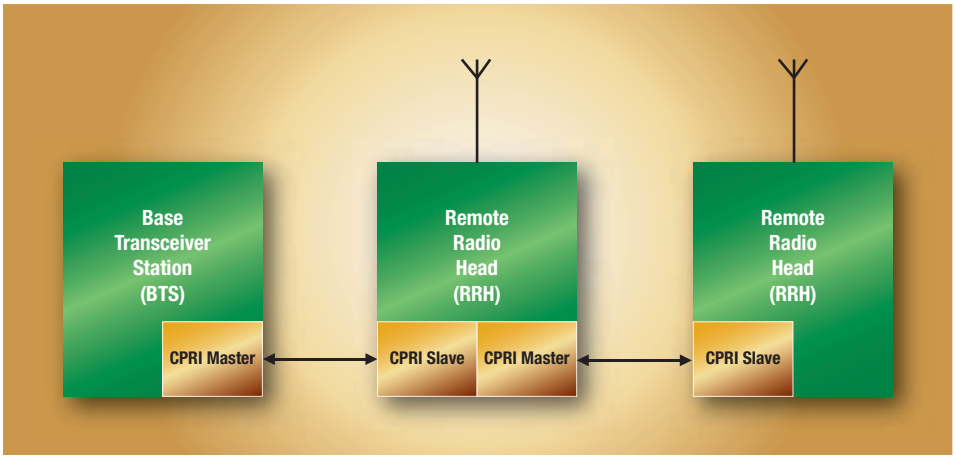

Figure 1 – Diagram of a multihop topology

In our design, we have configured CPRI cores to run at 9.8 Gbps. At this line rate, it is necessary to use an LC-tank-based oscillator for the transceiver clock. Transceivers in the Kintex-7 device are arranged in quads, with each transceiver quad consisting of four transceiver channels and one LC-tank-based quad phase-locked loop (QPLL). It is necessary for all the cores to share the QPLL and the clock generated by the uplink clocking. Figure 3 shows the QPLL and clock output ports on the uplink core customized with shared logic connected to the appropriate input ports on a downlink CPRI core that has been customized with it excluded.

ROUTING DATA BETWEEN CPRI CORES

We have also instantiated the IQ switch and the Ethernet switch to allow data to be routed between the cores.

Control and management data in the CPRI network is transmitted via an Ethernet subchannel. The Ethernet switch in the system makes it possible to issue firmware updates or commands remotely and transmit them to any node. The IP was designed to use as few logic resources as possible, since a fully featured Ethernet switch in this situation is not necessary.

The IQ switch provides the ability to route any IQ sample between CPRI cores with deterministic latency. An important feature for multihop radio systems is the ability to accurately measure the link delay, and the CPRI standard defines a method to facilitate this measurement.

CONNECTING INTERFACES WITH IPI

IPI bus interfaces map a defined set of logical ports to particular physical ports on the IP. If we use interfaces wherever possible, we move from connecting many signals to connecting a few interfaces. Common bus interfaces on IP are those that conform to the ARM® AXI specification, such as AXI4-Lite and AXI4-Stream. This elevation of abstraction makes design entry

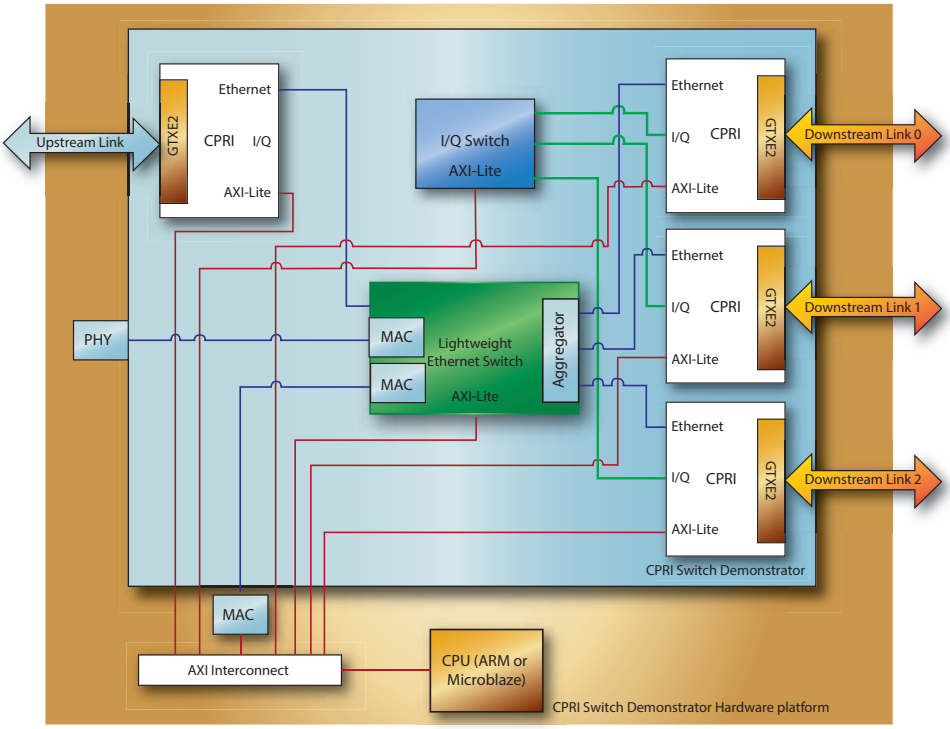

Figure 2 – CPRI switch hardware platform

easier and faster, and also allows you to take advantage of design rule checks for the interface. Vivado IP Packager will allow you to use your own IP within IP Integrator and to take advantage of interfaces in your own design.

IPI makes it easy to connect interfaces together. Simply click on the interface and IPI will indicate what it can connect to. Drag the connection line to the desired end point and the connection will be made. This technique allows you to connect many signals with just a couple of clicks.

Figure 4 shows the Ethernet switch providing a number of AXI4-Stream interfaces, two GMII interfaces and an AXI4-Lite interface. The streaming interfaces allow direct connection to the CPRI cores and this removes the need for internal buffering on the CPRI core. The GMII interfaces allow connection to an Ethernet PHY, which could be useful

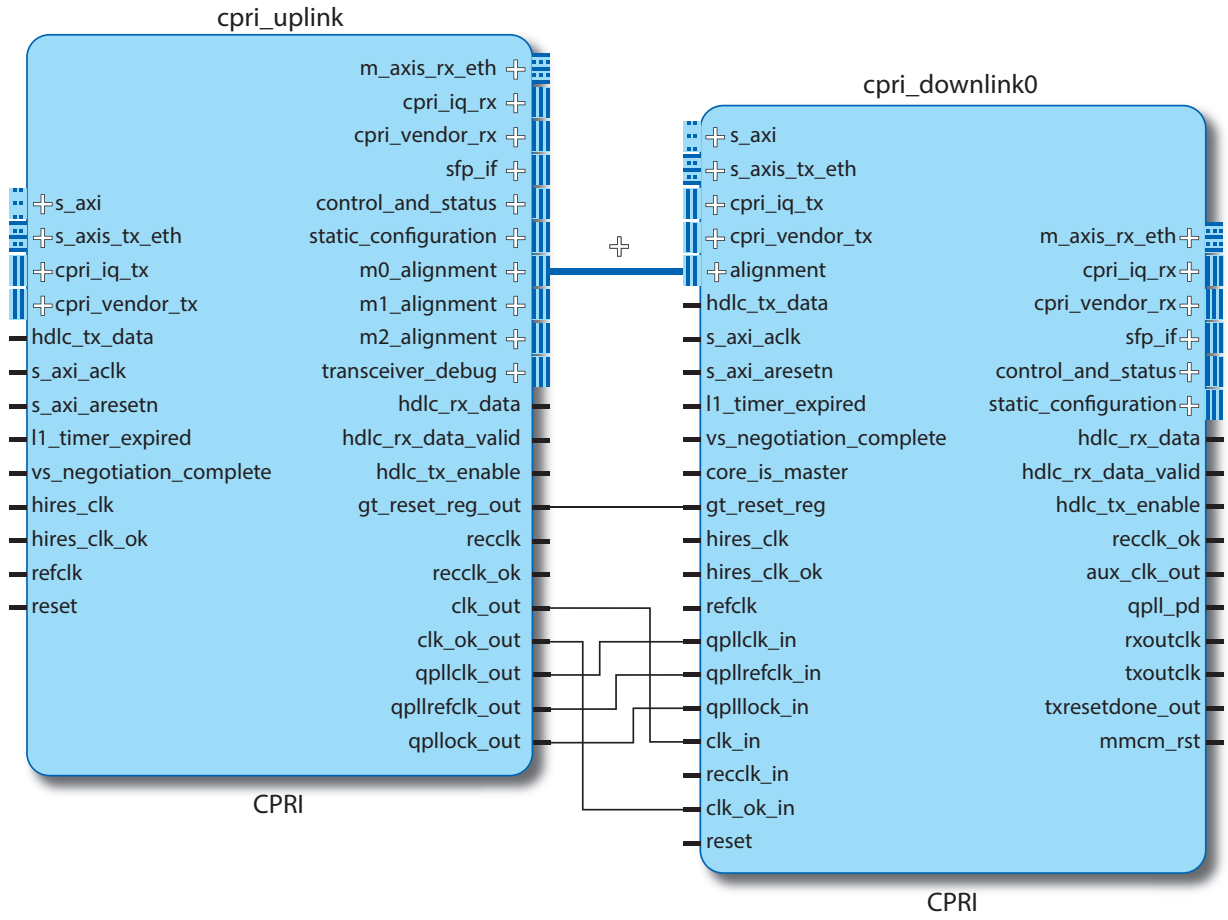

Figure 3 – Shared logic connections for a QPLL

for an engineer in the field debugging a network issue. The AXI4-Lite management interface provides access to the address table mapping and other configuration options such as the address table aging interval.

Continuing in this fashion, we can build up our system, connecting the interfaces within IPI. You have the flexibility to use whatever entry method works best for you. In addition to using the GUI to link interfaces, you can also opt to directly issue commands through the Tcl console or source them from a script. Every time you do something in the GUI, the resulting command will be echoed back.

You can also export the entire design when you have finished creating it with the command "write_bd_tcl." This command will create a Tcl file that can be sourced to create the entire block design from scratch and can be easily used as part of a scripted build flow. All of the IP in the design provides an AXI4-Lite management interface to allow the cores to connect to a host processor. Intelligence built into IPI allows connection automation. With this mechanism, IPI will recognize that the AXI4-Lite interface on our IP will connect to the AXI bus interconnect and automatically configure the appropriate address ranges and connect the bus for us. You can then connect this bus to the host processor with the aid of IPI. The host processor in our case is a MicroBlaze™, but if using a Zynq SoC series device it could be easily changed to leverage the ARM CPU.

FURTHER GAINS COMING

Vivado IP Integrator capabilities are growing rapidly and with that growth, further gains will be achieved. With the right IP, we can put together whole subsystems quickly and reap the rewards.

For more information on the CPRI, Ethernet switch or IQ switch IP, contact Perminder Tumber at Xilinx Wireless Communications (*permind@xilinx.com*).

Figure 4 – Ethernet switch symbol with interfaces