Productivity Skyrockets with Xilinx's UltraScale Architecture

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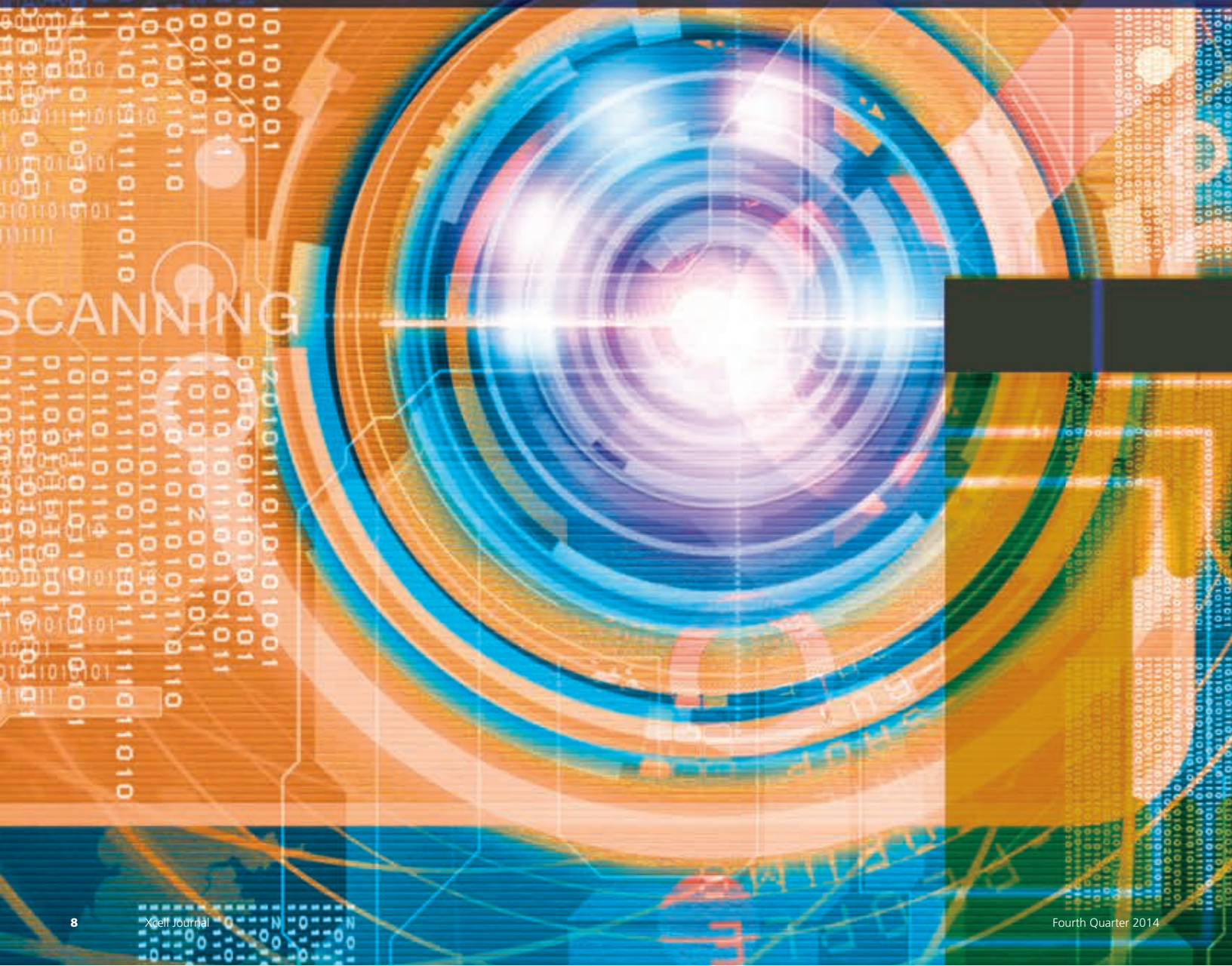
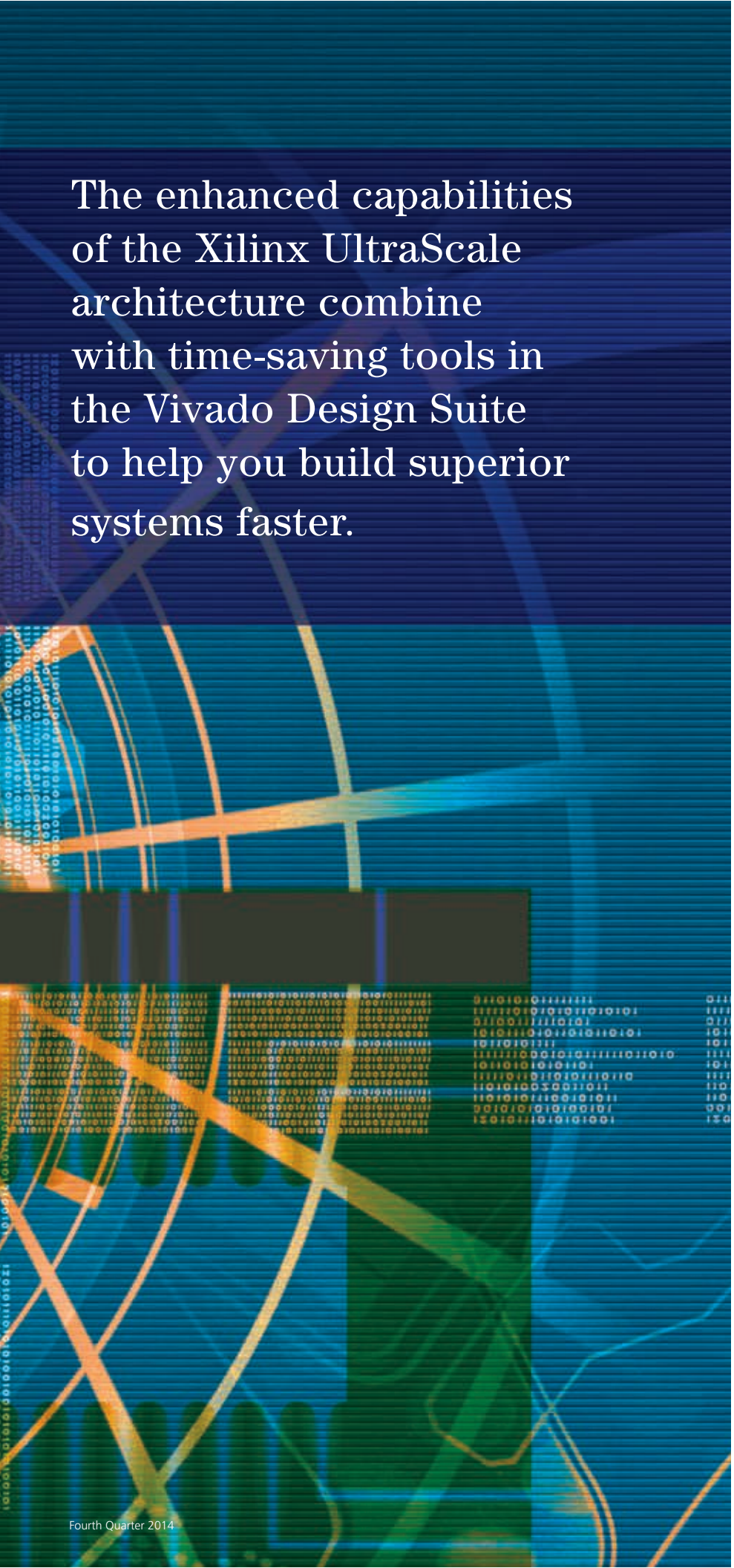


The enhanced capabilities of the Xilinx UltraScale architecture combine with time-saving tools in the Vivado Design Suite to help you build superior systems faster.



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Many markets and applications require a tremendous increase in system bandwidth and processing capability. Whether in wired or wireless communications, digital video or image processing, increased data throughput requirements have the same result: increasing traffic and demands on all system components. More data arrives on-chip through parallel and serial I/O. The data must then be buffered, again through both parallel I/O in the form of DDR memory and serial I/O in the form of serial memory standards such as Hybrid Memory Cube (HMC) and MoSys Bandwidth Engine. The data must then be processed in the logic and DSP before being transmitted to its next destination back through the parallel and serial I/O.

System processing requirements are becoming more complex for a number of reasons; larger data packets traveling at an increased data rate result in wider parallel data buses at increased frequency. To efficiently process the data, it is often necessary to build an entire system in a single device, thereby eliminating the latency and power consumption associated with sending large quantities of data between two FPGAs. The result is a need for ever-denser FPGAs with more capabilities. It is imperative that as these high-capability FPGAs are more heavily utilized, they maintain the ability to operate at their maximum possible performance, avoiding performance degradation as the device fills up.

Filling complex, high-capacity devices to high utilization could sound like a daunting task for the designer. Xilinx provides numerous solutions specifically aimed at reducing design time, freeing designers to

Data is transported to and from UltraScale FPGAs through a combination of high-performance parallel SelectIO and high-speed serial transceiver connectivity.

focus their efforts on what differentiates their product in their market.

THE ULTRASCALE ARCHITECTURE

To address the prevailing market challenges, Xilinx recently introduced the UltraScale™ architecture (Figure 1), providing unprecedented levels of system integration, performance and capability. Xilinx has used this new architecture to create two high-performance FPGA families. The Xilinx® Virtex® UltraScale and Kintex® UltraScale families combine to address a vast spectrum of system requirements with a focus on lowering total power consumption through numerous innovative technological advancements. Sharing numerous building blocks, the UltraScale technology provides a scalable architecture, optimized for different market demands.

INCREASING SYSTEM BANDWIDTH

Before any signal processing or data manipulation can occur, data needs to reach its destination. Numerous serial and parallel protocols and standards exist today tailored to the specific needs of their target applications. The common theme among most standards is the desired increase in total data throughput, enabling vast quantities of information to move through a system at increasing data rates.

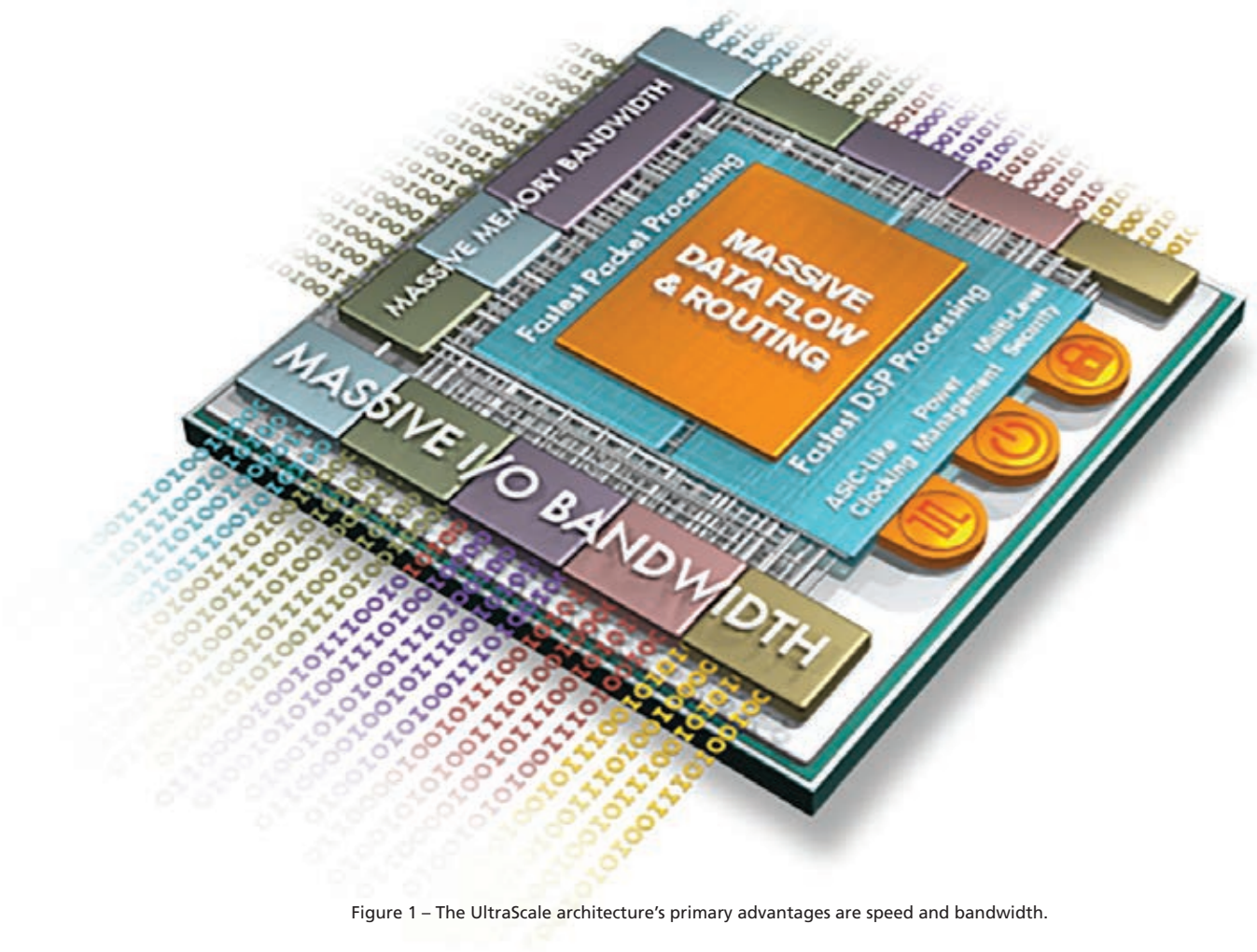

Figure 1 – The UltraScale architecture's primary advantages are speed and bandwidth.

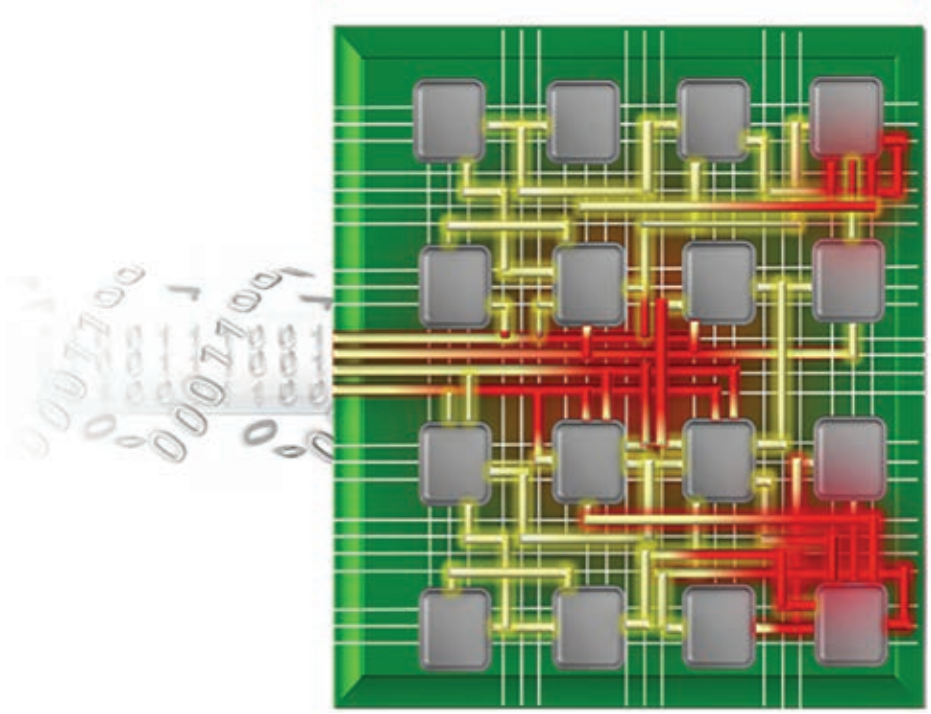

Figure 2 – The UltraScale architecture is capable of processing vast quantities of data.

Data is transported to and from FPGAs based on the UltraScale architecture through a combination of the high-performance parallel SelectIO™ and high-speed serial transceiver connectivity. I/O blocks enable cutting-edge memory interfacing and network protocols through flexible I/O standards and voltage support. The different serial transceivers in the UltraScale architecture transfer data at up to 16.3 Gbps, providing all the performance required for mainstream serial protocols, and at up to 32.75 Gbps, enabling 25G+ backplane designs with dramatically lower power per bit than previous-generation transceivers. All transceivers in UltraScale FPGAs support the required data rates for PCI Express® Gen3 and Gen4, and integrated blocks for PCI Express enable FPGAs based on the UltraScale architecture to support up to x8 Gen3 Endpoint and Root Port designs.

CLOCKING AND BUFFERING DATA

All synchronous systems rely on one or more clock signals for circuit synchronization. Increasing system performance dictates higher clock frequency with larger device capacity, demanding both improved clock flexibility and lower total clock power.

The UltraScale architecture contains powerful, rearchitected clock-management circuitry, including clock synthesis, buffering and routing components that together provide a highly capable framework to meet design requirements. The clock network allows for extremely flexible distribution of clocks within the FPGA to minimize the skew, power consumption and delay associated with clock signals. In addition, the clock-management technology is tightly integrated with dedicated memory-interfacing circuitry to enable support for high-performance external memories, including DDR4. Clock segmentation and new clock-gating granularity provide extra control of clock power consumption vs. existing FPGAs.

A dramatic increase in the number of global-capable clock buffers compared with previous and competing FPGAs provides a significant advantage to designers' productivity. Historically, it has been necessary to be frugal with global buffer usage, with only 32 global clock buffers located in the center of the FPGA. The UltraScale architecture has a liberal distribution of global-capable clock buffers throughout the architecture, providing resources where they are required and reducing the need to be parsimonious. In addition, Xilinx has greatly simplified the types of clock buffers over previous FPGA generations, with all the clock-switching, clock-dividing and clock-enabling functionality maintained. The result is a wealth of flexible, capable clock buffers with all the functionality just where it's needed.

STORING, PROCESSING AND ROUTING DATA

The key to any system is its ability to process, manipulate and convert the data it receives (Figure 2). Increasing system complexity requires a combination of general-purpose fabric with more specialist functions dedicated to specific types of data processing.

There are many elements to the fabric of today's FPGAs: configurable logic blocks (CLBs) containing six-input lookup tables (LUTs) and flip-flops; DSP slices with 27x18 multipliers; and 36-kbit Block RAMs with built-in FIFO and ECC support. These resources are all linked together with an abundance of high-performance, low-latency interconnect.

In addition to logical functions, the CLBs provide shift register, multiplexer and carry-logic functionality as well as the ability to configure the LUTs as distributed memory to complement the highly capable and configurable Block RAMs. The DSP slices—with new 96-bit-wide XOR functionality, wider 27-bit pre-adder and 30-bit input—perform numerous independent functions including multiply-accumulate, multiply-add and pattern detect. In addition to the device interconnect, in devices enabled using second-generation SSI 3DIC technology, signals can cross between super-logic regions using dedicated, low-latency interface tiles. These combined routing resources enable easy support for next-generation data bus widths, allowing device utilization of better than 90 percent.

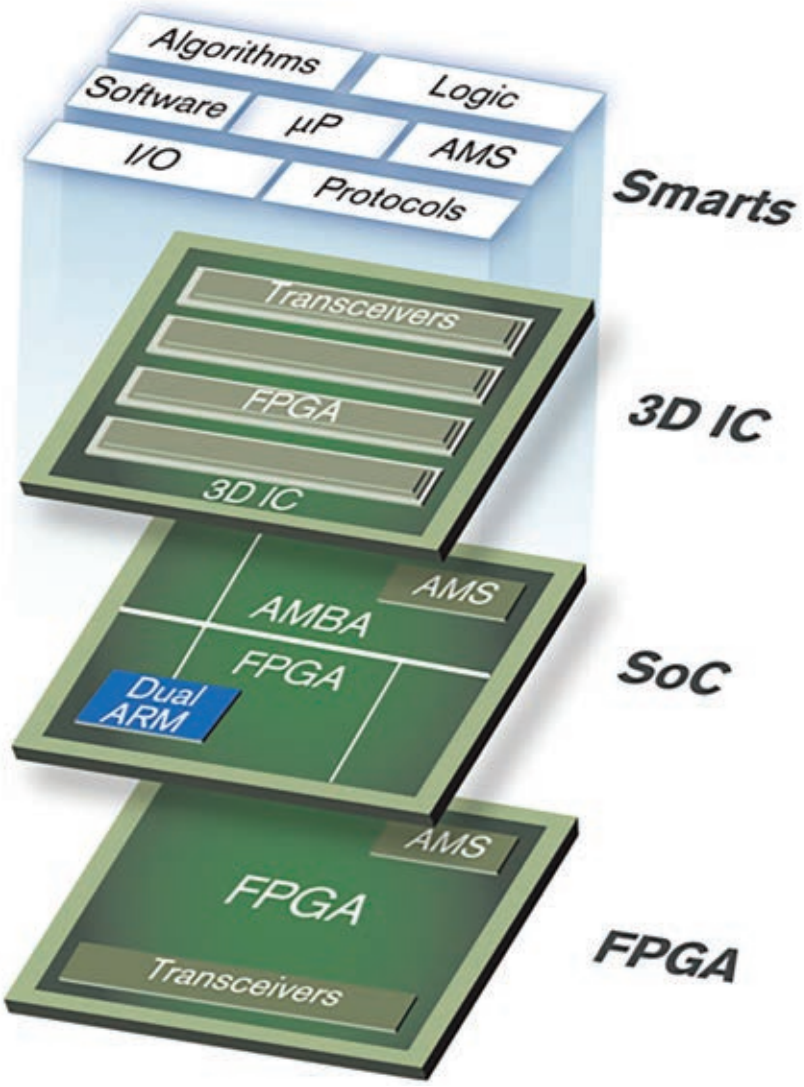

Figure 3 – UltraScale devices add popular functions to industry-leading technology.

EASING THE DESIGN CHALLENGE

The architectural enhancements delivered in the UltraScale architecture enable designers to pack more design in the same area but, in addition, device size is increasing. The result of being able to fit more design into a single device is a major benefit but places pressure on the design team to be able to implement their specified design quickly in order for their end product to achieve the fastest possible time-to-market. With the UltraScale architecture and the co-optimized Vivado® Design Suite, Xilinx delivers several time-saving and productivity-enhancing solutions.

INTEGRATING CORE FUNCTIONS

The flexibility of programmability is a valuable asset but, as with many things, it does not come free. A function built out of programmable resources can be larger, possibly even slower, than a block dedicated to the same function. Of course, by their very nature, FPGAs are predominantly programmable. But Xilinx FPGAs contain the right balance of dedicated-function, integrated IP to enable users to quickly implement commonly used functions (Figure 3). The UltraScale architecture contains integrated blocks for several popular communications protocols. There are multiple integrated blocks for PCI Express, 100G Ethernet and 150G Interlaken in Kintex UltraScale and Virtex UltraScale devices, all fully tested and verified, providing guaranteed functionality.

In addition to the communication protocols, every I/O bank contains a programmable memory PHY, configurable by the Memory Interface Generator (MIG) tool. This is a great illustration of integrating when necessary. The memory PHY and some of the control logic are created as a programmable dedicated function, but the digital portion of the memory interface is built out of device fabric, providing all the necessary customization and support for different modes that a dedicated circuit could struggle to offer.

Within the device fabric are numerous other blocks, tailored to perform specific functions while maintaining an element of programmability. Designers can configure the block memories in numerous depths and widths, cascading to make larger, low-power arrays. The DSP slices have many modes that allow the user access to the various components of the block, depending on the chosen function. So there is a wealth of functionality across the UltraScale architecture beyond mere gates and registers.

CUSTOMIZABLE, REPEATABLE IP ENHANCES PRODUCTIVITY

Every design consists of various architectural building blocks connected together to build a system. Few functions are so established in the industry that it makes economic sense to provide them as dedicated, fixed-function blocks. Rather, the optimum method is to design a function to be built from programmable logic, verify that function and then reuse the function whenever it is needed. The concept of IP in this form has been around for many generations, but Xilinx has recently introduced several productivity enhancements (Figure 4).

PLUG-AND-PLAY IP

In 2012, Xilinx adopted the ARM® AMBA® AXI4 interface as the standard

Figure 4 – Vivado tools accelerate the creation and implementation of complex designs.

interface for plug-and-play IP. Using a single, standard interface makes IP integration far easier than in the past, consolidating a broad array of interfaces into one, with designers no longer expected to understand numerous different interfaces. The UltraScale architecture continues to benefit from the flexibility and scalability of AXI4 interconnects to allow designers to achieve the fastest time-to-market while simultaneously optimizing IP for performance, area and power consumption with different AXI4 interconnect protocols, including AXI4-Lite and AXI4-Stream.

The Vivado IP Packager and IP Catalog leverage the IP-XACT standard, originally created by the SPIRIT Consortium as a standard structure for packaging, integrating and reusing IP within tool flows. IP-XACT is now an approved IEEE standard (IEEE1685-2009). The Vivado IP Packager makes a design with its constraints, testbenches and documentation available in an extensible IP catalog on a local or shared drive. The Vivado IP Catalog enables users to combine their own IP with Xilinx and third-party IP in order that all IP can be shared across a design team in a consistent and easy-to-use manner.

VIVADO IP INTEGRATOR

The Vivado IP Integrator (Figure 5) is an IP-centric design flow for accelerating time-to-system integration, making it quicker and easier to put together a system from its constituent parts. With an interactive graphical user interface, IPI provides intelligent autoconnection of IP interfaces, one-click IP subsystem generation and powerful debug capability, enabling designers to quickly and easily connect up any and all of the IP in their IP catalog. This capability enables designers to rapidly assemble complex systems that consist of design sources from many origins—some free, some purchased, some created in-house—with the knowledge that all the building blocks are correctly configured. Getting from concept to debug has never been faster.

In short, the UltraScale architecture includes architectural innovations in many key areas to successfully meet the aggressive demands of next-generation, high-performance designs. Ensuring the ability to implement designs with wide data buses at ever-increasing system frequencies, as UltraScale does, is a major piece of the puzzle. However, with device size and complexity increasing, it is critical to enable designers to continue ramping productivity. Providing a combination of integrated blocks and preverified IP, Xilinx provides the designer with all the tools necessary to implement a superior solution, faster.

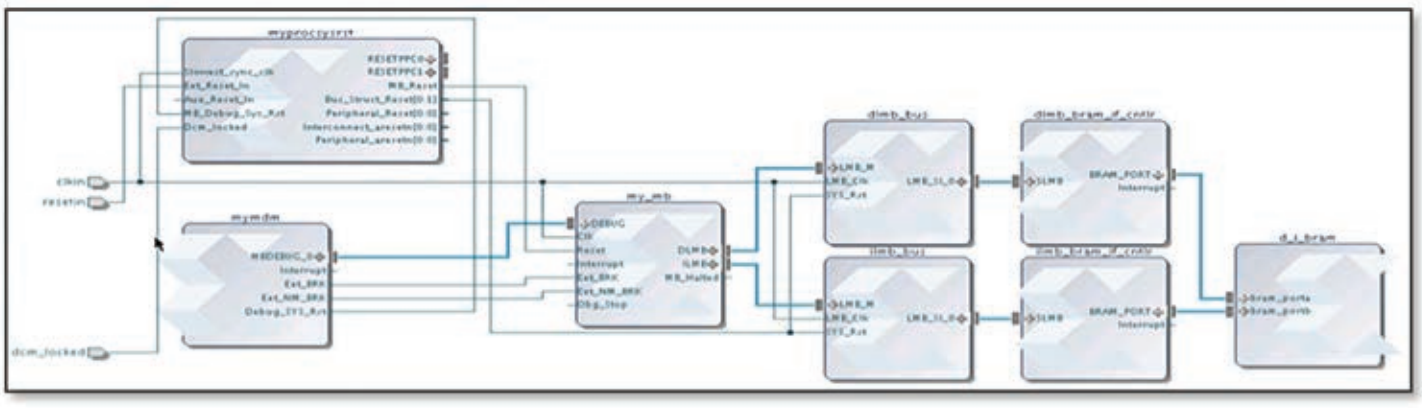

Figure 5 – Building a design in IP Integrator is a simple matter of connecting IP blocks.