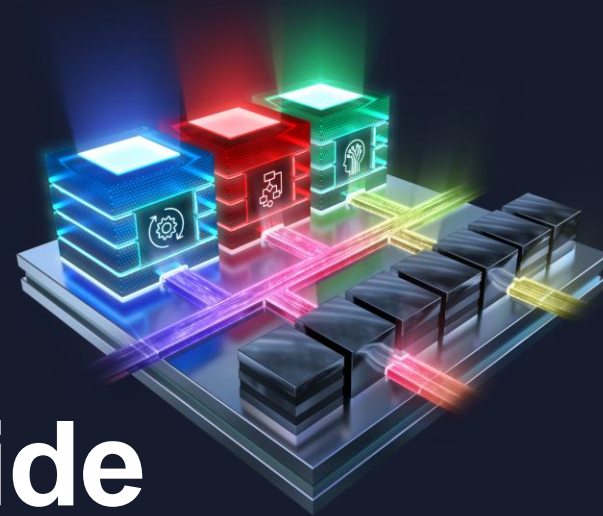




Versal® ACAP Prime Series Product Selection Guide



Industry's First Adaptive Compute Acceleration Platform (ACAP)

Versal® Prime Series – Resources

		VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902	
Adaptable Engines	System Logic Cells (K)	329	693	1,238	981	1,968	1,139	1,575	1,969	2,233	
	LUTs	150,272	316,928	565,760	448,512	899,840	520,704	719,872	900,224	1,020,928	
	NoC Master / NoC Slave Ports	5	9	18	21	28	21	30	28	42	
	Distributed RAM (Mb)	5	10	17	14	27	16	22	27	31	
Memory	Total Block RAM (Mb)	5	18	40	34	34	21	49	47	70	
	Total UltraRAM (Mb)	44	50	80	130	130	74	127	190	181	
	Total PL Memory (Mb)	54	78	137	178	191	111	198	264	282	
	DDR Memory Controllers	1	2	4	3	4	3	3	4	3	
Intelligent Engines	DDR Bus Widths	64	128	256	192	256	192	192	256	192	
	DSP Engines	464	832	1,696	1,312	1,968	1,312	1,904	3,984	2,672	
Scalar Engines	Application Processing Unit	Dual-core Arm® Cortex-A72, 48KB/32KB L1 Cache w/ parity & ECC; 1MB L2 Cache w/ ECC									
	Real-time Processing Unit	Dual-core Arm Cortex-R5F, 32KB/32KB L1 Cache, and 256KB TCM w/ECC									
	Memory	256KB On-Chip Memory w/ECC									
	Connectivity	Ethernet (x2); USB 2.0 (x1); UART (x2); SPI (x2); I2C (x2); CAN-FD (x2)									
Serial Transceivers	GTY Transceivers	0	24	24	44	44	0	0	0	0	
	GTYP Transceivers	8	0	0	0	0	32 ⁽¹⁾	8	28 ⁽¹⁾	8	
	GTM Transceivers (56Gb/s)	0	0	0	0	0	0	40	20	40	
Integrated Protocol IP	CCIX & PCIe® w/DMA (CPM)	-	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	1 x Gen4x16, CCIX	2 x Gen5x8, CCIX	-	2 x Gen5x8, CCIX	-	
	PCI Express®	1 x Gen4x8	2 x Gen4x8	2 x Gen4x8	4 x Gen4x8	4 x Gen4x8	4 x Gen5x4	2 x Gen5x4	2 x Gen5x4	2 x Gen5x4	
	100G Multirate Ethernet MAC	1	2	2	4	4	2	6	2	6	
Ordering Information	Extended Temp ²	-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE					-1MSE, -1LSE, -2MSE, -2MLE, -2LSE, -2LLE, -3HSE				
	Industrial Temp ²	-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI, -2LLI, -2HSI					-1MSI, -1MLI, -1LSI, -1LLI, -2MSI, -2MLI				

Notes:

- 16 GTYP transceivers are dedicated to the CPM for PCI Express use.
- In extended and industrial temperature grades, some ordering combinations can operate for a limited time with a junction temperature of 110°C. Timing parameters adhere to the same speed file at 110°C as they do below 110°C, regardless of operating voltage. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime.

Versal® Prime Series – Packaging

		VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902
Package	Package Dimensions (mm)	Ball Pitch (mm)	XPIO DDR Only, XPIO DDR+PL HDIO, MIO GTY, GTYP, GTM							
SFVA784	23x23	0.8	132, 84 22, 78 0, 8, 0							
NBVB1024	31x31	0.92		132, 84 22, 78 16, 0, 0	132, 192 22, 78 16, 0, 0					
NFVB1369	35x35	0.92				132, 246 22, 78 16, 0, 0				
NSVF1369	35x35	0.92		168, 156 22, 78 8, 0, 0	168, 480 22, 78 8, 0, 0					
VFVC1596	37.5x37.5	0.92		168, 264 22, 78 24, 0, 0	168, 480 22, 78 24, 0, 0					
VFVC1760 ⁽¹⁾	40x40	0.92				132, 246 44, 78 44, 0, 0	132, 246 44, 78 44, 0, 0			
VSVD1760 ^(2,3)	40x40	0.92		168, 156 0, 78 16, 0, 0	168, 480 0, 78 16, 0, 0		186, 462 0, 78 24, 0, 0			
VFVF1760 ⁽⁴⁾	40x40	0.92						180, 306 22, 78 0, 8, 40		180, 306 22, 78 0, 8, 40
VSVA2197	45x45	0.92				192, 294 44, 78 44, 0, 0	186, 462 44, 78 44, 0, 0			
VSVC2197 ⁽⁴⁾	45x45	0.92					186, 300 44, 78 0, 32, 0		132, 516 0, 78 0, 28, 20	

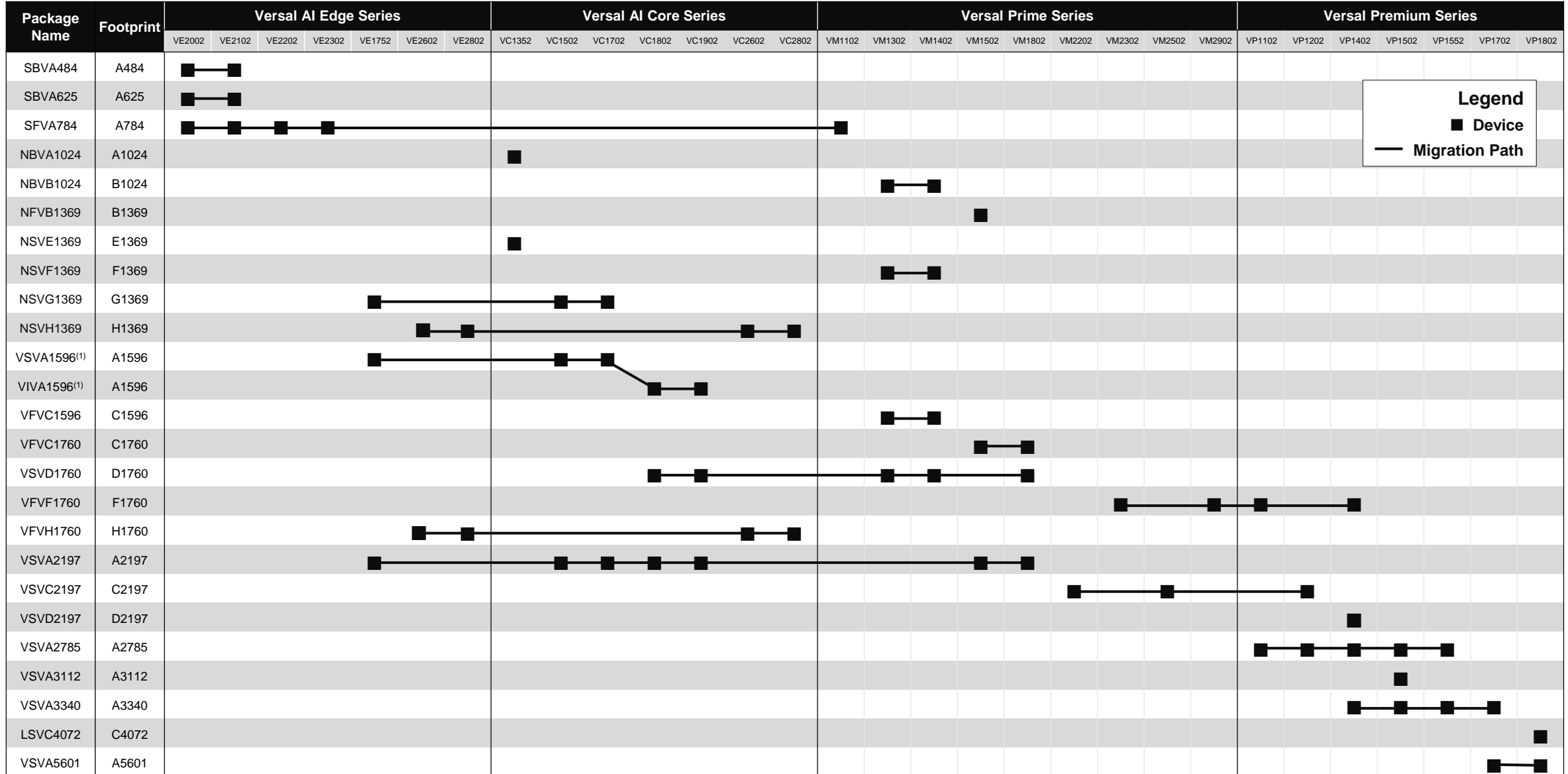
Notes:

1. Devices in VFVC1760 support peak LPDDR4 in 162 I/O only. The remaining 216 I/O support limited data rates. See the associated data sheet.
2. VM1302 in VSVD1760 supports peak LPDDR4 in 162 I/O only. The remaining 162 I/O support limited data rates. See the associated data sheet.
3. VM1402 in VSVD1760 supports peak LPDDR4 in 324 I/O only. The remaining 324 I/O support limited data rates. See the associated data sheet.
4. Some packages are compatible with Versal Premium series devices.

Versal® Prime Series – Figures of Merit

		VM1102	VM1302	VM1402	VM1502	VM1802	VM2202	VM2302	VM2502	VM2902	
Adaptable Engines	Adaptable Engine Peak Perf – INT1	TOPs	157	336	591	469	941	544	753	941	1067
	Adaptable Engine Peak Perf – INT2	TOPs	72	154	271	215	431	250	345	431	489
	Adaptable Engine Peak Perf – INT4	TOPs	19	40	70	56	112	65	89	112	127
	Adaptable Engine Peak Perf – INT8	TOPs	5	10	18	14	29	17	23	29	33
	NoC Cross-sectional Bandwidth	Tb/s	0.6	0.6	1.1	1.7	2.2	1.7	1.7	2.2	1.7
Memory	Total Bandwidth – Block RAM	Tb/s	22	72	166	137	139	86	202	193	285
	Total Bandwidth – UltraRAM	Tb/s	16	19	30	49	49	28	48	72	69
	Total SRAM Bandwidth	Tb/s	39	91	196	186	188	114	250	265	354
	DDR4 Memory Bandwidth	GB/s	25.6	51.2	102.4	76.8	102.4	76.8	76.8	102.4	76.8
	LPDDR4 Memory Bandwidth	GB/s	34.1	68.3	136.5	102.4	136.5	102.4	102.4	136.5	102.4
Intelligent Engines	DSP Engine Peak Perf – INT8	TOPs	3.2	5.9	11.7	9.1	13.6	9.1	13.1	27.5	18.4
	DSP Engine Peak Perf – INT24	TOPs	1.1	2.0	3.9	3.0	4.5	3.0	4.4	9.2	6.1
	DSP Engine Peak Perf – CINT18	Complex TOPs	0.5	0.8	1.7	1.3	1.9	1.3	1.9	3.9	2.6
	DSP Engine Peak Perf – FP32	TFLOPs	0.7	1.4	2.7	2.1	3.2	2.1	3.1	6.4	4.3
Scalar Engines	Arm Cortex-A72 Performance	DMIPs	18,942	18,942	18,942	18,942	18,942	19,516	19,516	19,516	19,516
	Arm Cortex-R5F Performance	DMIPs	2,672	2,672	2,672	2,672	2,672	2,672	2,672	2,672	2,672
I/O	Transceiver Bandwidth	Tb/s	0.51	1.35	1.35	2.48	2.48	2.10	7.75	4.09	11.36
	Sensor I/O Bandwidth	Gb/s	269	845	1,536	941	1,478	960	979	1,651	979

Versal® ACAP Migration Table



Legend

- Device
- Migration Path

Note:

1. VSVA1596 package dimensions are 37.5x37.5mm, VIVA1596 package dimensions are 40x40mm with 1.25mm overhang.

Versal® ACAP Ordering Information



Device Name			Device Attributes					Package Definition			
XC	V	C	1902	-1	M	S	E	V	S	V	D1760
Xilinx XC: Commercial XA: Automotive XQ: Defense	Architecture Versal	Series Name E: AI Edge C: AI Core M: Prime P: Premium H: HBM	Device Number Digits 1-3: Value Identifier Digit 4: # of Primary Cores	Speed Grade -1: Slowest -2: Mid -3: Highest	Voltage L: Low (0.7V) M: Mid (0.80V) H: High (0.88V)	Static Screen S: Standard L: Low Static	Temp Grade E: 0 to 110°C ⁽¹⁾ I: -40 to 110°C ⁽¹⁾ Q: -40 to +125°C M: -55 to +125°C	Ball Pitch V: 0.92mm, w/LSC N: 0.92mm, no LSC S: 0.8mm L: 1.0mm	Lid S: Lidless, w/Stiffener Ring F: Lidded B: Lidless, no Stiffener Ring H: Lidded Overhang I: Lidless, w/Stiffener Ring & Overhang	RoHS6 Code ⁽²⁾ V: Pb-free Ball Q: Eutectic Ball R: Ruggedized, Eutectic Ball	Footprint

Note:
 1. Operation at 110°C Tj is limited to 3% of the device lifetime and can occur sequentially or at regular intervals as long as the total time does not exceed 3% of device lifetime—except -1E and -3E (standard 0–100°C).
 2. All packages have Pb-free bumps.

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