Designing with Ethernet MAC Controllers

Connectivity 3

CONN-EMAC-ILT (v1.0)

Course Specification

Course Description

Become acquainted with the various solutions that Xilinx offers for Ethernet connectivity. Learn the basics of the Ethernet standard, protocol, and OSI model while applying Xilinx solutions via hands-on laboratory exercises. Perform simulation to understand fundamental principles and obtain the knowledge to assess hardware design considerations and software development requirements. Become familiar with Ethernet IP core design architectures, core IP port naming conventions, and signal waveforms.

Level – Connectivity 3

Course Duration – 2 days

Course Part Number – CONN-EMAC-ILT

Who Should Attend? – Engineers who would like to come up to speed on utilizing Xilinx Ethernet connectivity solutions

Prerequisites

- FPGA design experience
- Completion of the *Designing FPGAs Using the Vivado Design Suite 1* course or equivalent knowledge of Xilinx Vivado® software implementation tools
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Vivado Design or System Edition 2014.3

Hardware

- Architecture: 7 series and UltraScale™ FPGAs*
- Demo board: Kintex®-7 FPGA KC705 board (optional)*

* This course focuses on the 7 series, UltraScale, and Zynq® SoC architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the basics of the Ethernet standard, protocol, and OSI model
- Identify the various solutions that Xilinx offers for Ethernet connectivity
- Utilize various Ethernet cores either in a standalone mode or as a peripheral in a processor-based design
- Use simulation to become familiar with IP core port names and operations
- Explore the Xilinx-provided example software application using the lwIP stack
- Integrate Ethernet IP into your design using the Vivado Design Suite

Course Outline

Day 1

- Introduction
- Ethernet Basics
- Network Protocols, Ethernet Interfaces, and Hardware
- **Lab 1:** Exploring Ethernet Frames
- Physical Layer
- AXI Interface
- **Lab 2:** Advanced Ethernet Frames
- Xilinx EMAC Offerings
- **Lab 3:** AXI Ethernet Example Design

Day 2

- 10/100/1000 EMAC Solutions
- Processor-Based Ethernet
- **Lab 4:** Processor-Based Ethernet Design
- 10/25/40/100GE Solutions
- Ethernet Odds and Ends
- **Lab 5:** Analyzing 10GE MAC Frames

Lab Descriptions

- **Lab 1:** Exploring Ethernet Frames – Perform a functional simulation of the Tri-Mode Ethernet MAC LogiCORE™ IP. This IP is available through the Vivado IP catalog tool. A Vivado Design Suite project, based on the Tri-Mode Ethernet MAC example design, is provided and includes a simulation testbench. You will use the Vivado simulator to analyze Ethernet frames and identify the components of the frames. You will then modify the testbench to view its effect on core behavior.
- **Lab 2:** Advanced Ethernet Frames – Perform a functional simulation of a Vivado Design Suite project, based on the Tri-Mode Ethernet MAC example design, that is provided with several simulation testbenches. You will use these testbenches to generate various kinds of frames and observe how the core behaves to these received frames. AXI MAC register configuration commands will be modified to affect the behavior of the MAC core. You will also study various signals involved in identifying frames and classify them into good frames or bad frames.
- **Lab 3:** AXI Ethernet Example Design – Create a new Vivado Design Suite project, use the IP catalog tool to generate an AXI Ethernet Subsystem core, and open the Xilinx-provided example design. You will then analyze, simulate, synthesize, and implement the design for the Kintex-7 FPGA.
- **Lab 4:** Processor-Based Ethernet Design – Use the Vivado IP integrator tool to create an Ethernet-based embedded system. The design will be based around the MicroBlaze® processor and the Ethernet Lite controller. The SDK tool will be used to create and build the *lwIP Echo Server* example software application. This lab encompasses the entire design experience from cradle to grave.
- **Lab 5:** Analyzing 10GE MAC Frames – Investigate the PHY and client interfaces of the 10-Gigabit Ethernet MAC LogiCORE IP, available in the Vivado IP catalog, by performing a functional simulation. You will use the Vivado simulator to view these waveform signals.

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