Designing with UltraScale FPGA Transceivers

Connectivity 3

CONN-MGTUS-ILT (v1.0)

Course Specification

Course Description

Learn how to employ serial transceivers in your UltraScale™ FPGA design. Understand and utilize the features of the serial transceiver blocks, such as 8B/10B and 64B/66B encoding, channel bonding, clock correction, and comma detection. Additional topics include use of the UltraScale FPGAs Transceiver Wizard, synthesis and implementation considerations, board design as it relates to the transceivers, and test and debugging. This course combines lectures with practical hands-on labs.

Level – Connectivity 3

Course Duration – 2 days

Course Part Number – CONN-MGTUS-ILT

Who Should Attend? – FPGA designers and logic designers

Prerequisites

- Verilog experience (or the *Designing with Verilog* or the *Designing with VHDL* course)
- Familiarity with logic design (state machines and synchronous design)
- Basic knowledge of FPGA architecture and Xilinx implementation tools are helpful
- Familiarity with serial I/O basics and high-speed serial I/O standards is also helpful

Software Tools

- Vivado® System Edition 2015.3
- Mentor Graphics Questa Advanced Simulator 10.4

Hardware

- Architecture: UltraScale FPGAs
- Demo board: None

* This course focuses on the UltraScale architecture. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations.

After completing this comprehensive training, you will have the necessary skills to:

- Describe and utilize the ports and attributes of the serial transceivers in the UltraScale FPGAs
- Effectively utilize the following features of the gigabit transceivers:
  - 64B/66B and other encoding/decoding, comma detection, clock correction, and channel bonding
  - Pre-emphasis and receive equalization
- Use the UltraScale FPGAs Transceivers Wizard to instantiate GT primitives in a design
- Access appropriate reference material for board design issues involving signal integrity and the power supply, reference clocking, and trace design
- Use the IBERT design to verify transceiver links on real hardware

Course Outline

Day 1

- UltraScale FPGA Overview
- UltraScale FPGA Transceivers Overview
- UltraScale FPGA Transceivers Clocking and Resets
- Transceiver Wizard Overview
- **Lab 1:** Transceiver Core Generation
- Transceiver Simulation
- **Lab 2:** Transceiver Simulation
- PCS Layer General Functionality

Day 2

- PCS Layer Encoding
- **Lab 3:** 64B/66B Encoding
- Transceiver Implementation
- **Lab 4**: Transceiver Implementation
- PMA Layer Details
- Transceiver Board Design Considerations
- Transceiver Test and Debugging
- **Lab 5**: IBERT Design
- Transceiver Application Examples

Lab Descriptions

- **Lab 1:** Transceiver Core Generation – Use the UltraScale FPGAs Transceivers Wizard to create instantiation templates.
- **Lab 2:** Transceiver Simulation – Simulate the transceiver IP by using the IP example design.
- **Lab 3:** 64B/66B Encoding – Generate a 64B/66B transceiver core by using the UltraScale FPGAs Transceivers Wizard, simulate the design, and analyze the results.
- **Lab 4:** Transceiver Implementation – Implement the transceiver IP by using the IP example design.
- **Lab 5:** IBERT Design – Verify transceiver links on real hardware.

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