Embedded Systems Design

Embedded Hardware 3

EMBD-HW-ILT (v1.0)

Course Specification

Course Description

This course is designed to bring FPGA designers up to speed on developing embedded systems using the Vivado® Design Suite. The features and capabilities of both the Zynq® System on a Chip (SoC), Zynq UltraScale+™ MPSoC, and the MicroBlaze™ soft processor are covered in lectures, demonstrations, and labs, along with general embedded concepts, tools, and techniques. The hands-on labs provide students with experience designing, expanding, and modifying an embedded system, including adding and simulating a custom AXI-based peripheral.

The Xilinx Zynq families enable a new level of system design capabilities over previous embedded technologies, which is highlighted throughout the course.

Level – Embedded Hardware 3

Course Duration – 2 days

Course Part Number – EMBD-HW-ILT

Who Should Attend? – Engineers who are interested in developing embedded systems with the Xilinx Zynq SoC, Zynq UltraScale+ MPSoC, and/or MicroBlaze soft processor core

Prerequisites

- FPGA design experience
- Completion of the *Essentials of FPGA Design* course or equivalent knowledge of Xilinx Vivado® software implementation tools
- Basic understanding of C programming
- Basic understanding of microprocessors
- Some HDL modeling experience

Software Tools

- Vivado Design or System Edition 2018.1

Hardware

- Architectures: Zynq-7000 SoC (Cortex™-A9 processor), Zynq UltraScale+ MPSoC (Cortex-A53 and Cortex-R5 processors), and MicroBlaze processor*
- Demo board: Zynq-7000 SoC ZC702 or ZedBoard*

* This course focuses on the Zynq-7000 SoC and Zynq UltraScale+ MPSoC architectures. Check with your local Authorized Training Provider for the specifics of the in-class lab board or other customizations. The Zynq UltraScale+ MPSoC software projects use QEMU rather than a physical board.

After completing this comprehensive training, you will have the necessary skills to:

- Describe the various tools that encompass a Xilinx embedded design
- Rapidly architect an embedded system containing a Cortex-A9/A53/R5 or MicroBlaze processor using the Vivado IP integrator and Customization Wizard
- Develop software applications utilizing the Eclipse-based Software Development Kit (SDK)
- Create and integrate an IP-based processing system component in the Vivado Design Suite
- Design and add a custom AXI interface-based peripheral to the embedded processing system
- Simulate a custom AXI interface-based peripheral using verification IP (VIP)

Course Outline

Day 1

- Embedded UltraFast Design Methodology {Lecture, Demo}
- Overview of Embedded Hardware Development {Lecture, Demo}
- Driving the IP Integrator Tool {Lecture, Lab}
- Overview of Embedded Software Development {Lecture}
- Driving the SDK Tool {Lecture, Lab}
- AXI: Introduction {Lecture}
- AXI: Variations {Lecture}
- AXI: Transactions {Lecture, Lab, Demo}
- Introduction to Interrupts {Lecture}
- Interrupts: Hardware Architecture and Support {Lecture}

Day 2

- AXI: Connecting AXI IP {Lecture, Demo}
- Creating a New AXI IP with the Wizard {Lecture, Lab}
- AXI: BFM Simulation Using Verification IP (Lecture, Lab}
- MicroBlaze Processor Architecture Overview {Lecture, Lab}
- MicroBlaze Processor Block Memory Usage {Lecture}
- Zynq-7000 SoC Architecture Overview {Lecture, Lab, Demo}
- Zynq UltraScale+ MPSoC Architecture Overview {Lecture, Lab, Demo}

Topic Descriptions

Day 1

- Embedded UltraFast Design Methodology – Outlines the different elements that comprise the Embedded Design Methodology.
- Overview of Embedded Hardware Development – Overview of the embedded hardware development flow.
- Driving the IP Integrator Tool – Describes how to access and effectively use the IPI tool.
- Overview of Embedded Software Development – Reviews the process of building a user application.
- Driving the SDK Tool – Introduces the basic behaviors required to drive the SDK tool to generate a debuggable C/C++ application.
- AXI: Introduction – Introduces the AXI protocol.
- AXI: Variations – Describes the differences and similarities among the three primary AXI variations.
- AXI: Transactions – Describes different types of AXI transactions.
- Introduction to Interrupts – Introduces the concept of interrupts, basic terminology, and generic implementation.
- Interrupts: Hardware Architecture and Support – Reviews the hardware that is typically available to help implement and manage interrupts.

Day 2

- AXI: Connecting AXI IP – Describes the relationships between different types of AXI interfaces and how they can be connected to form hierarchies.
- Using the Create and Import Wizard to Create a New AXI IP – Explains how to use the Create and Import Wizard to create and package an AXI IP.
- AXI: BFM Simulation Using Verification IP – Describes how to perform BFM simulation using the Verification IP.
- MicroBlaze Processor Architecture Overview – Overview of the MicroBlaze microprocessor architecture.
- MicroBlaze Processor Block Memory Usage – Highlights how block RAM can be used with the MicroBlaze processor.
- Zynq-7000 SoC Architecture Overview – Overview of the Zynq-7000 SoC architecture.
- Zynq UltraScale+ MPSoC Architecture Overview – Overview of the Zynq UltraScale+ MPSoC architecture.

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