Xilinx Partial Reconfiguration Tools and Techniques
FPGA 4

Course Specification

- Implement a PR system in an embedded environment
- Debug PR designs

Course Outline

Day 1
- Introduction to Partial Reconfiguration
- Demo: Introduction to Partial Reconfiguration
- Partial Reconfiguration Flow
- Lab 1: Partial Reconfiguration Tool Flow
- Lab 2: Partial Reconfiguration Project Flow
- Lab 3: Floorplanning the PR Design
- Partial Reconfiguration Design Considerations
  - Optional: FPGA Configuration Overview
- Partial Reconfiguration Bitstreams
- Demo: Partial Reconfiguration Controller (PRC) IP
- Lab 4: Using the Partial Reconfiguration Controller in a PR Design

Day 2
- Partial Reconfiguration: Managing Timing
- Lab 5: Partial Reconfiguration Timing Analysis and Constraints
- Partial Reconfiguration in Embedded Systems
- Lab 6: Partial Reconfiguration in Embedded Systems
- Debugging Partial Reconfiguration Designs
- Lab 7: Debugging a Partial Reconfiguration Design
- Partial Reconfiguration Design Recommendations
- PCle Core and Partial Reconfiguration

Lab Descriptions

- Lab 1: Partial Reconfiguration Tool Flow – Illustrates the basic Vivado Design Suite Partial Reconfiguration flow. At the completion of this lab, you will download a partial bitstream to the demo board via the JTAG connection.
- Lab 2: Partial Reconfiguration Project Flow – Illustrates Partial Reconfiguration (PR) project flow in the Vivado® Design Suite. At the end of this lab, you will be able to create multiple RMfs and configurations using Partial Reconfiguration Wizard.
- Lab 3: Floorplanning the PR Design – Illustrates how to create efficient Pblocks for a Partial Reconfiguration design. At the end of this lab, you will understand the impact of the SNAPPING_MODE property for a Pblock.
- Lab 4: Using the Partial Reconfiguration Controller in a PR Design – Illustrates using the PRC IP and hardware triggers to manage partial bitstreams.
- Lab 7: Debugging a Partial Reconfiguration Design – Demonstrates using ILA cores to debug PR designs and shows which signals to monitor during debugging.
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